Folded-Patch Chip-Size Antennas for Wireless Microsystems

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Abstract – **We report on design and fabrication of a folded-patch chip-size antenna for operation at 5.7 GHz and use in short-range wireless communications. Application of wafer-level chip-scale packaging (WLCSP) techniques like adhesive wafer bonding and through-wafer electrical via formation, combined with the selected antenna type allows on-chip integration and is the main novelty of our design work. This antenna, built on two stacked substrates, allows size reduction down to 4.5x4x1 mm^3 and has projected efficiency of 66%.**

Keywords – **Folded-patch antenna, chip-size antenna, antenna integration.**

I. Introduction

Wireless small-size distributed microsystems equipped with short-range communication capabilities will highly be facilitated if cheap and easy-to-use 'on-chip' or 'in-package' solutions would be available. However, a chip-size antenna, as the key element in achieving a fully integrated solution, and notwithstanding all the development efforts, still remains to be an open challenge. Together with inductances, the on-chip antenna integration can be an added benefit in order to achieve a fully integrated RF microsystem.

The antenna integration depends on the possibility to fabricate the designed structures using integrated circuits compatible materials and processes. Also, on-chip integration requires the antenna to be small and to be realised on a low-loss substrate compatible with integrated circuits operation and fabrication [1]. Patch antennas on high-resistivity silicon (HRS) or on glass are two possible options [2, 3]. Concerning the antenna efficiency, the glass substrates are superior, due to higher losses observed in HRS [3]. On the other hand, HRS has significantly higher dielectric constant than glass (11.7 vs. 5-6), so using of HRS instead of glass provides a way to reduce antenna size.

To increase the patch antenna efficiency, application of bulk-micromachining technology for selective silicon removal underneath the antenna has been proposed. However, the resulting effective dielectric constant will be lower when the silicon is removed, which leads to a larger antenna. A folded shorted-patch antenna (FSPA) can be used instead, as a compact solution for the on-chip antenna integration [4]. Due to its rather complicated structure, its implementation is not trivial.

In this paper, design and process considerations for on-chip implementation of an FSPA are presented. This antenna can be built using two-stacked glass or HRS wafers, or a combination of both. Various options for achieving antenna integration within a microsystem using wafer level chip scale packaging (WLSCP) techniques are analyzed.

II. Antenna Modelling and Design

The proposed antenna was designed to operate inside the 5-6 GHz ISM band. The design presented here operates at 5.695 GHz. The simulation analysis was performed with HFSS 8.5 from Ansoft.

The proposed, on-chip integrated, folded shorted-patch antenna is shown in Fig. 1.

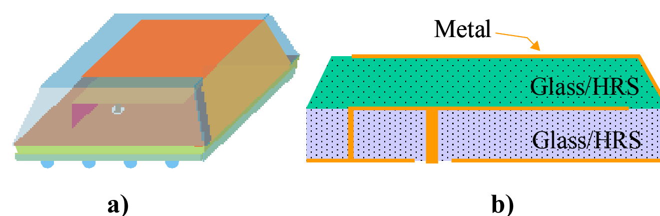


Figure 1: Folded shorted-patch antenna: a) envisioned application; b) antenna cross-section.

It consists of three horizontal metal sheets that are electrically connected by two vertical metal walls. All this is embedded in a dielectric substrate having certain

electrical permittivity and dielectric losses. These two parameters together with the antenna geometry and its actual dimensions will determine its radiation characteristics and overall performance.

For the best performance, the metal sheets should have minimum resistivity and the dielectric should be a low-loss material with high electrical permittivity. This allows achieving small antenna dimensions and high efficiency. At frequencies above 1 GHz, glass becomes a very attractive option. Its main advantages are low losses, reasonable ε_r, availability in a form of wafers with any required thickness and diameter, and, last but not least, low cost.

A FSPA can be realised with a stack of two wafers with patterned metal layers and through-wafer interconnects in the form of metallized vias. One way to reduce the aspect ratio of those trough-wafer vias is to use a thin wafer. However, the antenna performance depends on the wafer thickness. Table 1 summarizes the expected antenna performance for different options.

Table 1: Summary of antenna properties for different substrate thickness values.

Substrate Thickness [µm]	Frequency [GHz]	Bandwidth [MHz]	Efficiency [%]
100	5.4	17	23
250	5.63	39	48
500	5.71	62	66
800	5.6	88	76

The main drawback, when the wafer thickness is reduced, is the low efficiency obtained. High antenna efficiency requires thicker substrates (>300 µm) and therefore high aspect ratio vias in glass or HRS are required.

The design of such antenna requires the use of a 3D model. The proposed antenna model is shown in Fig. 2. As shown, the antenna model is mainly the result of two parts, the antenna itself and the feeding structure.

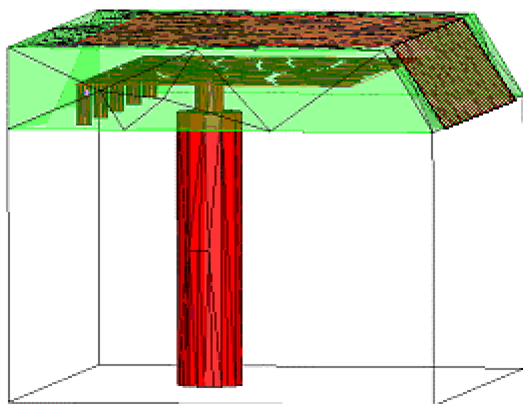


Figure 2: Model used to design the FSP antenna.

As mentioned before, the antenna is composed by the three metallic layers (ground, middle patch and upper patch), together with the feeding via and the shorting metallic walls. All this structure is supported by the substrate. Beneath the antenna is the feeding structure. A 50 Ω coaxial cable was used to feed this model since it was the most straightforward way to do it. The conductors in the coaxial used to feed the antenna are modeled as a lossless ideal metallic wall. Also, a metallic box is used to take into account the SMA connector influence.

A simplified model was built to compute the simulated results as fast as possible. In this way, to speed up the simulations, electrical walls boundary conditions were used instead of effective metallic layers. This approximation was made in all the antenna metallic parts, except the shorting and feeding vias. This was done since the aluminum metallic layers are only 2 µm thick, which is very small, when compared to other antenna dimensions. In this way, to get accurate results, the mesh would need to be very dense and the simulation time would increase.

To check the accuracy of that approximation, a model having the finite thickness of metallization layers was also built. The electric wall approximation may affects the electrical behavior since it doesn't include the metallic losses, due to the metal finite conductivity and skin depth. The losses associated with finite conductivity can be simulated by HFSS using the finite conductivity boundary. This boundary uses the skin depth to model the losses associated with the imperfect conductor. However, the thickness of the metallic layers (~10 µm for copper) may change the antenna operating characteristics, mainly the center frequency and bandwidth, and it was necessary to check how large can that shift be.

After performing several simulations with the described models it was found that the approximated model with the finite conductivity boundary give efficiency results very close to the results from the model which includes the finite thickness of the metallic layers. If the electric wall approximation is used, the obtained antenna efficiency is ~5 % higher. Also, the use of electric walls instead of a finite thickness may lead to a shift in the operating frequency. It was observed a shift from 5.7 GHz (electric wall) to 5.61 GHz (finite thickness).

Fig. 3 shows return loss of the proposed FSPA, considering the use of two stacked, 500 µm thick Corning Pyrex #7740 glass substrates and dimensions of 4.5x4x1 mm^3. Considering the use of these two stacked wafers, a simulated radiation efficiency of 66 % and bandwidth of 50 MHz at -10 dB return loss have been achieved.

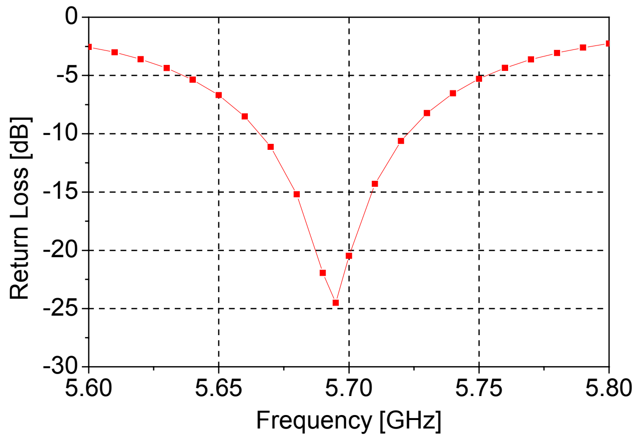


Figure 3: Simulated return loss of the FSPA.

The predicted far-field radiation pattern is displayed in Fig. 4. It shows that the power is being mainly radiated upwards and the antenna interference with backside devices is minimized.

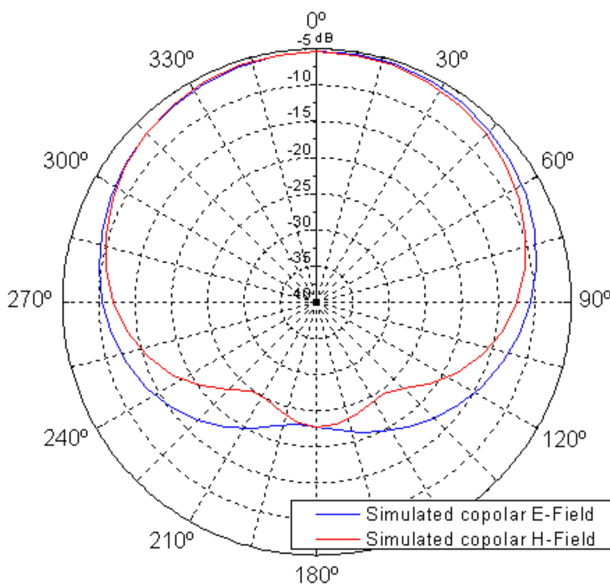


Figure 4: Simulated co-polar far-field gain patterns for FSPA operating at 5.695 GHz.

III. FABRICATION

Two different fabrication schemes for realization of on-chip integrated FSPAs have been proposed [5] and the antenna prototype fabrication is currently in progress. Both fabrication schemes are based on WLCSP techniques and are schematically shown in Fig. 5. This figure shows the fabrication sequence required when we use laser ablation or powder blasting.

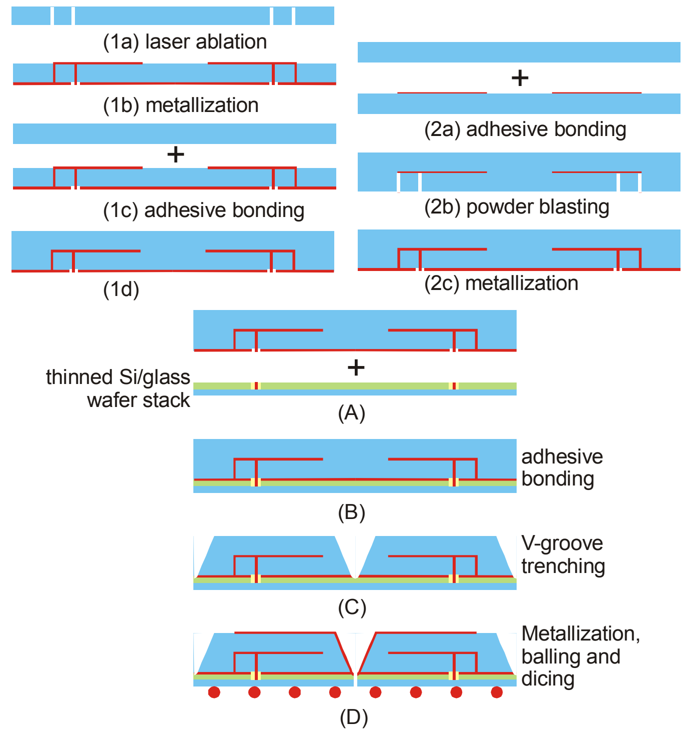
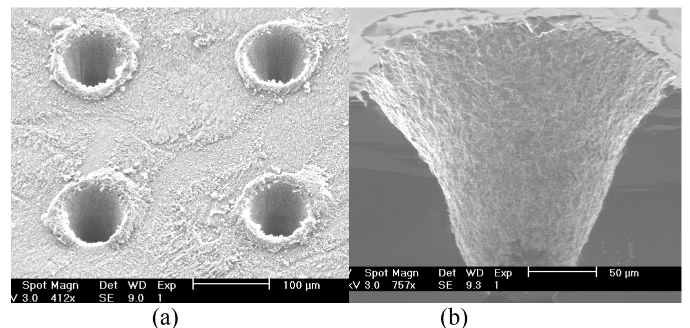


Figure 5: Schematic fabrication sequence using laser ablated vias (left); using powder blasted vias (right).

The most demanding fabrication step required to realize the proposed antenna structure, is the through-wafer high-aspect-ratio via forming in glass. There are various techniques that can be used for via fabrication in thick glass substrates (>300 µm), but all of them have severe limitations in their throughput or achievable aspect ratios. We have explored two of them: powder blasting and laser ablation (see Fig. 6).



(a) (b)

Figure 6: SEM picture of (a) 80 µm circular vias in a 500 µm glass substrate fabricated using a 193 nm excimer laser (front side); (b) cross-section of a 200 µm diameter powder-blasted via.

A. Powder blasting

Powder blasting is a widely used method in glass processing. Its main disadvantage is that the typical side-wall slope is about 75° which results in rather limited achievable aspect ratio of powder-blasted vias of ~2.5:1. Fig. 6b shows a cross sectional SEM photograph of a

powder-blasted, 200 µm diameter via in a 240 µm thick substrate. Higher aspect ratios are possible by applying this technique from both wafer sides.

Other interesting property of glass powder blasting, which we want to employ to simplify fabrication, is its selectivity to copper metalization.

B. Laser ablation

Glass starts to loose its transparency in the UV region and therefore excimer lasers are needed for glass ablation to form through wafer vias. Due to the limitations of the focusing system, direct ablation of the required pattern is not possible and an intermediate hard mask between the laser beam and glass wafer is required. Fig. 6a shows SEM photograph of 80 µm diameter vias formed in a 500 µm thick glass wafer using a 193 nm excimer laser. A 30:1 pattern reduction and projection optics avoid damage to the hard mask and provides high accuracy in pattern transfer.

C. Fabrication scheme

The schematic fabrication sequence is shown in Fig. 5 and has two options according the selected via-fabrication method. The first one (Fig. 5: 1a-1d) is based on laser ablation of high-aspect-ratio vias in glass with subsequent electroless plating and patterning of the bottom and middle Cu layers, followed by glass-to-glass adhesive bonding.

The second fabrication option (Fig. 5: 2a-2c) starts with deposition and patterning of Cu layer on a glass wafer followed by adhesive bonding to the upper glass wafer (Fig. 5: 2a). The encapsulated middle Cu patch is then reached by powder blasting (Fig. 5: 2b) employing its high selectivity between copper and glass etching. This step is followed by plating and patterning of the bottom Cu layer (Fig. 5: 2c).

In both cases, the fabrication sequence continues by bonding to a pre-processed core process silicon IC wafer (Fig. 5: B) and a V-groove trenching (Fig. 5: C) using shaped dicing blade [6]. Finally the upper Cu layer is deposited and patterned. The processing sequence is completed by singulation into individual dies by dicing (Fig. 5: D). Fig. 7 shows an AF-45 glass substrate from its backside after the laser ablation has been performed from the wafer front side. In Fig. 7a, the antenna patch-to-ground connection is realized as a rectangular slit of 100 x 3000 μm^2. In Fig. 7b, this connection is realized using an array of nine vias with diameter of 100 µm.

As the ablation time for this type of structures is proportional to the etched area, replacing the slit with an array of vias significantly shortens the ablation time.

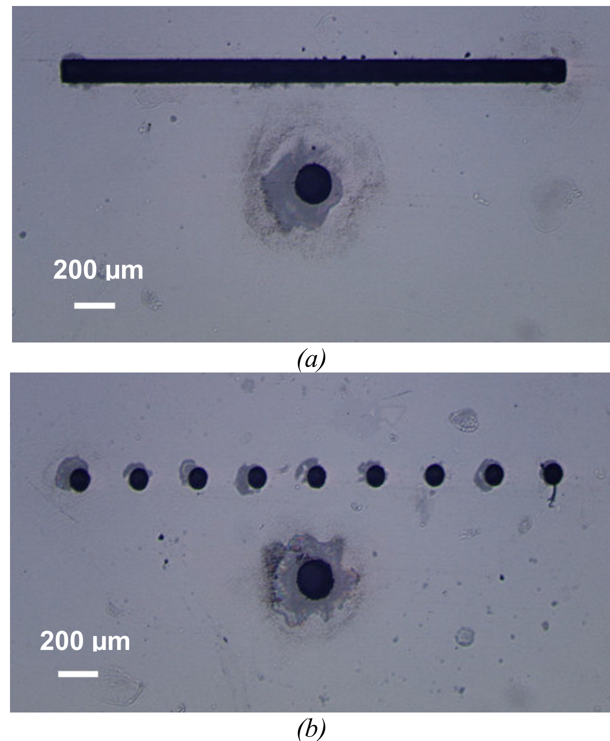


Figure 7: Microphotograph of a 500 µm thick AF-45 glass substrate with laser ablated through-wafer vias. The antenna patch-to-ground connection is realised using (a) a 100x3000 μm^2 slit; (b) an array of 9x100 µm vias. Note that the photos are taken from the wafer back side.

In case the glass substrate is replaced by HRS, the through-wafer via formation is performed using DRIE at cryogenic temperatures [7] and the overall processing becomes much easier.

IV. CONCLUSIONS

A folded-patch antenna was designed and critical electrical and fabrication parameters were analyzed.

Ansoft HFSS 3-D EM simulation tool was used to design folded-patch chip-size antennas for operation in 5-6 GHz frequency range. Different fabrication options, based on wafer-level chip-scale packaging techniques, and their influence on antenna electrical performance were analysed. The glass/glass combination was considered from the electrical as well as fabrication point of view. Fabrication of high-aspect-ratio vias (>5:1) in thick glass substrates (>300 µm) using excimer laser ablation was demonstrated. It is predicted that the glass/glass substrate combination would provide an antenna with the highest efficiency and still acceptable dimensions.

This work demonstrates that folded-patch antennas operating at 5-6 GHz are feasible for WLSCP integration on a RFIC chip for wireless short-range communications.

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