Wafer-Level Chip-Scale Packaging for Low-End RF Products

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***Abstract* — This paper gives a short overview of wafer-level chip-scale packaging technology and analyses its added value in the packaging of RF ICs. Particularly, the possibilities of substrate crosstalk suppression by substrate thinning and trenching together with embedding of rf passives (inductors, antennas) are addressed. The Shellcase-type wafer-level packaging solution is used as a study case presenting its fabrication aspects and its potential for RF IC packaging.**

***Index Terms* — Wafer-level packaging (WLP), chip-scale packaging (CSP), system-on-chip (SoC), embedded passives, crosstalk suppression.**

I. Introduction

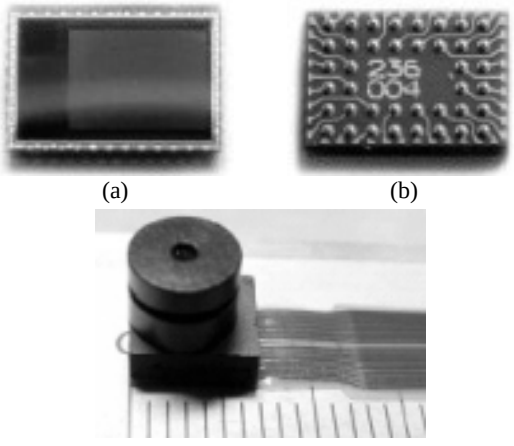
As the demand for ever-smaller electronic systems grows, manufacturers are seeking ways to increase IC integration levels and to reduce the size and weight of IC packages. The explosive expansion of mobile electronic terminals generates strong demand for high-performance, cost-effective and miniaturized RF modules providing desired wireless connectivity. Ideally, they should be realized as a single-chip solution and could easily be embedded into any electronic system. Such System-on-Chip (SoC) RF ICs have set a challenge for packaging, especially at the low-end market segment where low-cost solutions are required. The chip size package (CSP) and wafer-level packaging (WLP) resulting from this effort, have been introduced into manufacturing at an unprecedented rate.

The driving force behind is not only the reduced size and weight, but primarily the fact that the wafer-level chip-scale packaging (WLCSP) technology has potential of electrical performance improvement at a comparable or even reduced manufacturing cost and thus providing an improved performance-to-price ratio. Moreover, the same processing steps that are used to achieve the WLP technology basic packaging goal, can be adopted for implementation of an additional functionality at no or very limited additional cost. As an example, packaging of RF silicon ICs with simultaneous integration of high-quality passives, antennas or isolation structures [1] or protection of MEMS structures [2] can be mentioned. The emerging WLCSP technology and related integrated passive devices (IPDs) have proven to have capabilities of significant size reduction at a comparable cost and an improved electrical performance [3], [4].

In this paper, WLCSP technology is introduced and its capabilities and added value for packaging of RF ICs are analyzed. The Shellcase-type package as a commercially available solution is presented and its potential for RF IC packaging is explored.

II. Wafer-Level Chip-Scale Packaging

Wafer-level packaging is an IC packaging technology where most or all of the packaging process steps are carried out at the wafer level. The result of WLP is usually a chip size, surface-mount technology (SMT) compatible device i.e. device with area array solder bumps with pitch of 0.4-0.8 mm. As an example, Fig. 1 shows a VGA CMOS image sensor packaged using the Shellcase wafer-level packaging technology [5]. It is obvious that the achieved device miniaturization has opened new possibilities for its application in hand-held products.



(a) (b)

(c)

Fig. 1. A VGA CMOS image sensor packaged using Shellcase WLP technology: (a) front side; (b) back side; (c) device in a camera module with dimensions of 6x7x5.5 mm[3].

Fig. 2 shows schematically a typical WLP fabrication sequence used by Shellcase. The processed silicon IC wafer with bonding pad extensions into scribe lanes is adhesively bonded to a glass wafer. This glass substrate serves as a mechanical carrier allowing silicon substrate thinning down to 50-100 μm and trench forming beneath the pad extensions. Then a second glass substrate is adhesively bonded resulting in silicon islands fully encapsulated by the adhesive. A V-shaped dicing blade is subsequently used to perform notching within the scribe lane regions. The exposed pad extensions at each die periphery are then redistributed to the area array of solder balls on the bottom glass substrate. This is done by sputtering and patterning of an Al layer, followed by solder bump forming using solder paste deposition or attachment of pre-formed solder spheres. The process is completed by singulation into individual dies.

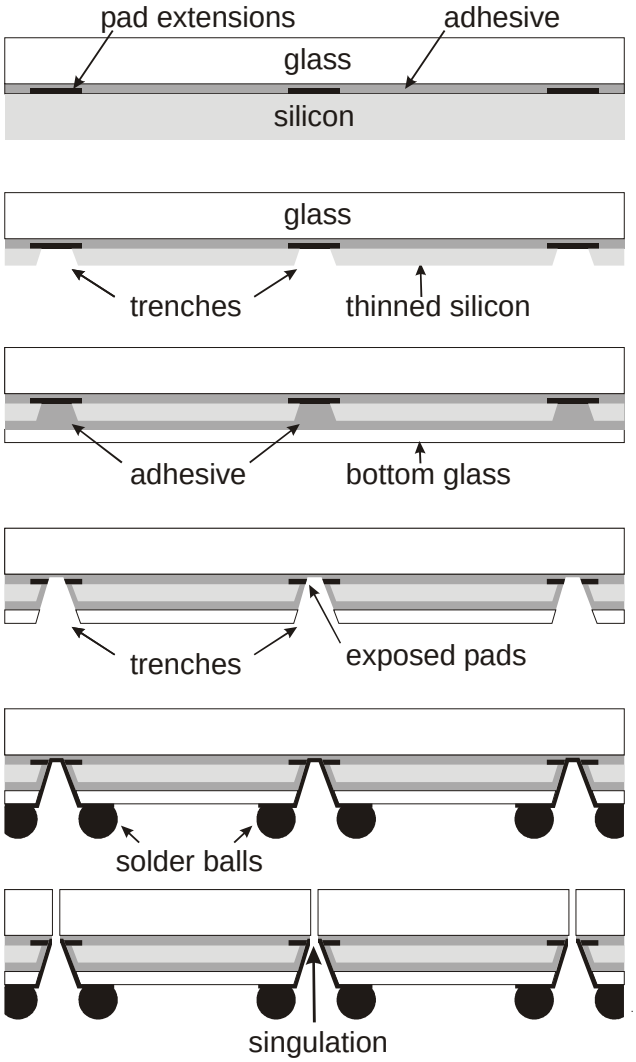


Fig. 2. Schematic WLCSP fabrication sequence used by Shellcase (for explanation see the text).

The principal goals of any wafer-level packaging process are: 1) environmental protection of the sensitive silicon die; 2) electrical signal redistribution from silicon dies to solder bumps; and 3) stress decoupling between solder bumpss and the silicon die. Depending on the method used to de-couple the mechanical stress between the packaged silicon die and the bumps soldered to the printed circuit board, following three major classes of WLCSPs can be distinguished:

- Interposer based WLCSPs – solder bumps are on a rigid interposer which de-couples the stress (e.g. ShellCase, Xicor, M-CSP);
- Compliant bump WLCSPs – each solder bump itself is compliant due to its special geometry (e.g. TI, Hitachi, Tessera, Form Factor, Shinko);
- WLCSPs with thin film redistribution and bumping – less effective stress de-coupling, but cheap (e.g. Fraunhofer Institute, Apack, Fujitsu, etc.).

The relatively large solder bump pitch used in WLPs enables simple handling and due to the mechanical stress de-coupling together with an increased solder bump height (>250 μm), it also avoids necessity of underfill. The current expectations predict main application of WLCSP in integrated passives, lower leadcount and memory ICs. The actual market penetration will be determined by packaging cost. As this is directly impacted by the number of dies per wafer together with wafer yield, small dies with a large die count per wafer are favorable for application of WLP.

III. Application of WLP for RF ICs

The same processing steps that are used to achieve the WLP technology basic packaging goal, can be adopted for implementation of an additional functionality at no or very limited additional cost. As an example, packaging of RF silicon ICs with simultaneous integration of high-quality passives, antennas or isolation structures can be mentioned (see Fig. 3).

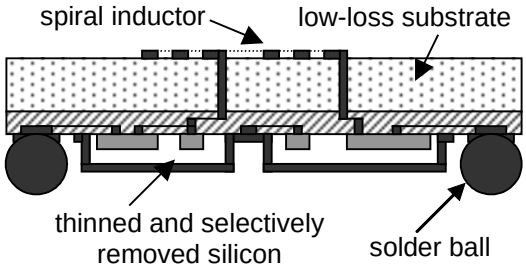


Fig. 3. Schematic view of a wafer-level chip-scale package based on adhesive bonding of a low-loss substrate to a Si RF IC wafer enabling implementation of rf enhancements e.g. through-substrate isolation trenches for crosstalk suppression, vertically-spaced passives, ground plane, low interconnect parasitics, etc.

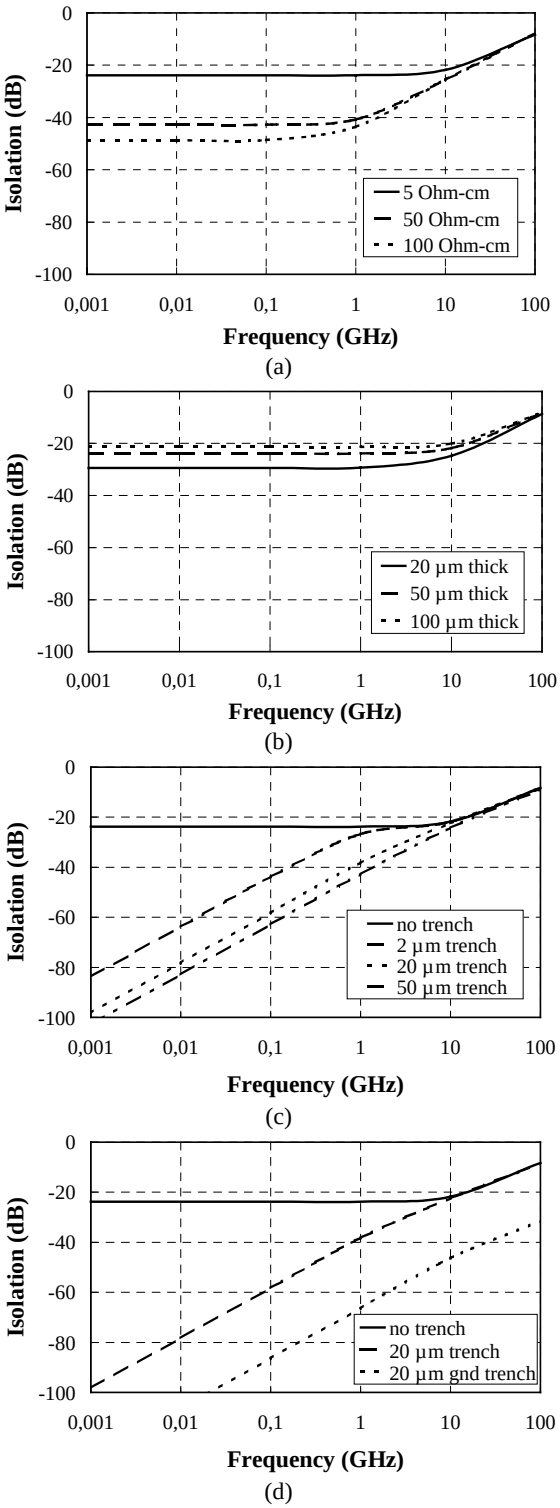


Fig. 4. Simulated isolation between two substrate contacts vs. frequency for: (a) different substrate resistivities; (b) different substrate thicknesses (no trench); (c) different trench widths; and (d) an isolation trench with and without grounded backside metallization. If not mentioned otherwise a 50 µm-thick, 5Ω-cm substrate is considered.

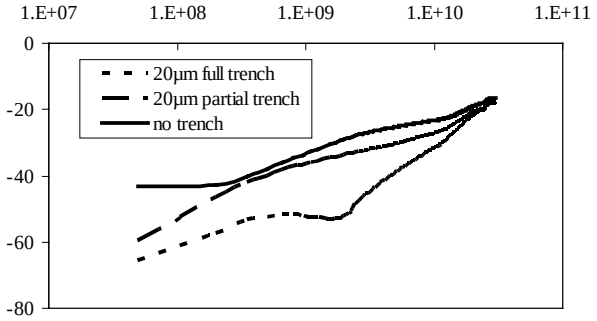


Fig. 5. Measured isolation vs. frequency between 2 substrate contacts showing influence of a partial and a full trench (contact separation is 100 µm).

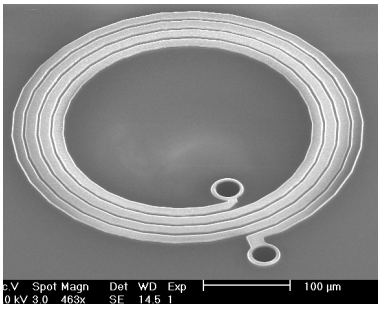
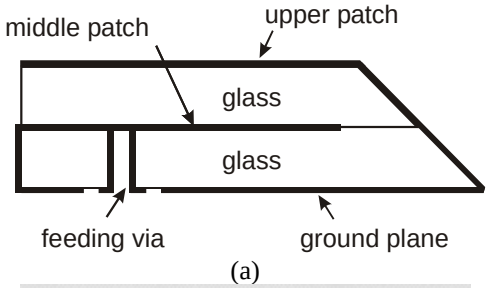
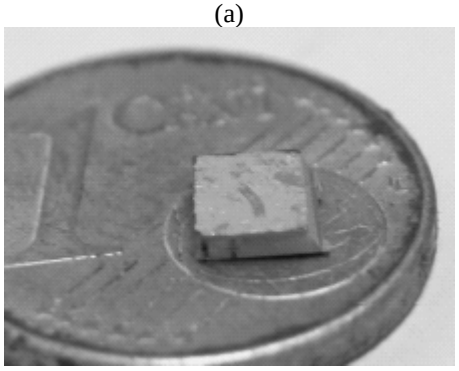


Fig. 6. SEM photographs of a spiral inductor on high-resistivity polysilicon (HRPS) with via connections through the substrate.



(a)



(b)

Fig. 7. A folded shorted-patch antenna for 5.6 GHz frequency range integrated on a stack of two glass substrates using WLP technology: (a) schematic cross section, (b) photograph of a functional prototype with dimensions of 4x4x1 mm^3.

Substrate thinning and trenching [6] have been explored theoretically and experimentally as techniques for

crosstalk suppression (see Fig. 4 and 5). Fig. 6 shows an example of spiral inductor embedding where a high-resistivity polysilicon substrate bonded to the Si RF wafer is used as a low-loss spacer and carrier for integrated passives [1]. Stacking of multiple wafers and through-substrate interconnect allow realization of more complex structures. Fig. 7 shows the prototype of a 5.6 GHz folded shorted-patch chip-size antenna (overall dimensions of 4x4x1 mm^3) realized using stack of two 500 µm thick glass wafers and 3D metallization.

IV. Shellcase Packaging Solution

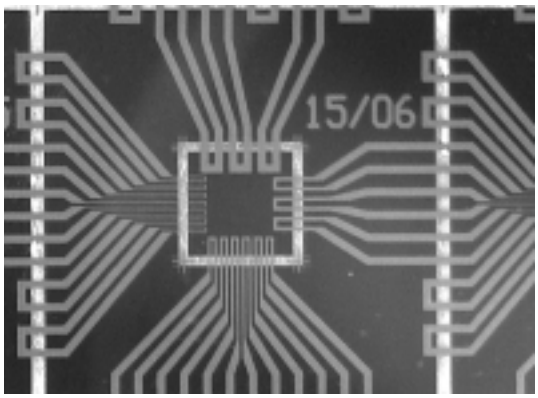


Fig. 8. Photograph of the test samples used in development of a dry etching process for silicon substrate partitioning after its adhesive bonding to a glass carrier.

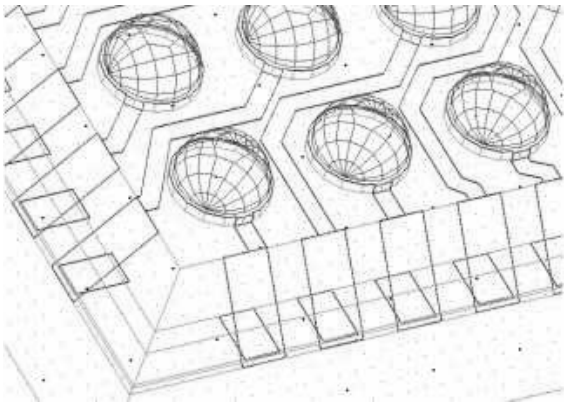


Fig. 9. A detail of a 3D model used to extract the package electrical interconnect parasitics.

As mentioned previously, the Shellcase WLP solution is based on sandwiching of a thinned silicon IC wafer between two glass plates using adhesive bonding and subsequent redistribution of the bond pads from die periphery to an area array of solder bumps. In the frame of the EU project Blue Whale [7], application of the Shellcase WLP technology for packaging of RF ICs is explored. The main issue addressed is the substrate crosstalk suppression by substrate thinning and partitioning by through-substrate trenches (see Fig. 8). This approach is easily extendable to selective substrate removal beneath e.g. integrated spiral inductors resulting in high-quality passives.

The thermo-mechanical and electrical analysis performed (see e.g. Fig. 9) indicates that this package-type with an low-loss glass carrier has reasonable heat dissipation capabilities and low electrical interconnect parasitics (L = 0.3-1 nH) and is highly suitable for low-power RF applications.

V. Conclusions

The recently introduced wafer-level packaging technology penetrates the markets at an unprecedented rate, due to its ability to provide cost effective solution for the limitations of conventional single-die packages. Application of WLP opens new possibilities for performance enhancements in RF packaging such as integration of high-quality passives (e.g. spiral inductors, antennas, transmission lines), substrate cross-talk suppression, low interconnect parasitics, etc.

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