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Small Size $\Sigma\Delta$ Analog to Digital Converter for X-rays imaging Aplications

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This report describes the analog to digital converter for an image sensor, implemented in a standard CMOS process. The image sensor, after coated with a scintillator material, can acquire x-rays images. Since it uses standard CMOS technology, the digital circuits of control and signal processing can be integrated into the same chip. The analog to digital convertion is based in a sigma delta approach, being implemented inside each pixel.

1 Sensor description

Figure 1 shows a block diagram of the image sensor with an analog to digital converter for each pixel. The sensor consists in an array of blocks, containing each one a photodiode and an analog to digital converter. The pixel blocks are addressed column by column by means of a shift register, and each pixel is connected to an output line, being all lines read at the same time by the output circuit. When the shift register is reset, its first output line goes to the high level. The other lines stay at the low level. In this case the digital outputs of the first column are read.

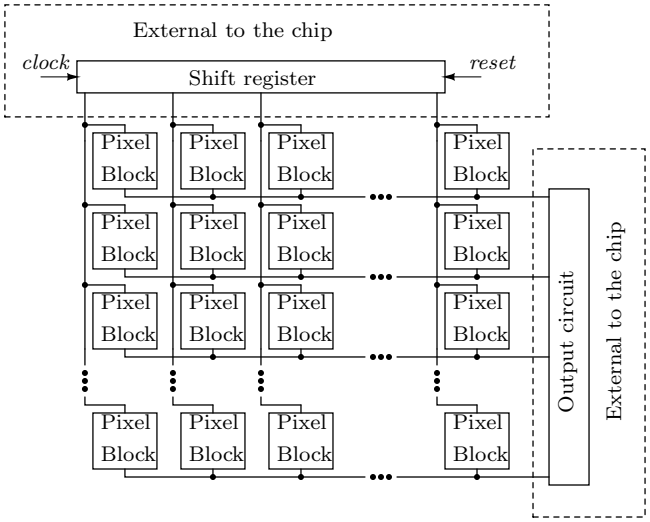

Figure 1: Block diagram of image sensor.

Each pixel block of figure 1 is shown with more detail in figure 2. At the

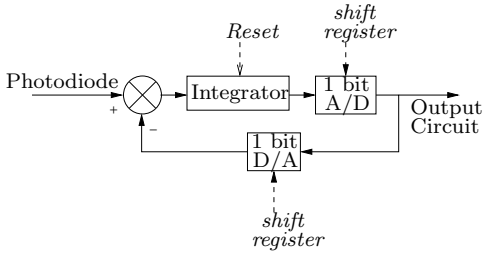

Figure 2: Block diagram for each pixel.

beginning all the integrators are reset in order to start at a known state. This procedure improves 3 dB in the signal to noise ratio [4].

After the radiation fall upon the scintillators, and an image be focused in the photodetectors, the sigma delta converters start the conversion. Their result is then read in all lines at the same time, column by column. The oversampling rate of sigma delta is established by the wished signal to noise ratio. It was concluded that the oversampling ratio (N), as a function of signal to noise ratio must be

$$N = 10^{\frac{20b \log 2 + 5.17}{30}} \tag{1}$$

As an example, in order to obtain a resolution of 8 bits, the signal to noise ratio must be at least 48.2 dB, requiring an oversample ratio greater than 60. For a resolution of 14 bits, the signal to noise ratio must be 84.3 dB, and it requires an oversampling ratio greater than 982. This high oversampling ratio may become a problem if the image sensor is very large.

The digital values coming from the sigma delta modulators are reconstructed through a decimation filter. This filter, depending on the type of application, may be implemented in software, using special purpose hardware external to the sensor, or integrated with the sensor. Decimation filtering is the process that converts high frequency sampled data to the Nyquist frequency, separating the signal from quantization noise, once the sigma delta modulator shifts the quantization noise to high fequencies. As the signal is in a band of interest between DC and half the Nyquist frequency, during decimation, a low pass filter is used in order to remove most of the quantization noise without affect the input signal.

2 Circuit description

The circuit consists of three sections: the integrator, the 1 bit analog to digital converter and the 1 bit digital to analog converter. The chosen photodetector is a photodiode constructed from a sp-substrate junction, in order to have a better response in the wavelengths of emission of the scintillator (560 nm).

2.1 Integrator

The integrator, based on a current mirror it is illustrated in figure 3. The

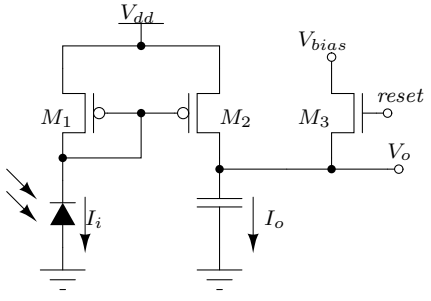

Figure 3: Schematic diagram of an integrator based in a current mirror.

photodiode current flows through M_1. As $V_{GS1} = V_{GS2}$, if the Mosfets are of the same size, ideally the same current flows through M_2, since it is working in the saturation region. The current in M_1 is given by

$$I_{D1} = I_i = \frac{\beta_1}{2} \left(V_{GS1} - V_T\right)^2, \tag{2}$$

and the output current, if it is assumed that M_2 is in saturation is

$$I_{D2} = I_o = \frac{\beta_2}{2} \left(V_{GS2} - V_T\right)^2. \tag{3}$$

As $V_{GS1} = V_{GS2}$, the relation between both currents is

$$\frac{I_{D2}}{I_{D1}} = \frac{\beta_2}{\beta_1} = \frac{W_2 L_1}{W_1 L_2}, \tag{4}$$

where

$$\beta = KP_p \frac{W}{L}. \tag{5}$$

KP_p is a SPICE parameter of the p-channel MosFet. Equation 4 shows that if the channel widths (W) and lengths (L) are adjusted properly, the desired output current is obtained.

The maximum output voltage is limited by the fact that M_2 must remain in saturation, therefore

$$Vo_{max} = V_{DD} - V_{DSsat} = V_{DD} - (V_{GS2} - V_T). \tag{6}$$

The output resistance of the current mirror is simply given by the resistance of M_2, so

$$r_o = \frac{1}{\lambda I_o}, \tag{7}$$

where λ is the LAMBDA SPICE parameter of M_2.

The small signal model of the integrator is shown in figure 4.

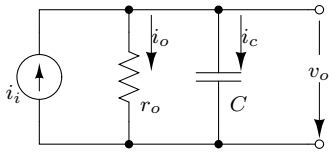

Figure 4: Small signal model of the integrator.

In this circuit, $i_i = i_c + i_o$, where $i_o = v_o/r_o$ and $i_c = C dv_o/dt$. After reduction,

$$\frac{dv_o}{dt} = Av_o + Bi_i, \tag{8}$$

where

$$A = -\frac{1}{r_o C} \quad \text{and} \quad B = \frac{1}{C}. \tag{9}$$

If this system is sampled with a sampling period h, it comes

$$v_o(h+1) = \Phi V_o(h) + \Gamma i_i(h), \tag{10}$$

where

$$\Phi = e^{Ah} \quad \text{and} \quad \Gamma = \frac{B}{A}\left(e^{Ah} - 1\right). \tag{11}$$

The transfer function is given by

$$H(z) = \frac{\Gamma z^{-1}}{1 - \Phi z^{-1}}, \tag{12}$$

and the DC gain is

$$H(1) = -\frac{B}{A} = r_o. \tag{13}$$

Equation 13 shows that the DC gain is large, so it is finite and higher than the oversampling ratio. In this conditions, the quantization noise in the signal band only increases 0.3 dB [2].

Also in this circuit, M_3 is used to reset the integrator, in order to the sigma delta modulator start at a known level. According to Netravali [4], there is about 3 dB improvement in signal to noise ratio by resetting the integrator at the beginning of each slow cycle, when uniform weights are used for the digital filters. Simulations shows that it is true even if the decimation is made with an optimum filter.

2.1.1 Integrator linearity

The behaviour of the integrator was simulated, for an input current of 100 nA, and Figure 5 shows the result.

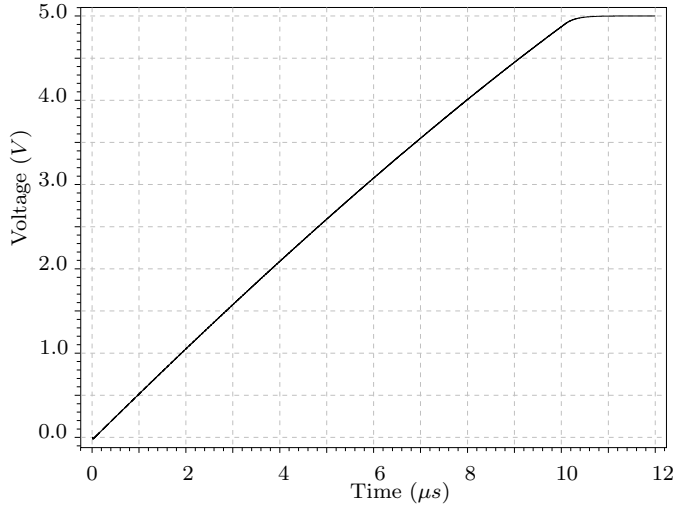

Figure 5: Time response of the integrator circuit, for an input current of 100 nA.

A detailed analysis to the curve of figure 5 indicates that the integrator is linear from 0 V to 4.8 V, and it shows up a Pearson product moment correlation coefficient of 0.999496, quite close to 1. This means that the integrator has a linearity close to ideal.

2.2 One bit analog to digital converter

Figure 6 shows the schematic diagram of the one bit analog to digital converter. MosFets M_2 and M_3 constitute a differential pair which amplifies the voltage difference between V_{in} and V_{bias}. The sign of this difference is stored in the latch constituted by M_5 and M_6, when the clock falls down. The latch state is maintained while M_4 is off. This happens when the clock is at down level. Figure 7

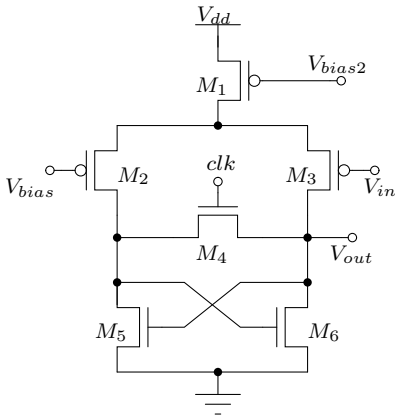

Figure 6: One bit analog to digital converter.

shows the output waveform of the circuit for a random V_{in}. The reference voltage (V_{bias}) is 2.5 V.

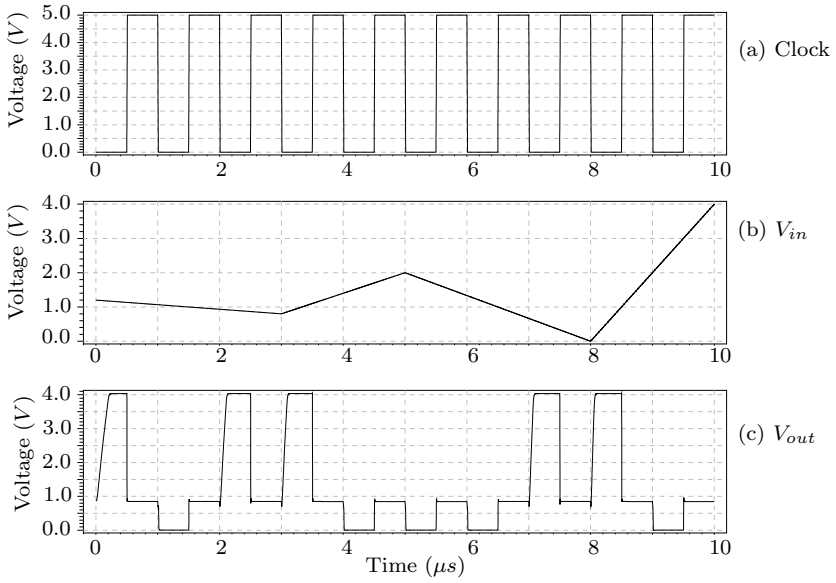

Figure 7: Waveform of the one bit analog to digital converter.

As is shown in figure 7, for each negative clock transition, the output voltage is at the high level if V_{in} is less than $V_{bias} = 2.5\ V$, and it is $0\ V$ if V_{in} is greater than V_{bias}. The clock signal comes from the shift register as it can be seen in figures 1 and 2

2.2.1 Time delay in the one bit analog to digital converter

A one bit analog to digital converter parameter that affects the global performance of the circuit is the time delay in the transitions to the high output level. This time delay can be estimated with the small signal simplified model of figure 8. First, suppose that the drain capacitance of Mosfet M_6 is equal to the

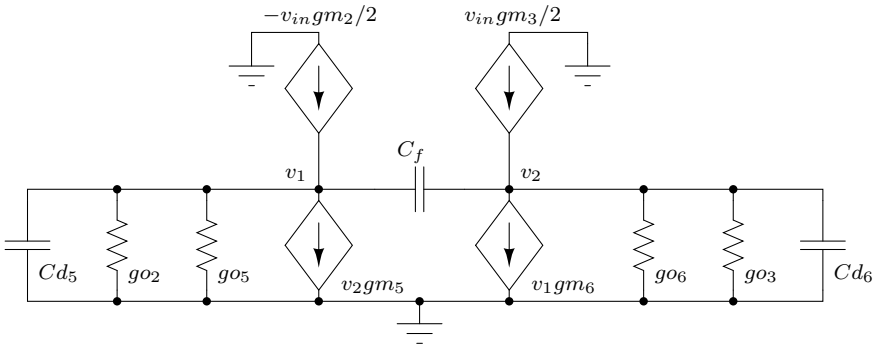

Figure 8: Small signal simplified model of the one bit analog to digital converter.

drain capacitance of M_5. This assumption is false, but if it is assumed that both capacitances are given by $c1 = \max(Cd_6, Cd_5)$, the analysis produces an upper bound to the latch velocity. Finally, assume that the voltage difference between the gates of M_2 and M_3 is ϵ. These assumptions give the following equations

$$v_1(go_5 + go_2) + (Cd_5 + C_f)\frac{dV_1}{dt} - C_f\frac{dv_2}{dt} - v_2gm_5 = \epsilon\frac{gm_2}{2} \tag{14}$$

and

$$v_2(go_6 + go_3) + (Cd_6 + C_f)\frac{dV_1}{dt} - C_f\frac{dv_1}{dt} - v_2gm_6 = \epsilon\frac{gm_3}{2}. \tag{15}$$

Suppose that $go_5 + go_2 = go_6 + go_3 = go$, $Cd_5 = Cd_6 = C_1$, $gm_5 = gm_6 = gm_n$ and $gm_2 = gm_3 = gm_p$, and $\delta v = v_2 - v_1$, then

$$\delta v(g_o - gm_n) + (c_1 + 2c_f)\frac{d\delta v}{dt} = -gm_p\epsilon \tag{16}$$

and

$$\delta v = \frac{gm_p\epsilon}{gm_n - go}e^{\frac{gm_n - go}{c_1 + 2c_f}t}. \tag{17}$$

Note that C_1 must be equal to the total capacitance seen by the drain of M_6. In order to produce a commutation to zero at the output, δv must change approximately 180 mV. This means that the gain of the amplifier must be greater than 30. The delay time of the latch is given by

$$t_l = -\frac{c_1 + 2c_f}{gm_n - go}\ln\left(\frac{0.2(gm_n - go)}{gm_p\epsilon}\right). \tag{18}$$

Note that if ϵ tends to zero, t_c tends to infinity. This is a common problem of metastability of the latches [3]. The graph diagram of figure 9 shows the waveform of the output voltage overlapped to the clock signal. The simulated time delay of the one bit analog to digital converter is about 15 ns, when the output signal goes to the high level.

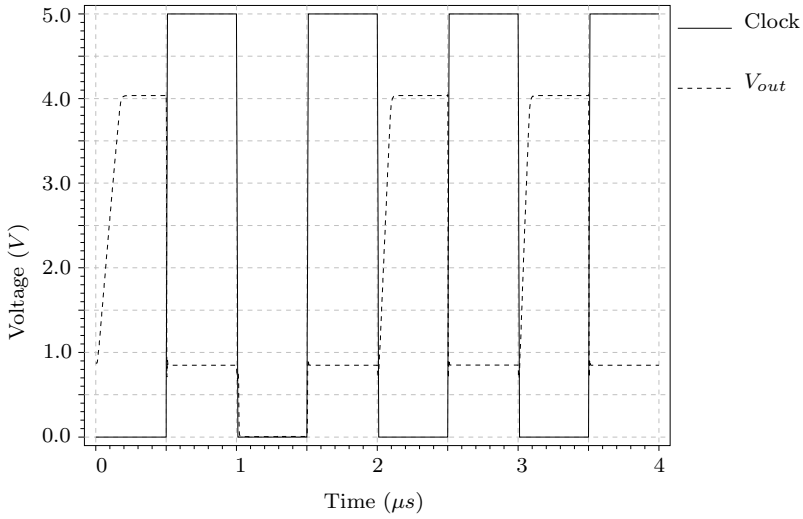

Figure 9: Time delay of the one bit analog to digital converter.

2.3 One bit digital to analog converter

The schematic diagram of the one bit digital to analog converter is shown in figure 10. This circuit is based on a current mirror controlled by the clock signal

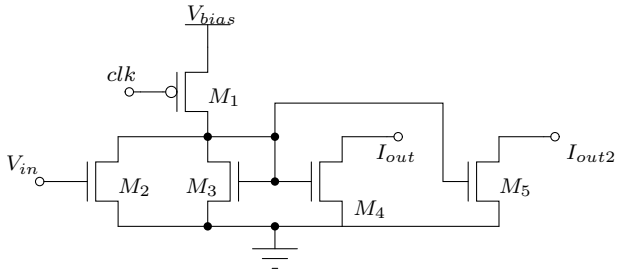

Figure 10: One bit digital to analog converter

and the output voltage of the one bit analog to digital converter (V_{in}). Once again, the clock signal comes from the shift register as it can be seen in figures 1 and 2 MosFet M_1 acts as a constant current source, whose value is determined by V_{bias}, when the clock is at the low level. MosFets M_3, M_4 and M_5 form a current mirror. When the clock and V_{in} signals are at the low level, M_1 is switched on and M_2 is switched off. A current appears at the drain of M_4. This current is equal to the one at the drain of M_1 in the case of the dimensions of M_3 and M_4 be identical. If the clock signal or the one at the output of the analog to digital converter (V_{in}) are at the high level, M_1 is switched off or M_2 is switched on. This produces a null current at the drain of M_3. The graphic of figure 11 shows the output current waveform of the circuit of figure 10. The output current I_{out} discharges the capacitor of the integrator and I_{out2} is connected to the output line of the circuit.

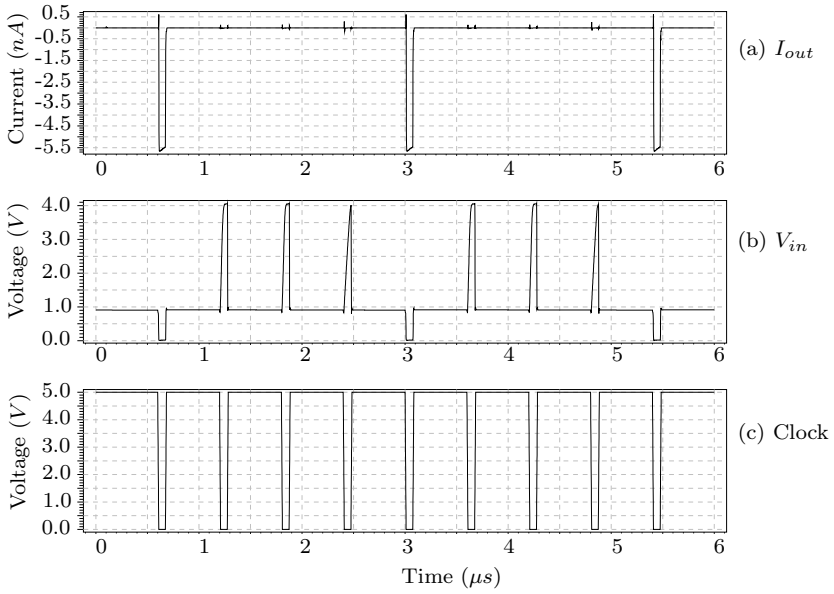

Figure 11: Input and output waveforms of the one bit digital to analog converter.

2.4 Closed loop analysis of the sigma delta converter

Figure 12 shows the waveforms of integrator output voltage (V_{int}) and 1 bit analog to digital converter output voltage (V_{out}).

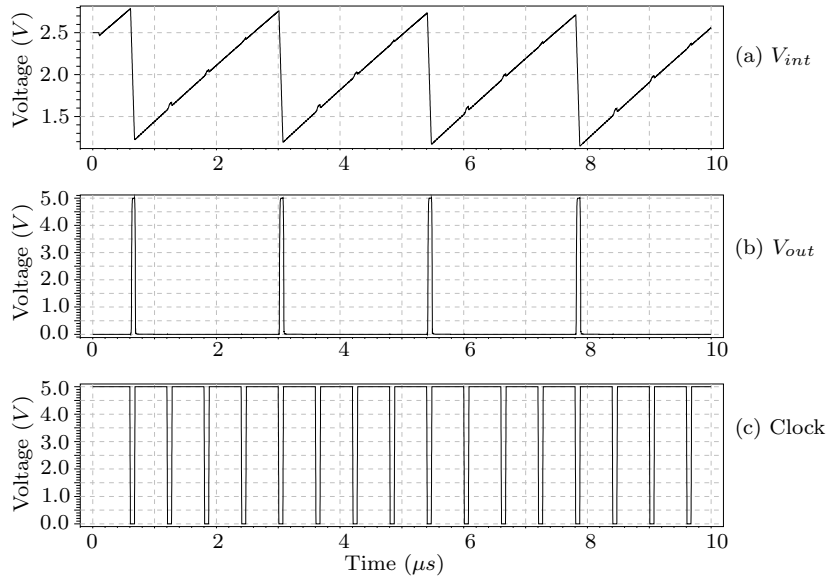

Figure 12: Input and output waveforms of the sigma delta converter.

Figure 13 shows the output value of the sigma delta converter for different input currents and an oversample ratio of 256. The response is linear with a Pearson product moment correlation coefficient of 0.99972. In order to obtain this graphic, a simple accumulate-and-dump digital filter was used. Its transfer function is given by

$$H(z) = \frac{1}{N} \sum_{i=0}^{N-1} z^{-i}, \tag{19}$$

where N is the integer ratio between the input frequency and the output frequency of the filter.

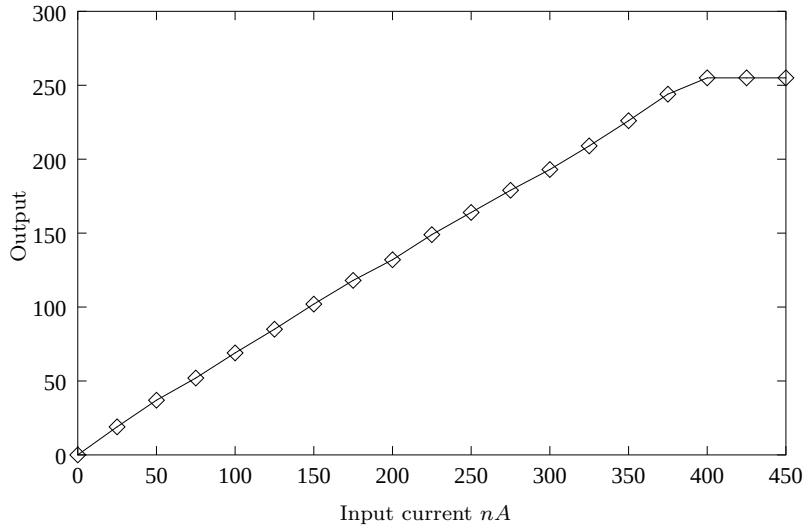

Figure 13: Binary output of the sigma delta converter

Figure 14 shows the spectral power of quantization noise. In order to obtain this graphic, 14 conversions are made for different input currents, with an oversample of 256. The 14 output bit streams were windowed by an Hanning window in order to calculate its fast Fourier transform. Then the average value was taken in order to draw the graphic. With a noise power of -60 db near the signal band-

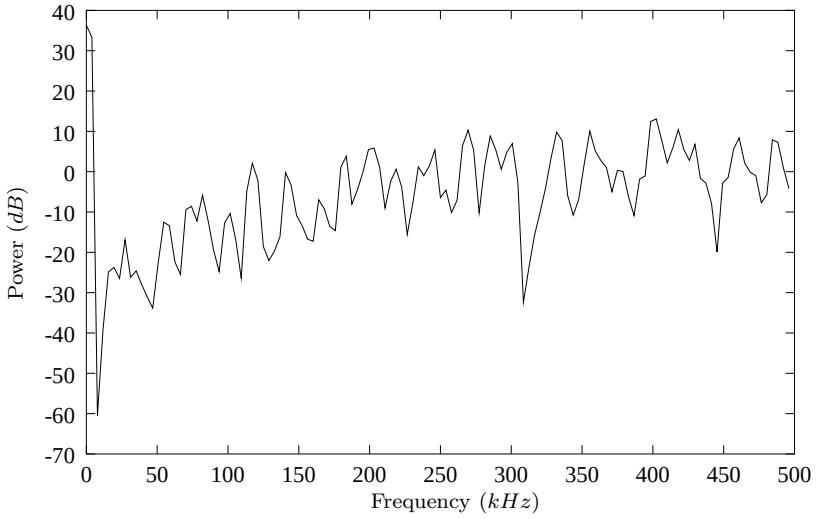

Figure 14: Spectral power distribution of the quantization noise of the sigma delta converter, with an oversampling rate of 256.

width, theoretically is possible to achieve an output resolution near 10 bits. In practice, and due to the non idealities of the decimation filter, the noise power in the signal bandwidth will be greater. But with a oversample ratio of 256 is quite easy to obtain 8 or 9 bits of output resolution.

3 Conclusion

The circuit presented at this report has only 14 small size MosFets and one capacitor. With it, an output resolution of 8 or 9 bits can be achieved with an oversample ratio of 256. After the analysis of the simulations, one can conclude that the pixel array of photodetectors with an analog to digital converter for each pixel is feasible.

References

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