A CMOS Optical Microspectrometer With Light-to-Frequency Converter, Bus Interface, and Stray-Light Compensation

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***Abstract*—A single-chip CMOS optical microspectrometer containing an array of 16 addressable Fabry–Perot (F–P) etalons (each one with different resonance cavity length), photodetectors, and circuits for readout, multiplexing, and driving a serial bus interface has been fabricated in a standard 1.6-μm CMOS technology (chip area 3.9×4.2 mm^2). The result is a chip that can operate using only four external connections (including V_{dd} and V_{ss}) covering the optical range of 380–500 nm with FWHM $=$ 18 nm. Frequency output and serial bus interface allow easy multisensor, multichip interfacing using a microcontroller or a personal computer. Also, stray-light compensation techniques are implemented. Power consumption is 1250 μW at a clock frequency of 1 MHz.**

***Index Terms*—Fabry–Perot etalon, internal/external bus interface, light-to-frequency converter, on-chip optical microspectrometer, visible light.**

I. Introduction

NUMEROUS applications, e.g., systems for chemical analysis by optical absorption and emission control of gas outlets, will benefit from the availability of low-cost single-chip spectrometers. Miniaturized spectrometers will offer significant advantages over existing instruments, including size reduction, low cost, fast data-acquisition, and high-reliability. Previously developed microspectrometers, fabricated using bulk or surface micromachining, contain movable parts to perform wavelength tuning [1], [2]. As the result, these are less reliable and suitable only for operation in a limited spectral band (mostly near-IR) [3], [4]. Moreover, high-voltage electrostatic actuation is necessary for resonance cavity tuning. Also, research on tunable vertical-cavity surface-emitting lasers (VCSEL) is promising a new generation of devices using III–IV compounds [5]. In this paper, a fully integrated array-type single-chip microspectrometer in CMOS technology with a light-frequency converter and a bus interface is presented. Although the focus of this paper is on the detector array with the Fabry–Perot (F–P) filter fabrication and on-chip integrated readout circuits, the optical aspects and a technique for stray-light compensation are also discussed.

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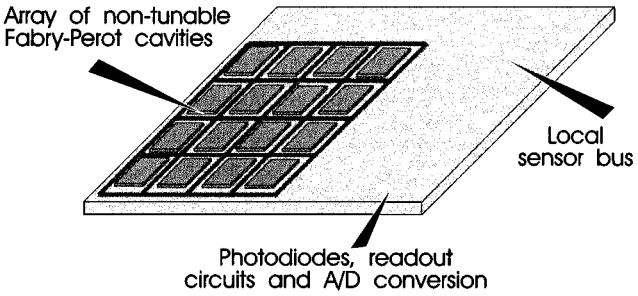

Fig. 1. Schematic diagram of a single-chip optical microsystem based on an array-type spectrometer of F–P etalons integrated with photodiodes underneath the 16 etalons, readout electronics, and the bus interface.

II. Single-Chip CMOS Microspectrometer

A. Array-Type Microspectrometer

The single-chip CMOS microspectrometer uses fixed-cavity F–P etalons with optical quality and long-term stability much higher than tunable devices [1], [2]. An array of detectors is needed to cover a large optical spectral range with high resolution. Therefore, the single-chip microspectrometer contains an array of 16 addressable F–P etalons with the respective photodetector underneath each of these (see Fig. 1).

B. Fabry–Perot Etalon

A F–P etalon (schematically shown in Fig. 2) consists of a vertically integrated structure composed of two mirrors separated by an air gap or a thin film. Such a structure is known in optics to cause interference between transmitted an internally reflected light, resulting in a spectral peaking of the transmission at particular wavelengths. The dependence of the transmission peaks on the gap width between the mirrors has resulted in the term "optical resonance cavity." In the device presented here both mirrors are at a fixed position, thus the optical properties are nontunable. In an earlier realization one of the mirrors was suspended using a micromachined structure and could be to deflected vertically using electrostatic actuation to enable wavelength tuning. The equation in Fig. 2 describes the F–P principle: d is the distance between the two mirrors; q is the resonance order; λ is the wavelength of the transmitted light; and n the refractive index of cavity medium (etalon of SiO_2). Successful operation of a tunable F–P device requires: parallelism of the mirrors, flatness and stability in the optically active region, and good optical properties (mirrors with high reflectivity

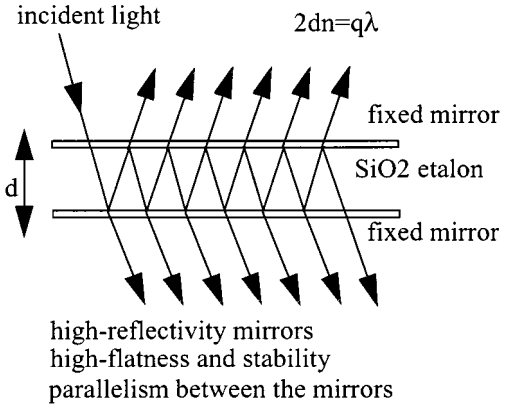

Fig. 2. F–P etalon description and requirements.

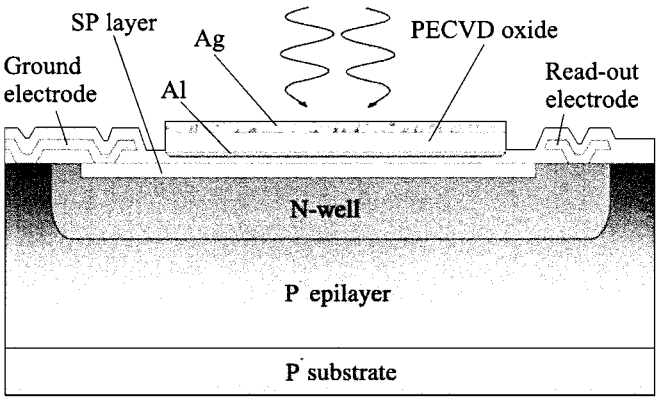

Fig. 3. CMOS F–P etalon with the photodiode underneath: a cross section.

and low absorption). These requirements are difficult to satisfy in a movable device.

CMOS post-processing consists of depositing an Al/SiO_2/Ag layer stack on top of each photodiode after the CMOS process has been completed (integrated-circuit fabrication). This stack functions as a tuned F–P resonance cavity. Compatibility with a CMOS process is required, also the photodiode should be fabricated in a CMOS process. Fig. 3 shows the F–P etalon structure plus the photodiode.

C. The Photodiodes

Each F–P etalon has an associated CMOS photodetector. The photodetectors have been realized in a conventional 1.6-μm n-well CMOS process. In an n-well CMOS process, three different types of photodiodes and one vertical phototransistor are available. The three different photodiodes result from the n-well/p-substrate junction, the n-well/p-diffusion, and the p-substrate/n-diffusion junction. The device used for photodetection is the vertical pnp phototransistor (Fig. 3), with the deep junction formed by the p-epilayer and the n-well, and the shallow junction formed by the n-well and a p+ implanted layer that is normally used for the drain/source contacts (sp). Both junctions are connected in parallel and operate at reverse bias. The upper junction contributes little to the generated photocurrent, especially at long wavelengths. Because of its large capacitance per area, this junction is mainly used for photocurrent integration. The sensors are arranged in a 4×4 array of square photodiodes with an active area of 500×500 μm^2 each. A typical dark current of 30 fA (12 pA/cm^2) was measured with both junctions reverse-biased at 5 V in parallel.

Crosstalk reduction techniques are implemented so that the operating current comes only from the photocarriers generated in or near the depletion layer between the p-diffusion/n-well junction. The utilization of the three-layer photodiode is an effective approach to improve photodiode performance.

D. Readout Electronics

The current-to-frequency conversion method can adequately cover the very large dynamic range of the silicon photodiodes. On-chip integration is essential to limit the influence of parasitic capacitances, leakage currents, and external noise pick-up and also provides properly matched components. Moreover, it enables the fabrication of array-type of detectors without a large number of external connections.

Low-noise read-out of photodiodes [6] has been implemented to cover a 10^5 dynamic range of light intensity level. The photocurrent-to-frequency circuits developed feature a dynamic range of sensitivity that is comparable to that of more complex analog circuits commercially available [7].

Fig. 4 shows the block diagram of the read-out circuit. Operation is based on a charge balancing technique, the voltage over the photodetector continuously varies from the reference level $V_{\rm dd}$ to the threshold voltage $V_{\rm th}$ of the comparator. The sensitivity of the current-to-frequency conversion is linear and can be calculated as $S_{\rm if} = f_{\rm o}/I_{\rm ph} = 1/(2\Delta {\rm Q})$. With ΔQ, the variation of the charge across the two junctions, depending on the junction capacitances of the photodiode. The total light-to-frequency conversion factor is given by the product of $S_{\rm if}$, the spectral responsivity of the photodiode and the transmittance of the F–P filter. This results in a current-to-frequency conversion factor of the circuit $S_{if} = f_o/I_{ph} = 1/2\Delta Q = 1.02 \times 10^5$ Hz/μA.

Only one photodiode can be connected to the comparator at a time using multiplexer S_1–$S_{\rm N}$. At a voltage $V_{\rm j}$ lower than $V_{\rm ref}$, the comparator output remains at a high logic level and, after synchronization with the clock, closes switch $S_{\rm ch}$, which forces the photodiodes to be quickly charged during one clock period to $V_{\rm dd}$. When this switch opens again, the photocurrent discharges the junction capacitance $C_{\rm jl}$ and $C_{\rm ju}$, until the comparator detects $V_{\rm j} < V_{\rm ref}$, which causes the cycle to repeat. The flip–flop chain divides the signal by two, resulting in a symmetrical output signal that can be transferred to the bus via a buffer.

Basically, the photodiode readout circuit can be considered a first-order (or relaxation) oscillator circuit and, since the circuit has only one pole (or frequency controlling element), it can be tuned over a very wide range [8]. The charge generated by the photoelectric effect directly modulates the charge in the integrating junction capacitance, thereby modulating the output frequency.

The charging switch $S_{\rm ch}$ is based on a complementary pair with equal-size PMOS and NMOS transistors to minimize capacitive charge injection at high oscillation frequencies. The currents in the multiplexer switches S_1–$S_{\rm N}$ are sufficiently low to allow a relatively high channel "on" resistance. The leakage current in the "off" state should be neglected compared to the

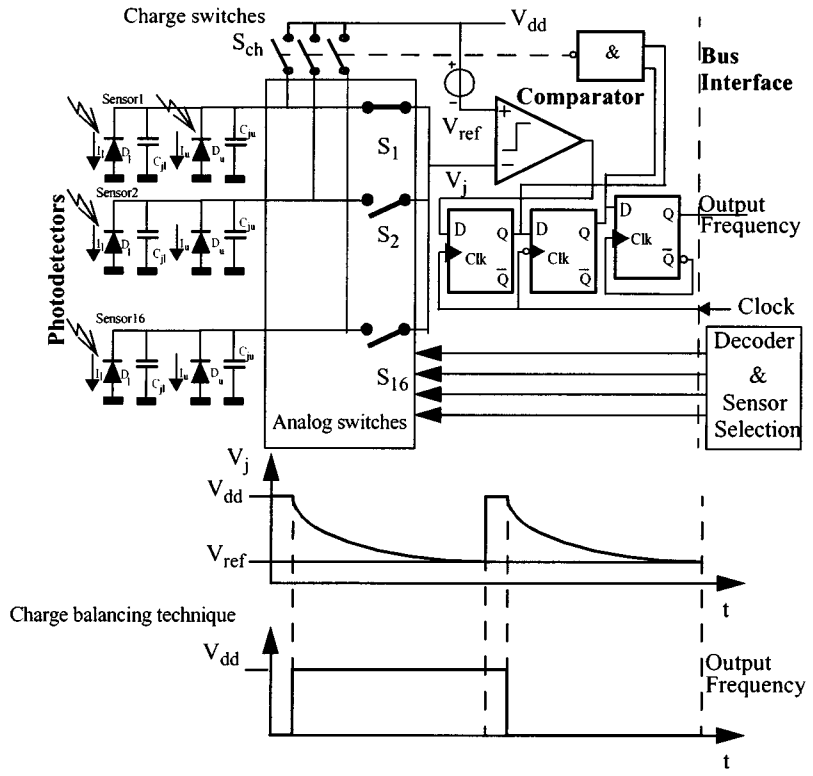

Fig. 4. Photodiode-readout circuits.

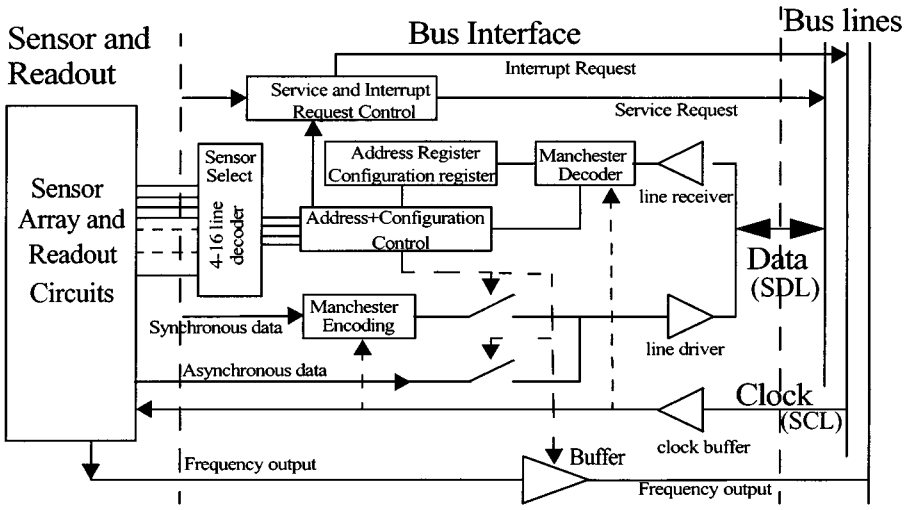

Fig. 5. Block diagram of the bus interface.

dark current of the diode. The channel of these MOS transistors has a W/L of 2 μm/16 μm. The input signals of the comparator can range from 1.3 V to the positive power supply rail V_{dd}. The bias current of the input stages makes it possible to set a speed/power consumption tradeoff. Table I summarizes the measured specifications of the comparator.

TABLE I
COMPARATOR SPECIFICATIONS

Input voltage range	1.3 – 5 V
Input offset (typical)	1.5 mV
Max. Frequency [MHz]	4
Propagation delay @ I_{bias} = 20 μA	100 ns
Propagation delay @ I_{bias} = 200 μA	60 ns
Power consumption @ I_{bias} = 20 μA	400 μW
Output rise and fall time	30 ns

E. Bus Interface

The upgraded version of the integrated smart sensor (ISS) bus interface [9] is based on a single controller to coordinate the activity on the bus and is characterized by the following:

1) a maskable interrupt mechanism;
2) calibration facilities;
3) small size;

4) low power consumption (which makes it very suitable for integration with optical sensors).

Apart from simplicity, the improved ISS bus interface has two convenient features, which makes it very suitable for an optical microsystem. First, analog data can be transferred over the bus. Data generated by a sensor with limited signal-processing capability are analog usually, so this requirement is necessary, but not present in the usual standard interfaces, which are designated to interconnect only digital subsystems. Second, the use of the Manchester encoding scheme for transmission of the data at the logical level adds further flexibility. In such a scheme, the clock is embedded into the data allowing four logical levels instead of two.

The physical structure consists of two wires: a data line and a clock line, both open drain driven. The data line allows half-duplex communication between the modules connected to the bus. In order to increase flexibility, we added a second data line to be used only in case of duplex transmission (e.g., in case of on-line sensor calibration or a testing procedure).

In case of the embedded systems, particularly for instrumentation systems, sensor modules should also be able to signal announce to the controller when data is available, or more generally, when some particular event has happened. In the realized interface, this flexibility is obtained by adding an interrupt request and a service request protocol.

An interrupt request message, if it is not disabled by the configuration used for that particular module, can be sent over the bus at any moment, even if the controller is in the middle of another conversation. A service request on the other hand, is allowed only if the bus is in the idle state. All messages excluding the request messages are initiated by the controller. The interface bus is composed of a number of synchronous blocks. Especially those that are pipelined have a significant portion of the total power dissipated by the clock (responsible for 50% of the total power dissipated) [10], [11]. Waste of power due to the clocking of blocks which are idle for a significant period of time in normal or standby modes must be avoided. To manage the power consumption, we implemented two modes:

1) Selective shut-down of different blocks based on the level of activity required to run a particular application. Different blocks of the chip may be idle for a certain period of time when different applications are running (this happens with the service and interrupt request blocks).
2) An idle mode for reducing power dissipation in the standby mode. Wake up is initiated only at the start of frame to enable verification of the address.

Fig. 5 shows the block diagram of the bus interface. A third bus line functions as the frequency output of the light-to-frequency converted signal (the simplest version of the bus interface uses only the clock line and data line). Also, the use of a different clock signal for the light-frequency conversion instead of the clock signal of the bus (SCL line) is allowed.

III. Device Fabrication

The electronic circuits and photodetectors were realized in a conventional double-metal, single-polysilicon 1.6-μm n-well CMOS process. After completion of the standard CMOS process, except for the last silicon nitride deposition step for scratch protection, a postprocessing module was used to build the F–P etalons on top of the photodetectors. This etalon consists of a thin-film stack (silver/PECVD oxide/aluminum). Fig. 6 presents a complete description of all CMOS postprocessing sequence steps.

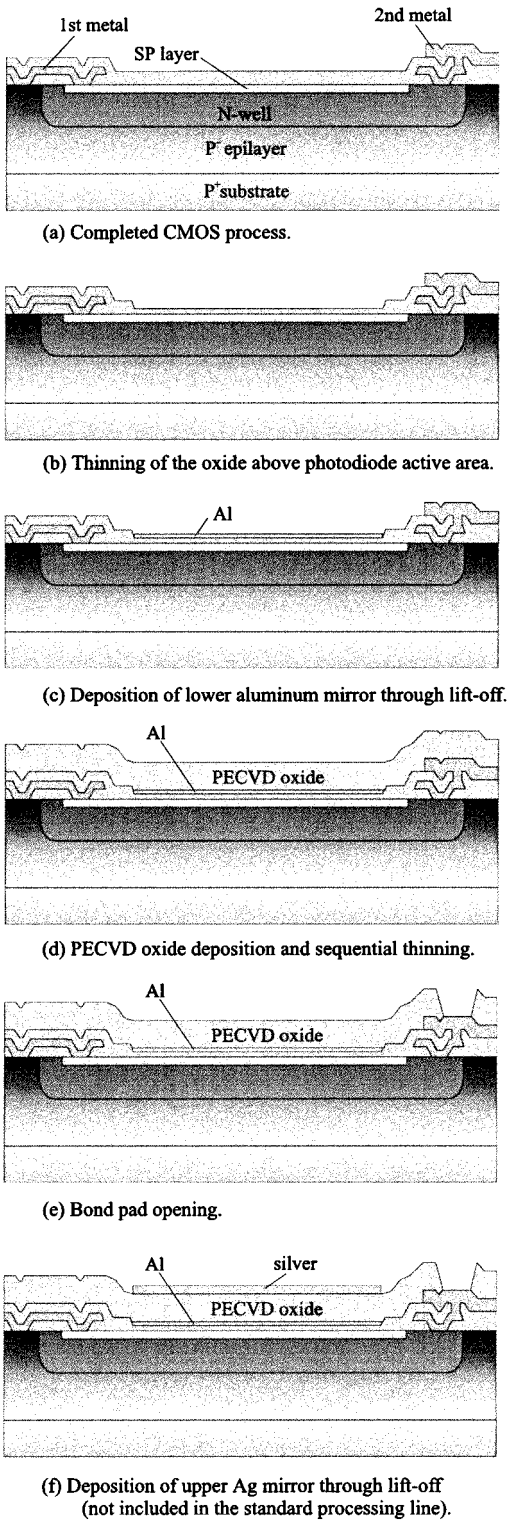

Fig. 6. CMOS post-processing fabrication sequence.

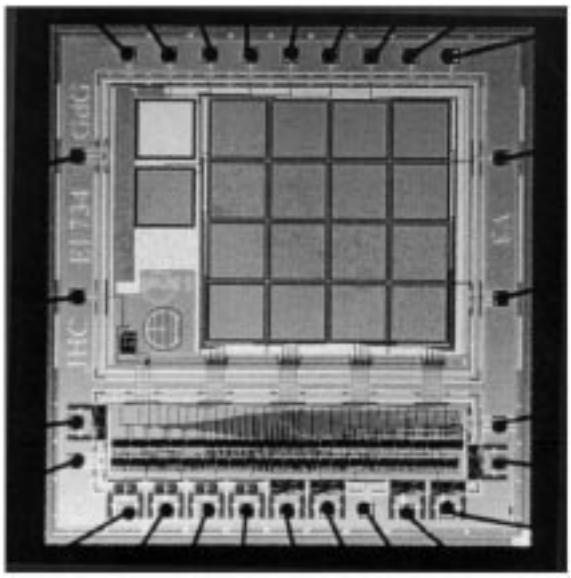

Fig. 7. Photograph of the single-chip CMOS optical microspectrometer.

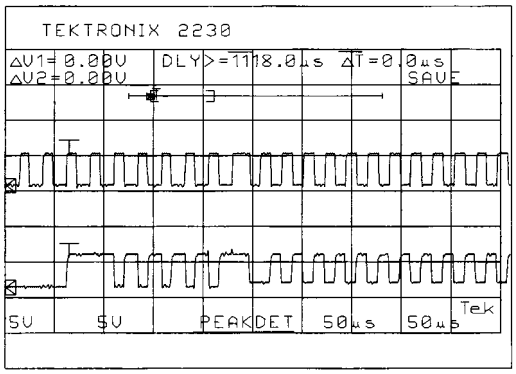

Fig. 8. Plot of clock and data lines from the oscilloscope.

The photodetector was formed in the n-well with the p-epi-layer by means of shallow boron implantation. Since the oxide layer on top of the photodiode is rather thick just after the CMOS process, this oxide layer was thinned to 50 nm to minimize the effect of the oxide layer on the transmittance.

The formation of the F–P etalon starts with the deposition of a 20-nm Al layer after completion of the CMOS process (including metallization and thinning of the oxide above the photodiodes). The oxide passivation layer on top of the photodetector (between the F–P etalon and Si substrate surface) is thinned to reduce its influence on the spectral response. The thin Al layer is evaporated and patterned using lift-off. Subsequently, a PECVD oxide layer is deposited with a thickness equal to the maximum cavity length. The thickness of the PECVD silicon dioxide layer, which is enclosed in between two semi-transparent metallic mirrors, determines the wavelength for tuning. In N subsequent plasma etching steps (for which different photoresist masks are used), the initially deposited PECVD oxide layer is thinned that 2^{N} channels are formed, each with a different resonance cavity length.

A microphotograph of the completed chip is shown in Fig. 7. The die measures $4.2\,\mathrm{mm} \times 3.9\,\mathrm{mm}$. The analog circuits can be seen in the upper part: a sensor array, analog switches, a stray-light compensation diode, a metal-covered diode (for dark-current compensation), a reference circuit, a reference capacitor, and a comparator. The lower part holds the bus interface, the multiplexer, and some other digital circuits. Only four external connections to the chip are strictly needed:

1) $V_{\mathrm{dd}}(+5\ \mathrm{V})$;
2) ground;
3) the clock input SCL;
4) and the bidirectional dataline (SDL) (since this line can also be used for transmission of the frequency output).

The other pads are the chip address pins and pins for testing purposes. The two grounds (analog ground and digital ground) and the two supplies (analog supply and digital supply) are separated on the layout design avoiding digital interference.

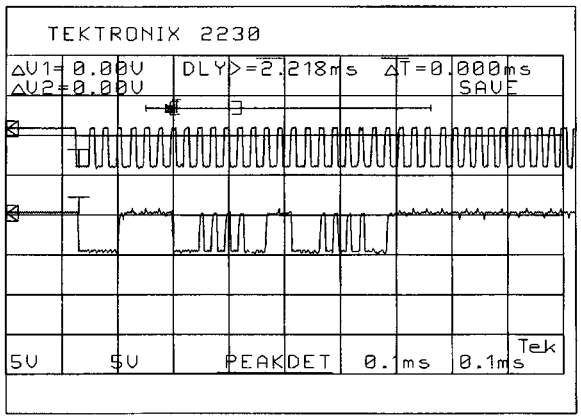

Fig. 9. Plot of service request proceeding.

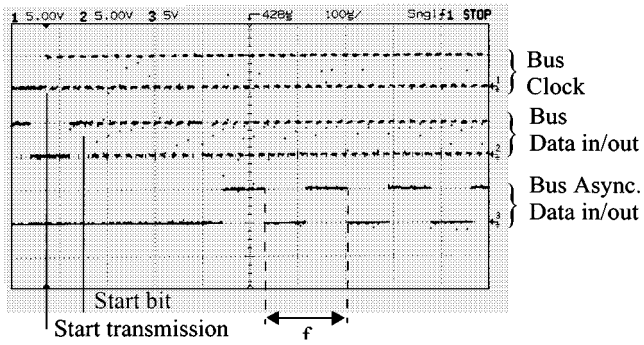

Fig. 10. Oscilloscope plot of the bus signals for a high light level.

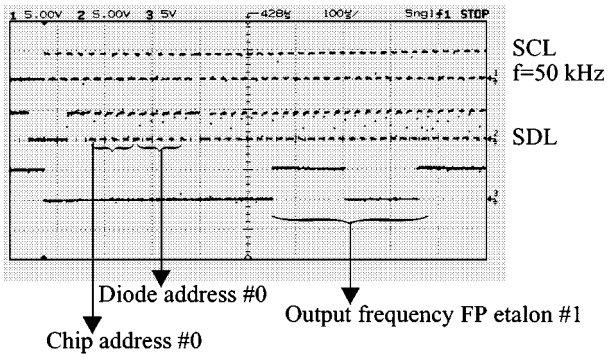

Fig. 11. Oscilloscope plot of the bus signals for a low light level.

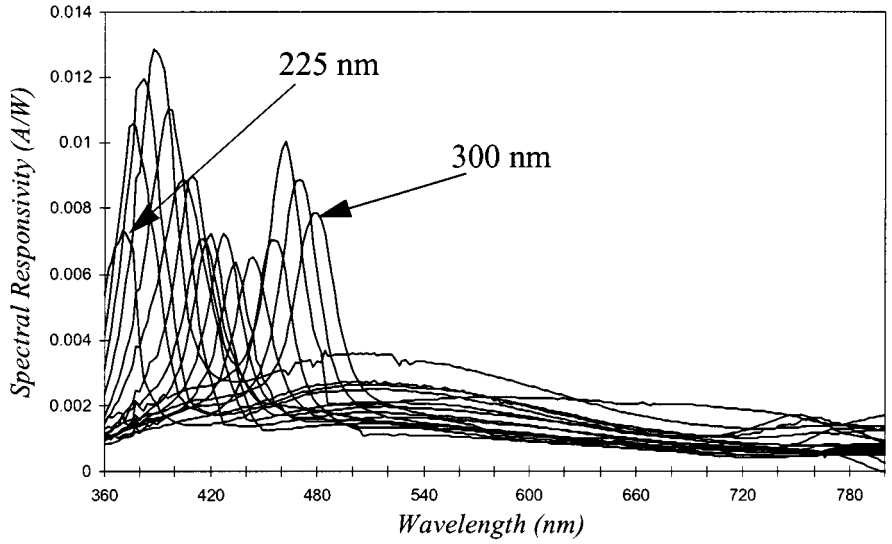

Fig. 12. Spectral responsivity of the 16-channel micro-spectrometer for a 45-nm Ag/SiO_2/20-nm Al layer stack. The SiO_2 layer thickness is used as a parameter and changes from 225 nm to 300 nm in 5-nm increments.

IV. Experimental Results

A. Single-Chip CMOS Microspectrometer

A particular etalon is addressed via an ISS bus interface by a conventional 8-bit microcontroller. A standard internal data-acquisition PC card can be also used for this purpose. A typical addressing sequence transmitted serially over the data bus has been recorded and is shown in Fig. 8. The frame transmitted was composed of a start bit, four bits for the device address and four more bits related to the internal sensor configuration. A network with three bus interfaces was implemented and the request block was successfully tested.

A typical service-request sequence transmitted serially over the data bus has been recorded and is shown in Fig. 9. When clock and data lines are idle, the sensor demands a service request by lowering the data line, and in reply the master issues a request for the address sensor.

The bus interface frames use eight bits for addressing. The four most significant bits are used for addressing the chip, so up to 16 chips can be addressed. The four least significant bits are used to select one of the 16 photodiodes. After selection, the corresponding sensor places its output frequency over the data asynchronous bus line. This sequence can be seen from the oscilloscope plots of Figs. 10 and 11.

The electrical characteristics and spectral responsivity were measured using an HP4142B dc source/monitor (full-scale range from 10^{-15} A to 1 A and a resolution of 10^{-13} A). A 100 W quartz tungsten halogen lamp with a monochromator TRIAX-180 (1200 g/mm grating with a spectral dispersion of 3.6 nm/mm and a spectral resolution of 0.3 nm at 546 nm), was used as light source. A collimator lens was used to image the light on the entrance slit. At the exit slit, a pinhole and a focusing lens were used to achieve a beam with a diameter of about 400 μm. The measurements were calibrated with a commercially available photodiode, Hamamatsu S1336-5BQ.

Fig. 12 presents the spectral responsivity (A/W) between 400 nm and 800 nm for all 16 channels using on-chip photodiodes. These results are somewhat different from what can be expected from Fig. 2 with PECVD oxide as the cacvity material ($n \approx 1.46$). These are basically due to the different metals used and the different thickness of the front and back mirror (45-nm silver at the frontside and 20-nm aluminum at the backside). The ratio between the base line value and the peak maximum ranges between 4 and 7. The relatively high stray-light, beam divergence, and the roughness surface are responsible for the background signal.

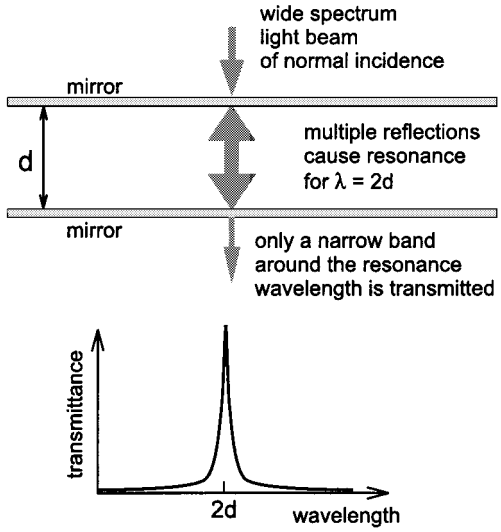

Fig. 13. Interaction of an ideal light beam with an ideal F–P optical filter.

B. Stray-Light Compensation Techniques

A method for significantly improving the performance of the F–P etalons in terms of spectral selectivity and/or requirements on the input light beam conditioning must be implemented. When an ideal plane-wave of normal incidence interacts with an ideal F–P resonance cavity, only a narrow spectral band around the resonance wavelength is transmitted (see Fig. 13). However, any imperfection of the incident light wave (components with nonnormal incidence, stray-light) and the F–P

TABLE II
SINGLE-CHIP OPTICAL MICROSPECTROMETER TEST RESULTS

	Condition	Test result
Operating voltage	--	5 V
Power dissipation @ 1MHz	Clk = 1 MHz	1250 μW
Power dissipation @ 100MHz	Clk = 100 MHz	700 μW
Max. clock frequency	--	6 MHz
Dark frequency	25°C	0.05 Hz
Free spectral range	--	380 – 500 nm
FWHM	--	18 nm
Responsivity (no FP etalon)	λ = 480 nm	0.18 A/W
Sensitivity (no FP etalon) [7] ref. TLS230 from Texas Instruments	λ = 670 nm	1.1 kHz/Wm^{-2}

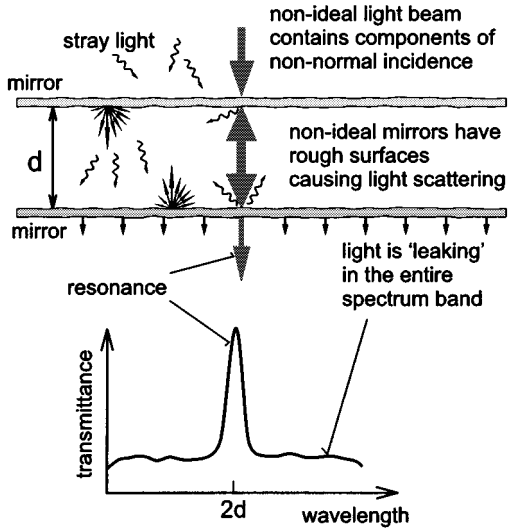

Fig. 14. Nonidealities of the incident light beam and the F–P structure itself causes a large background light level in the entire spectrum band.

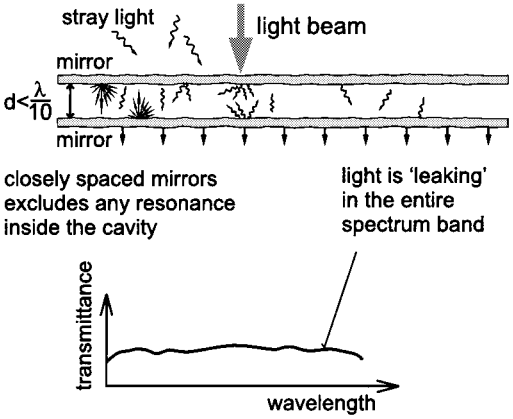

Fig. 15. Cross section of the compensation structure and its principle.

etalon itself (pinholes, scattering at the rough mirror surfaces), causes increased transmittance outside the narrow resonance band to which the F–P etalon is tuned, as is shown in Fig. 14. This results in an increased parasitic background signal.

A solution to this problem is to use a compensation structure, as shown in Fig. 15. It consists of the same layer stack as used in any of the active channels. The difference is that the optical length of the cavity is decreased below $\lambda/10$ (<40 nm if applied for measurements in the visible spectral range). This excludes

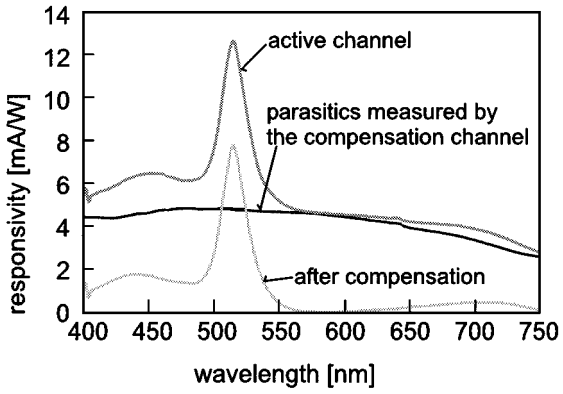

Fig. 16. Measured spectral response of both the active and compensating channel; when subtracted, the parasitic signal decreases by about a factor 10. In this method, no optics was required for the light beam conditioning.

any resonance inside the cavity. However, the parasitic signal caused by stray-light transmittance is similar to that of the active channel and can be used for compensation. Photodiodes are integrated underneath both the active and the compensating device and after subtraction of the photocurrents a compensated signal results. It should be mentioned that the conventionally used dark current compensation (an opaque layer deposited on top of a photodetector) compensates only for the nonidealities (dark current) of the detector itself. This method, in contrary, compensates for the nonidealities of detector, F–P filter and incident light beam at the same time.

If the impinging light beam has a uniform spatial distribution, one compensation channel for all active channels suffices. Fig. 16 shows the typical measured spectral response of both an active and a compensation channel. After photocurrent subtraction, the average background signal level is decreased by a factor of 10 and, as a consequence, the spectral selectivity of the device is increased [13]. When the overall contribution of the background component to the output signal (integral of the photocurrent over the entire measured spectral band) is considered, the significance of the method presented for application in on-chip spectrometers is even more obvious.

V. CONCLUSIONS

A single-chip CMOS optical microspectrometer containing an array of 16 addressable F–P etalons (each with a different resonance cavity length), photodetectors and circuits for

readout, multiplexing, and driving a serial bus interface was fabricated. The result is a chip that can operate using only five external connections (including $V_{\rm dd}$ and $V_{\rm ss}$) or in the simplest version with only four external connections (the data line will be also used for output frequency line) covering the optical visible range. The array-type microspectrometer can be glued on an active silicon platform using multi-chip-module (MCM) techniques. This configuration allow more than one microspectrometer glued on the platform (until 16, according to the four bits to address) increasing the spectral range. The advantage of the device presented is that it can easily be tuned during fabrication to cover different spectral bands, by adjusting the etching time only, without affecting the device layout. Stray-light compensation techniques improved the spectral selectivity of the F–P etalons. Power consumption is 1250 μW for a clock frequency of 1 MHz (see Table II).

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