A Single-Chip CMOS Optical Microspectrometer With Light-to-Frequency Converter and Bus Interface

José Higino Correia, Ger de Graaf, Marian Bartek, and Reinoud F. Wolffenbuttel

***Abstract*—A single-chip CMOS optical microspectrometer containing an array of 16 addressable Fabry–Perot etalons (each one with a different resonance cavity length), photodetectors, and circuits for readout, multiplexing, and driving a serial bus interface has been fabricated in a standard 1.6-μm CMOS technology (chip area 3.9 $\times$ 4.2 mm^2). The result is a chip that can operate using only four external connections (including V_{dd} and V_{ss}) covering the optical range of 380–500 nm with full-width half-maximum (FWHM) $=$ 18 nm. Frequency output and serial bus interface allow easy multisensor and multichip interfacing using a microcontroller or a personal computer. Power consumption is 1250 μW for a clock frequency of 1 MHz.**

***Index Terms*—Fabry–Perot etalon, internal/external bus interface, light-to-frequency converter, single optical microspectrometer, visible light.**

I. Introduction

NUMEROUS applications, e.g., systems for chemical analysis by optical absorption and emission control of gas outlets, will benefit from the availability of low-cost single-chip spectrometers. Miniaturized spectrometers will offer significant advantages over existing instruments, including size reduction, low cost, fast data acquisition, and high reliability. Previously developed microspectrometers, fabricated using bulk or surface micromachining, contain movable parts to perform wavelength tuning [1], [2]. As a result, these are less reliable and suitable only for operation in a limited spectral band (mostly, near-infrared) [1]. Moreover, high-voltage electrostatic actuation is necessary for resonance cavity tuning. In this paper, a fully integrated array-type single-chip microspectrometer with a light-frequency converter and a bus interface is presented.

II. Single-Chip CMOS Microspectrometer

A. Array-Type Microspectrometer

The single-chip CMOS microspectrometer uses $N \times N$ array fixed-cavity Fabry–Perot etalons with optical quality and long-term stability much higher than tunable devices [1], [2]. An array of detectors is needed to cover a large optical spectral range with high resolution. The single-chip microspectrometer in this paper contains a 4 $\times$ 4 array or 16 addressable Fabry–Perot etalons, each with a photodetector directly underneath.

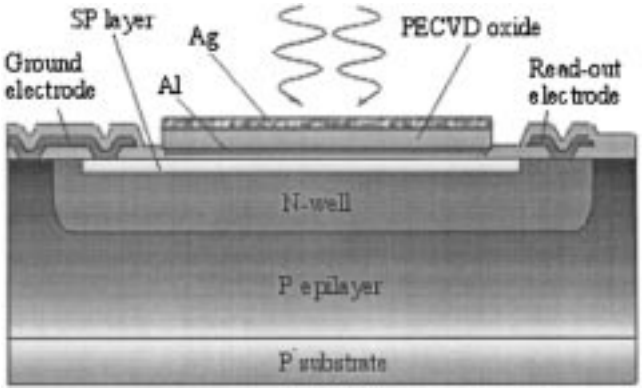

Fig. 1. CMOS Fabry–Perot etalon with the photodiode underneath. Cross section.

B. Fabry–Perot Etalon

CMOS postprocessing consists of depositing an Al–SiO_2–Ag layer on top of each photodiode after the CMOS process has been completed (integrated-circuit fabrication). This stack functions as a tuned Fabry–Perot resonance cavity. Compatibility with a CMOS process is required; also, the photodiode should be fabricated in a CMOS process. Fig. 1 shows the Fabry–Perot etalon structure plus the photodiode. Fig. 2 shows the photodiode readout circuits.

C. Bus Interface

The upgraded version of the integrated smart sensor (ISS) bus interface [3] is based on a single controller to coordinate the activity on the bus and is characterized by a maskable interrupt mechanism, calibration facilities, small size, and low power consumption, which makes it very suitable for integration with optical sensors.

Apart from simplicity, the improved ISS bus interface has two convenient features which make it very suitable for an optical microsystem. First, analog data can be transferred over the bus. Data generated by a sensor with limited signal-processing capability are usually analog, so this requirement is necessary, but is not present in the usual standard interfaces, which are designated to interconnect only digital subsystems. Second, the use of the Manchester encoding scheme for transmission of data at the logical level adds further flexibility. In such a scheme, the clock is embedded into the data, allowing four logical levels instead of two [see Fig. 3(a)].

The physical structure consists of two wires, a data line and a clock line, both open-drain driven. The data line allows half-duplex communication between the modules connected to the

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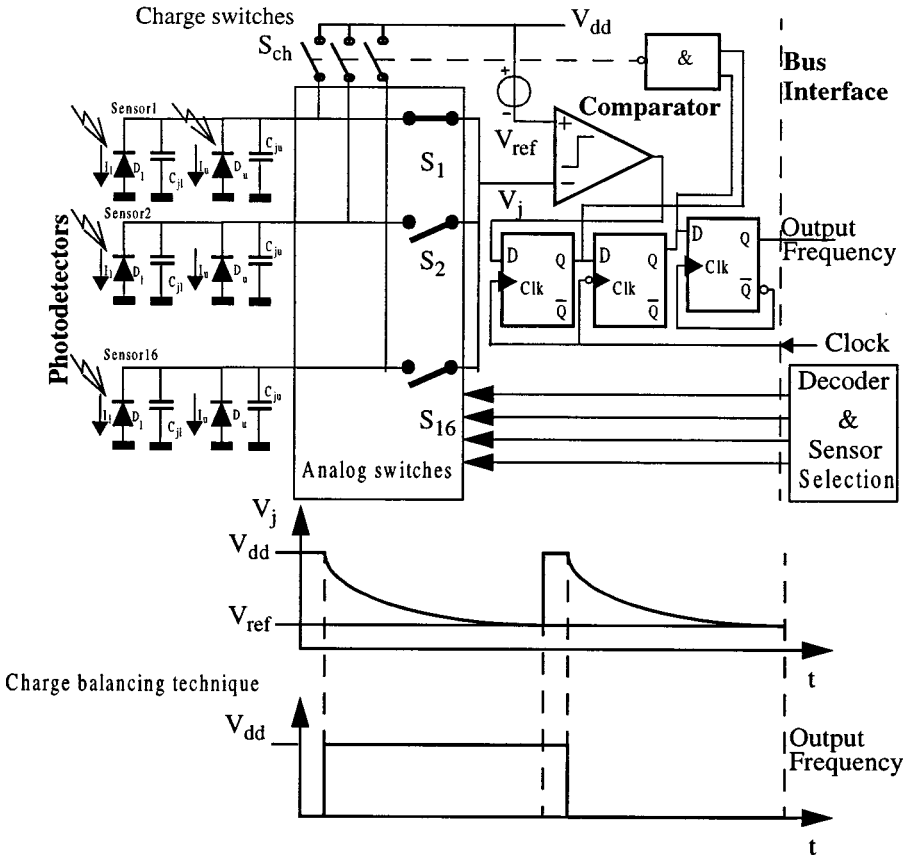

Fig. 2. Photodiode readout circuits.

bus. In order to increase flexibility, we added a second data line to be used only in case of duplex transmission (e.g., in the case of on-line sensor calibration or a testing procedure).

In the case of the embedded systems, particularly for instrumentation systems, sensor modules should also be able to signal announce to the controller when data is available, or more generally, when some particular event has happened. In the realized interface, this flexibility is obtained by adding an interrupt request and a service request protocol.

An interrupt request message, if it is not disabled by the configuration used for that particular module, can be sent over the bus at any moment, even if the controller is in the middle of another conversation. A service request on the other hand, is allowed only if the bus is in the idle state. All messages, excluding the request messages, are initiated by the controller.

The interface bus is composed of some synchronous blocks. Especially those that are pipelined have a significant portion of the total power dissipated by the clock (responsible for 50% of the total power dissipated). Waste of power due to the clocking of blocks which are idle for a significant period of time in normal or standby modes must be avoided. After the reception of the initial frame and the address validation is done, a flag is activated in the configuration control in order for the clock to be disconnected in the entry blocks. The only function that works in the reception mode all the time is the detection request block. To manage the power consumption, we implemented two modes.

1) Selective shutdown of different blocks based on the level of activity required to run a particular application. Different blocks of the chip may be idle for a certain period of time when different applications are running (this happens with the service and interrupt request blocks).
2) Idle mode for reducing power dissipation in the standby mode. Wakeup is initiated only at the start of frame to enable verification of the address.

The features of the bus interface are:

1) simplicity of structure;
2) only two communication wires used in the minimum configuration;
3) reliable data transfer by using the Manchester encoding with error-detection schemes;
4) flexibility of signal type, as synchronous and asynchronous transmission of digital data is possible in combination with semidigital signals, such as bitstreams, or even analog signals;
5) flexibility of signal handling based on a maskable interrupt mechanism;
6) sensor self-test capability over the bus using separate directional data lines, to be used as a separate die in microsystems and also suitable for on-chip integration with sensors;
7) smart power management for reducing power consumption [3].

Fig. 3(b) shows the block diagram of the bus interface. A third bus line is used to put the frequency output after the light-frequency conversion on the bus (the simplest version of the bus interface uses only the clock line and data line). Also, the

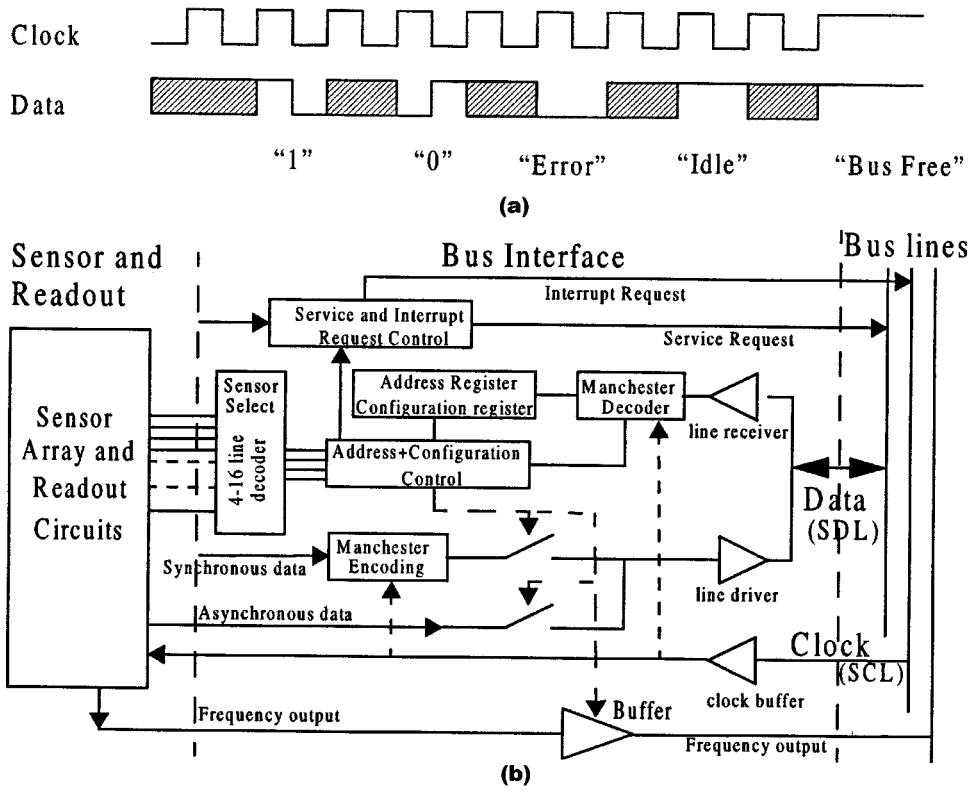

Fig. 3. Bus interface. (a) Manchester encoding scheme. (b) Block diagram of the bus interface.

use of a different clock signal for the light-frequency conversion instead of the clock signal of the bus (SCL line) is allowed.

III. Device Fabrication

The electronic circuits and photodetectors were realized in a conventional double-metal single-polysilicon 1.6-μm n-well CMOS process. After completion of the standard CMOS process, a postprocessing module was used to build the Fabry–Perot etalons on top of the photodetectors. Each etalon consists of a thin-film stack (Ag–PECVD SiO_2–Al). The Al serves as the etalon bottom mirror, the SiO_2 layer thickness is used as the gap-setting layer, and the Ag is the top mirror surface. Aluminum would be the most suitable in terms of CMOS fabrication compatibility, but, unfortunately, it has higher absorption losses than silver in the visible region.

The photodetector was formed in the n-well with the p-epi-layer by means of shallow boron implantation. The formation of the Fabry–Perot etalon starts with the deposition of a 20-nm Al layer after completion of the CMOS process. The thin Al layer is evaporated and patterned using liftoff. Subsequently, a PECVD oxide layer is deposited with a thickness equal to the maximum cavity length. The thickness of the PECVD silicon dioxide layer, which is enclosed between two semitransparent metallic mirrors, determines the wavelength for tuning. In N subsequent plasma-etching steps (for which different photoresist masks are used), the initially deposited PECVD oxide layer is thinned so that 2^N channels are formed, each with a different resonance cavity length. After the deposition of the silicon dioxide, each mask used has a different etching time $(T, T/2, T/4, T/8)$. For a 4×4 array-type microspectrometer, the first mask will etch one half of the whole thickness, the second will etch one fourth, etc. A microphotograph of the completed chip is shown in Fig. 4. The die measures 4.2 mm $\times$ 3.9 mm. The analog circuits can be seen in the upper part: a sensor array, analog switches, a test diode, a metal-covered diode (for dark-current compensation), a reference circuit, a reference capacitor, and a comparator. The lower part holds the bus interface, the multiplexer, and some other digital circuits. Only four external connections to the chip

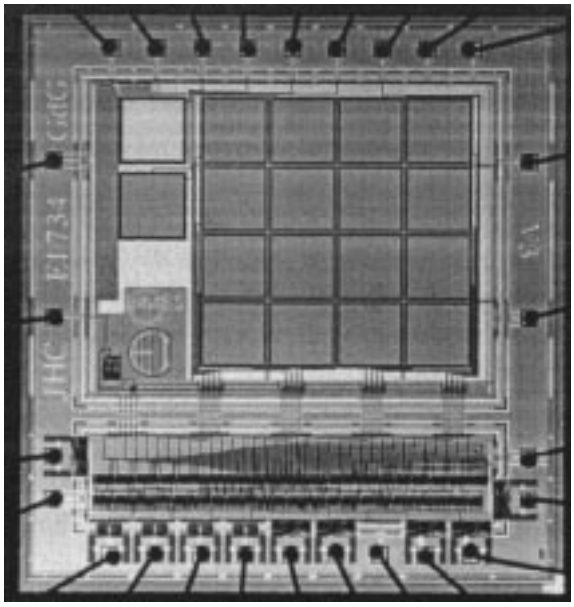

Fig. 4. Photograph of the single-chip CMOS optical microspectrometer.

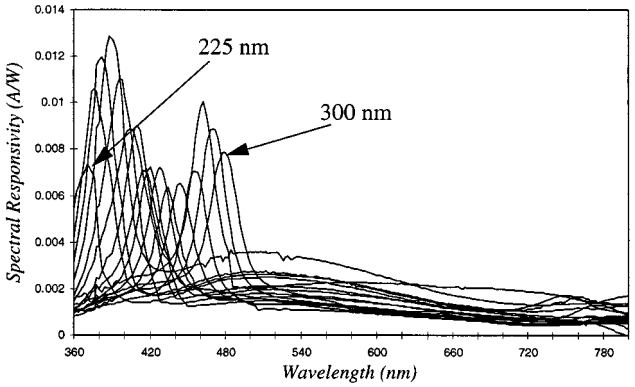

Fig. 5. Spectral responsivity of the 16-channel microspectrometer for a 45-nm Ag–SiO_2–20-nm-Al layer stack. The SiO_2 layer thickness is used as a parameter and changes from 225 to 300 nm in 5-nm increments.

are strictly needed: V_{dd} (+5 V), ground, the clock input SCL, and the bidirectional dataline (SDL), since this line can also be used for transmission of the frequency output. The other pads are the chip address pins and pins for testing purposes.

IV. Experimental Results

A device is addressed via an ISS bus interface by a conventional 8-b microcontroller. A standard internal data-acquisition PC card can also be used for this purpose. The frame is composed of a start bit and four more bits related to the internal sensor configuration (with four more bits, it is possible to address 16 microspectrometers). The bus interface frames use eight bits for addressing. The first four bits are used to select one of the 16 photodiodes. After selection, the corresponding photodiode places its output frequency over the data asynchronous bus line. Fig. 5 presents the spectral responsivity (A/W) between 380 and 500 nm for all 16 channels using on-chip photodiodes. The ratio between the base line and the peak maximum ranges from 4 to 7. The relatively high stray light, beam divergence, and roughness surface are responsible for the background signal. Stray-light compensation methods must be used in order to compensate for the nonidealities of both the incident light beam and the Fabry–Perot etalon. It consists of the same layer stack as used in any of the Fabry–Perot etalons. The difference is that the optical length of the cavity is decreased below $\lambda/10$ (<40 nm of SiO_2 if applied for measurements in the visible spectral range). This excludes any resonance inside the cavity. However, the parasitic signal caused by stray-light transmittance is similar to that of the Fabry–Perot etalon and can be used for compensation. Photodiodes are integrated underneath both the active and the compensating device, and after subtraction of the photocurrents, a compensated signal results. It should be mentioned that the conventionally used dark-current compensation (an opaque layer deposited on top of a photodetector) compensates only for the nonidealities (dark current) of the detector itself. The method used here, however, compensates for the nonidealities of the detector, Fabry–Perot etalons, and incident light beams at the same time. The rms roughness of the surface of both mirrors is approximately 6.4 nm.

V. Conclusion

A single-chip CMOS optical microspectrometer containing an array of 16 addressable Fabry–Perot etalons (each with a different resonance cavity length), photodetectors, and circuits for readout, multiplexing, and driving a serial bus interface was fabricated. The result is a chip that can operate using only five external connections (including V_{dd} and V_{ss}) covering the optical visible range. The array-type microspectrometer can be glued on an active silicon platform using multichip-module (MCM) techniques. This configuration allows more than one microspectrometer to be glued on the platform (up to 16, according to the four bits to address), increasing the spectral range. The advantage of the device presented is that it can easily be tuned during fabrication to cover different spectral bands, by adjusting the etching time only, without affecting the device layout. Power consumption is 1250 μW for a clock frequency of 1 MHz. The responsivity of the photodiodes for $\lambda = 480$ nm is 0.18 A/W with a sensitivity of 1.1 kHz/Wm^{-2} for $\lambda = 670$ nm.

Acknowledgment

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