A 195.6dBc/Hz Peak FoM P-N Class-B Oscillator with Transformer-Based Tail Filtering

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***Abstract*—A complementary p-n class-B oscillator with two magnetically coupled second harmonic tail resonators is presented. For the same oscillation amplitude (constrained by reliability considerations) and the same tank, the p-n oscillator achieves 3-4dB better Figure of Merit (FoM) than an n-only reference one. After frequency division by 2, the p-n oscillator has a measured phase noise that ranges from -150.8 to -151.5 dBc/Hz at 10MHz offset from the carrier when the frequency of oscillation is varied from 3.64 to 4.15GHz. With a power consumption of 6.3mW, a peak FoM of 195.6 dBc/Hz is achieved.**

I. Introduction

In LC oscillators reducing the power consumption while preserving their phase noise is a key goal especially for mobile applications. This can be achieved acting on the oscillator topology and/or on the tank quality factor (Q). Oscillator topology affects the conversion of circuit noise sources into phase noise changing the impulse sensitivity function (ISF) [1]. Moreover, it affects the power vs phase noise trade-off through the maximum achievable power conversion efficiency (η_P), i.e. the conversion of DC power (P_{DC}) into resonator RF power (P_{RF}), which directly affects the phase noise [2]. The use of voltage-biased topologies [3]–[5] eliminates a source of phase noise (i.e. the current generator) and improves power efficiency but increases frequency pushing. Large voltage swing (relative to the supply voltage) is desirable to achieve high power efficiency and to reduce phase sensitivity to device noise, as described by the ISF. However, as the active devices are driven by large signals, they can enter the triode region, thereby loading the tank, potentially degrading phase noise. This trade-off can be partially broken by adopting a low supply voltage, such that the active devices do not enter into triode even as the signal swing approaches (or exceeds) the supply rails. In practice, the use of a low supply voltage (e.g. 0.4V in [3]) makes the performances very sensitive to supply voltage variations and, when the oscillator is embedded in a complete transceiver, it necessitates a dedicated switch-mode voltage regulator to preserve power efficiency, thereby increasing cost. Other solutions include class-D oscillators [4], where the transistors are operated in deep triode to achieve good phase noise thanks to the low r_{ON} and the very fast switching, and clip-and-restore [5], where loading effects are compensated adopting step-up transformers to boost the gate voltage and reduce phase sensitivity to device noise. However, on-chip transformers typically have lower quality factors than simple inductors [6][1], moreover, in both cases a low supply is required for reliability. Higher order resonators have also been proposed (class-F oscillators [8]) in order to increase the maximum slope of the output signal for a given peak-to-peak voltage swing. However, an accurate analysis [2] reveals that this approach is beneficial only when the Q of the resonator is higher at $3f_{OSC}$ than at f_{OSC}, which is typically not the case. For a standard NMOS Class-B oscillator, if an additional LC tank (resonating at $2\omega_0$) is inserted at the source of the active devices [9], the switching transistors can enter the triode region without loading the tank since they see a high impedance in series with them. This allows to preserve the ISF while increasing power efficiency. High η_P and low phase noise however correspond to excessive voltage swings (ideally up to π times the supply voltage for 100% η_P). Adopting a complementary (push-pull) topology, the peak efficiency is reached at lower (theoretically half) voltage swing compared with an N-type-only one, avoiding reliability concerns. For this reason we present a high efficiency complementary Class-B oscillator with dual LC tail filter, which can use efficiently the supply current and achieve a low phase noise.

II. Excess Noise Factor in LC-Tank Oscillators

To benchmark the performance of an oscillator we rely on the widely used Figure of Merit (FoM) that normalizes phase noise to frequency of oscillation, offset frequency from the carrier and power consumption. Using the theory of Hajimiri and Lee [1] and assuming a nearly sinusoidal oscillation voltage, that the energy restoring element does not load the tank, 100% power efficiency, noiseless transistors and no other noise contribution, it can be shown that the FoM has a maximum called FoM_{MAX} that depends only on the Q of the tank as given below:

$$FoM_{MAX} = -10Log\left[\frac{kT}{2\cdot 10^{-3}\cdot Q^2}\right] \qquad (1)$$

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[1]This is only partially compensated by the fact that transformer-based resonators display a steeper phase response with respect to a simple LC-tank for the same quality factor [7].

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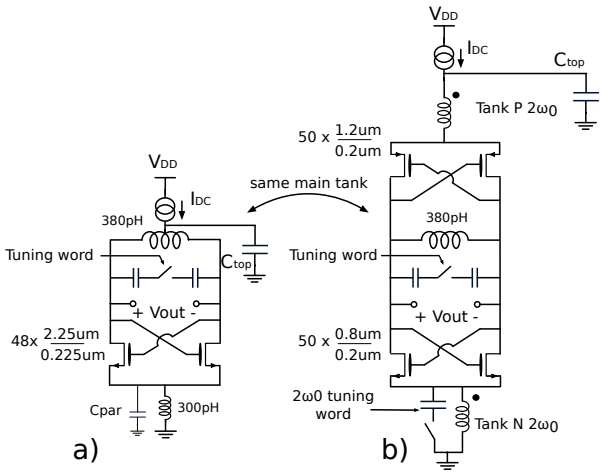

Fig. 1. Class-B oscillators with $2\omega_0$ LC tail filters: N-only and p-n

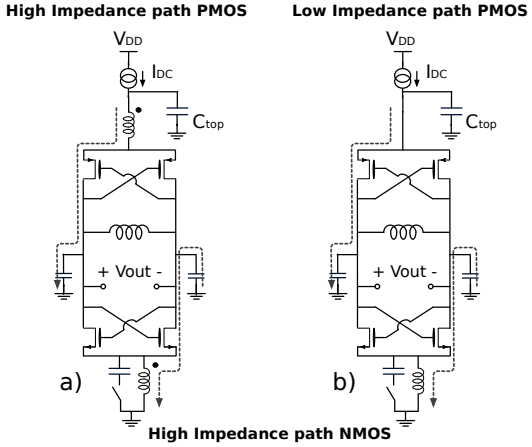

Fig. 2. Complementary p-n class-B oscillator with a) dual and b) single $2\omega_0$ LC tanks at the tails

FoM_{MAX} is a thermodynamic limit associated with the power dissipation of the unloaded tank. The Excess Noise Factor (ENF), defined [2] as the difference between FoM_{MAX} and the actual FoM, provides a figure of merit of the topology, independent from the tank Q. For a VCO with a direct coupling between tank and MOS gates, if the transistor current noise power spectral density is proportional to the derivative of the drain current with respect to the gate voltage and the active devices do not load the tank Mazzanti and Andreani [10] have shown that the transistors noise is γ_{MOS} times the tank noise, where γ_{MOS} is the excess noise of the MOS transistors. Using this result it can be shown that ENF is given by:

$$ENF = 10Log\left[\frac{(1+\gamma_{MOS})}{\eta_P}\right] \quad (2)$$

This shows that for all the topologies falling under the hypotheses above and for a given tank, the only diffrentiator is power efficiency.

III. Class-B with tail filter

Power efficiency is equal to the product of current efficiency (i.e. the ratio between the tank current at the fundamental frequency and the supply current), times voltage efficiency (i.e. the ratio between tank voltage and supply voltage). The key design goal of maximizing efficiency can be achieved acting on both current and voltage efficiencies. In class-C oscillators [10], [11], current efficiency is very high (up to 90%) but voltage efficiency need to be limited (to about 50%) to avoid loading the tank since the switching devices are connected to AC ground (resulting in a η_P between 45% and 55% [10], [11]). Standard class-B oscillators have lower current efficiency (ideally $2/\pi$) and voltage efficiency at maximum FoM similar to class-C (for the same reasons). The use of an additional LC tank at the source of the active devices (Fig. 1a) was originally proposed to reduce the current source noise [9] thanks to the filtering action of the large capacitance (C_{top}) in parallel with it. This topology has, however, two other important advantages. First, the common source node can swing below ground, increasing the maximum achievable voltage swing. Since current efficiency remains nearly constant, η_P is also increased, ultimately reaching a value close to 90%. Second, the switching transistors can enter the triode region without loading the tank since they see a high impedance in series with them. Hence, the peak efficiency corresponds also to the peak FoM because noise remains constant even when the switching transistors are pushed deeply into linear region, as opposed to what happens for class-C. Table I, reported in Section IV , compares the measured performance of various VCOs with different topologies, including their ENF (computed using the data available in the referenced papers). The comparison shows that the class-B oscillator with tail filter in [9] is superior by more than 1dB compared to any reported VCO (assuming accurate Q estimation). The main problem of this topology is the fact that for the optimum FoM the peak voltage across the transistors is more than twice the supply voltage, which may create reliability issues unless very high voltage devices or an extremely low supply are used. For the oscillator in [9], implemented in a $0.35\mu m$ CMOS technology and biased from 2.5V, the peak FoM of 195.4dBc/Hz is reached with a η_P of 81% for a peak swing of 6.4V (computed from the values of tank Q, inductor and current provided in the paper) which is almost twice the maximum allowed by the technology. This issue can be overcome using the complementary p-n topology shown in Fig. 1b, which, having twice the current efficiency of the N-only one, achieves the peak power efficiency (or equivalently reaches the peak FoM) with half the voltage swing. In [12] a p-n version of the oscillator of reference [9] was presented which achieved a FoM of 183.8 dBc/Hz and a ENF of 11dB. However, the focus of that work was to reduce the tail current noise at low frequencies ($1/f$), not to reduce ENF. The simplest way to implement a complementary oscillator with tail filter is shown in Fig. 2b. In this implementation the source of the PMOS transistors is connected directly to the current source and to the large capacitor C_{top}. However, since the tank cannot be made perfectly-differential, the PMOS transistors noise would see a

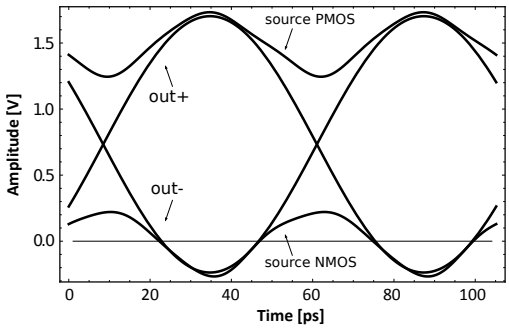

Fig. 3. Simulated voltage waveforms

low impedance path to ground, thereby loading the tanks and increasing phase noise at large amplitudes. This is confirmed by simulations, showing that at the higher end of the tuning range, when the common mode portion of the tank dominates, the PMOS transistors contribute more than 40% of the phase noise, while the NMOS contribute only 23%. An additional tail tank placed on the p-side of the VCO[2], as shown in Fig. 2a, prevents the PMOS transistors from loading the tank when they go into triode. As a result their phase noise contribution is reduced to 21% of the total, while the NMOS stays the same (at 23%) resulting in a 1.8dB phase noise improvement. Simulation shows (Fig. 3) that, thanks to the dual LC tail filter, the common source of NMOS and PMOS transistors can swing significantly above and below their DC voltage. This results in an oscillation amplitude (and consequently a power efficiency) 30% larger. Under these conditions the oscillator achieves, in simulation a maximum η_P of 85% and an ENF close to 4.2dB. To reduce area overhead, the tail inductances were magnetically coupled and laid out inside each other. The two coupled resonators have the same resonance frequency and can be tuned using a single capacitor bank. No attempt to control the second (higher frequency) resonance present in such a transformer was attempted [13].

IV. Oscillators Implementation

The difficulty to extract the tank Q, together with the high sensitivity of phase noise to Q, limits the ability to accurately assess the potential of a new topology. Because of this we have built a test chip that allows to compare the proposed topology with a reference oscillator, both working in the same operating conditions. The implemented chip prototype includes the class-B complementary p-n oscillator (with magnetically coupled tail filters), together with a class-B N-only oscillator with a single tail filter (used as reference) and was fabricated in a $55nm$ standard CMOS technology with only one ultra-thick metal layer. Circuit schematics are reported in Fig. 1. The oscillators use thick oxide devices (1.8V maximum voltage) and are biased from a 1.5V internal supply derived from the external 1.8 V supply through an on-chip band-gap referenced low-voltage-drop regulator. Both use identical tanks and can be tuned from about 7.4 GHz to 8.4 GHz (before frequency division by 2) with a 5 bits MOM capacitor bank. For the tail tanks the main design goal is to maximize its impedance at $2\omega_0$. This can be achieved using a high Q tank and/or a large inductor. A small inductor with high Q is preferable because it allows to use very large switching devices (with very low r_{ON} but large parasitic capacitance). This allows to improve power efficiency and gives about 1dB phase noise improvement (from simulations), although at the cost of an extra capacitor array for the tuning of the $2\omega_0$ tank. The coupled tanks (with inductance values of 180pH and 130pH and a coupling factor of 0.7) have a quality factor of about 10. A single 3-bit capacitor bank at the NMOS switching transistors source (controlled independently from the main tank) is used for tuning them. For the N-only oscillator the single tail tank has a quality factor of about 6 and uses an inductor of 300pH. A die photograph of the oscillators is shown in Fig. 4. Figure 5 shows the measured phase noise at the minimum and maximum frequencies for both oscillators. The $1/f^3$ noise corner is between 200kHz and 400kHz for the p-n oscillator and between 400kHz and 600kHz for the N only while the $1/f^2$ noise exceeds the 2G TX specification at 20MHz frequency offset by more than 7dB for the p-n oscillator and by 8 dB for the N-only, giving sufficient margin for other non-idealities. Fig. 6 shows the phase noise of both oscillators at the minimum frequency as a function of power consumption. The pn-oscillator has 0-1 dB lower phase noise of the N-only one with half the power consumption (i.e. the same output voltage for the same tank), hence the pn-oscillator has 3-4 dB higher FoM. The best achievable FoM is 195.6 dBc/Hz for the p-n oscillator and 192.3 dBc/Hz for the N-only, limited by reliability considerations, and it varies about 1.3 dB and 1.8 dB respectively across the tuning range (Fig. 7).

TABLE I
Comparison table

Ref	Topology	Tech	V_{DD} - $V_{0,pk}$ diff	f_{osc} [GHz]	FoM [dBc/Hz]	FoM_T [dBc/Hz]	ENF (Q)
[11]	class C PN	0.18um CMOS	1.8V 0.9V	6.1 - 7.5	189 - 191	196.4	5.8 (10)
[10]	Class C N-only	0.13um CMOS	1V 1.24V	4.5 - 5	193.5- 196	195.2	5.4 (17)
[9]	Class B N-only	0.35um CMOS	2.5V 6.4V	1.2	195.4	-	4.3 (14)
[4]	Class-D	65nm CMOS	0.4V 1.28V	2.5 - 3.3	189 - 190	198.4	6.8 (10)
[3]	Colpitts	0.13um CMOS	0.48V 1.5V	4.9	196.2	184.2	5.8 (18)
[8]	Class-F	65nm CMOS	1.2V 2V	5.9 - 7.6	192.2	200.2	8.7 (16)
This Work	Class B N-only	55nm CMOS	1.5V 2.1V	7.4 - 8.4	190.5 - 192.3	193.9	8 (15)
This Work	Class B PN	55nm CMOS	1.5V 1.6V	7.4 - 8.4	194.3 - 195.6	197.1	4.7 (15)

Table I compares the two prototype oscillators with the state of the art. With the exception of [3], the average FoM over the tuning range of the p-n oscillator is the highest reported. However the oscillator in [3] has an unpractical low supply and its FoM drops by 1dB for a 25mV supply voltage variation. For a further comparison the ENF was computed. The Q of

[2]A similar architecture was presented in [13] but not integrated in silicon.

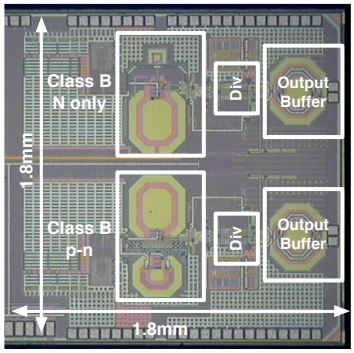

Fig. 4. Chip photo

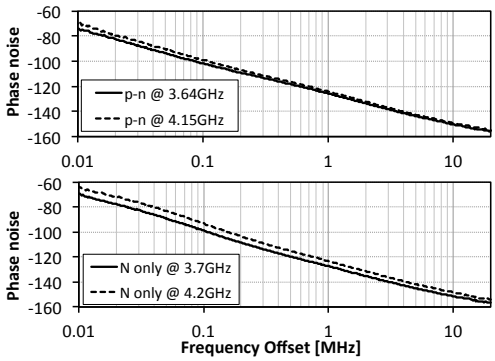

Fig. 5. Phase Noise measurements (after freq divider by 2) at the minimum and maximum frequency of oscillation

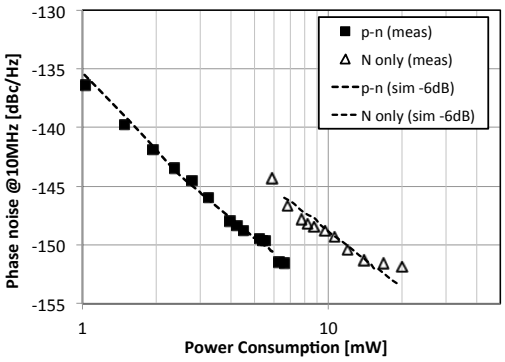

Fig. 6. Measured (dots) phase noise after freq. divider by 2 and simulated (lines) phase noise with 6dB reduction as a function of power dissipation of p-n and N only oscillators

the two prototype oscillators was estimated measuring both the minimum supply current needed to startup oscillations and the maximum absorbed current for a given supply voltage. Fitting the measured number with simulation gives in both cases an estimated Q between 14 and 15. With the exception of the N-only oscillator in [9] (that however far exceeds technology voltage limitations), the presented pn-oscillator has the lowest reported ENF. The p-n oscillator also has a high FoM_T of 197.1dBc/Hz , which is among the best of the high FoM and low ENF oscillators reported in the literature.

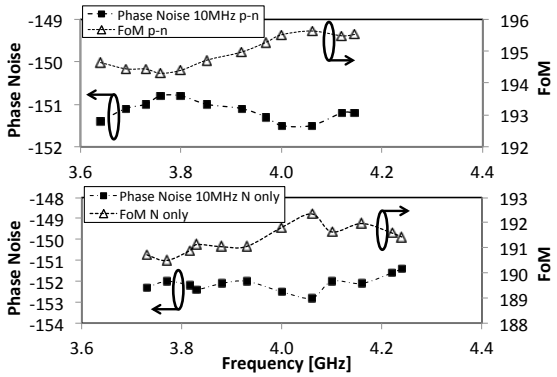

Fig. 7. Measured phase noise and FoM over tuning range of p-n and N only oscillators

V. Conclusion

We have proposed a complementary class-B oscillator with transformer based tail filtering that exhibits a high efficiency and has 3-4dB better FoM than a reference N-only oscillator, which is limited by reliability considerations. The fabricated 55nm CMOS oscillator displays one of the best ENF avoiding reliability concerns.

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