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A Novel Two-Switch Three-Level Active Rectifier for Grid-Connected Electrical Appliances in Smart Grids

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***Abstract*—A novel topology of two-switch three-level active rectifier (TSTL-AR) is proposed in order to connect electrical appliances to smart grids considering power quality aspects. The proposed active rectifier is presented as a powerful solution to mitigate the negative effects of current harmonic distortion of the diode-bridge rectifiers, besides the ability of operating with unitary power factor. These aspects are particularly relevant considering the new paradigm of smart grids, where almost all the electrical appliances should be controlled in order to comply normative impositions of power quality. In addition, active rectifiers are also fundamental devices regarding the electric vehicle battery chargers, which are a new and significant class of electrical appliances for smart grids. In this paper, a comprehensive and detailed description of the novel topology of TSTL-AR is presented and compared with the classical power factor correction topology. Along the paper, it is discussed in detailed a digital current control structure based on finite control set model predictive control, permitting an accurate, robust, and faster control of the grid current. A laboratory prototype was developed and experimental tests were performed, verifying the precise operation, and demonstrating the importance of the proposed active rectifier for electrical appliances in smart grids. The results show a low level of current THD, a unitary power factor, and a regulated dc-link voltage.**

Keywords—Active Rectifier; Three-Level; Two-Switch; Smart Grids; Power Quality; Predictive Control.

I. INTRODUCTION

Along the last decades, non-sinusoidal grid currents have been identified as a pertinent problem causing low-levels of power quality. This is more critical nowadays, since the new paradigm of smart grids requires high-levels of power quality for all the grid-connected electrical appliances. A detailed summary concerning the smart grid developments from the point of view of power quality is presented in [1]. In this context, also electric vehicle battery chargers should operate with high-levels of power quality independently of the novelty in terms of operation modes for the integration into smart grids. This is more relevant since EVs represent a new and significant class of electrical appliances for smart grids [2][3]. In [4] and [5] are presented innovative electric vehicle battery chargers, in terms of operational functionalities, and considering high-levels of power quality. An overview and an analysis of power quality for smart grids is presented in [6] and [7], respectively. As a main contribution to mitigate problems associated with power factor and harmonics of current, power factor correction (PFC) topologies that imposing sinusoidal grid currents are a pertinent substitute to diode and multi-pulse rectifiers [8][9]. Considering the different power levels of the grid-connected electrical appliances, many single-phase and three-phase topologies are being presented for a wide range of applications [10][11][12]. As example, the main single and three-phase PFC topologies are identified in [13] and [14], where the most relevant features of each one are explored as a comparison considering the interest for industrial applications.

The classical PFC topology is constituted by a diode full-bridge front-end converter and by a dc-dc boost-type back-end converter used to impose a controlled grid current with low total harmonic distortion (THD) and a controlled output voltage. An evaluation about PFC topologies based on the boost-type converter is presented in [15], where is also included an analysis for the evolution of this converter in terms of improved characteristics [15]. The PFC boost-type is a single-switch two-level topology with a single dc-link voltage. It is important to note that other dc-dc topologies can be applied for the same purpose, however, they have inferior results or more control complexity [16][17][18]. Besides the topologies based on the classical PFC topology, active rectifiers (in some cases also considering a bidirectional operation) are also emerging with an appropriated role to overcome power quality problems in smart grids.

Since the multi-level attribute is an important feature to distinguish PFC (and active rectifier) topologies, the most relevant multi-level PFC topologies (neutral-point-clamped converter, flying-capacitor converter, VIENNA-type converter, SWISS-type converter and cascade converter) are presented in [19], [20], [21], and [22]. Besides the multi-level attribute, PFC topologies can also be classified as interleaved (association of at least two PFCs in parallel) [23], as well as front-end bridgeless converters, i.e., without the full-bridge diode rectifier (differentiated as symmetrical and asymmetrical) [24][25]. A single-phase active rectifier, constituted by a single-switch based on the classical VIENNA rectifier is proposed in [26], where a divided dc-link represents the main disadvantage, since the dc-link voltage must be doubled when compared with the classical PFC. Single-switch PFC topologies are presented in [27] and [28], however, only allowing to establish a controllable power factor, where the high value of THD presented in the grid current is a negative effect for power quality in smart grids.

In this paper, a novel two-switch three-level active rectifier (TSTL-AR) is proposed for grid-connected electrical

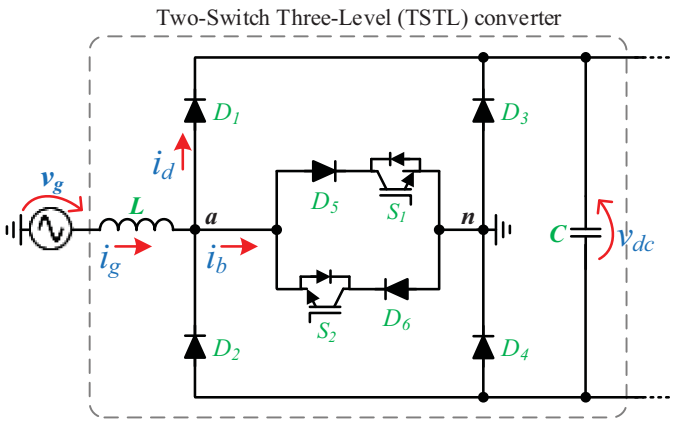

Fig. 1. Proposed single-phase two-switch three-level active rectifier (TSTL-AR) for grid-connected electrical appliances in smart grids.

appliances in smart grids. The circuity of the proposed TSTL-AR is presented in Fig. 1, where it is possible to identify its internal constitution. A classical full-bridge diode rectifier is used as an interface between the power grid and the dc-link. and a bidirectional and bipolar cell is used to establish the zero-voltage level of the converter during both positive and negative half-cycles. The indicated cell is constituted by two switches and two diodes. It noteworthy that the series connections formed by a switch and a diode are controlled independently, i.e., the top (s_1 and d_5) during the positive half-cycle and the bottom (s_2 and d_6) during the negative half-cycle. As shown, an inductive filter is used to couple the TSTL-AR to the power grid.

The control algorithm of the proposed TSTL-AR is described in section II. A comprehensive and extensive analysis, including the main simulation results, is presented in section III. An experimental validation of the proposed TSTL-AR, achieved with a developed laboratory prototype, is presented in section IV. Finally, section V summarizes the main conclusions of the work.

II. Control Algorithm

The structure of the control algorithm is divided into three fundamental parts, as shown in Fig. 2: (1) Establishment of the reference for the grid current (where is also included the control for the dc-link voltage); (2) Cost function for an optimized tracking between the grid current and its reference; (3) Finite control set model predictive control for the grid current control. The dc-link voltage is regulated using a proportional-integral (PI) controller. As the proposed TSTL-AR operates in single-phase systems, the dc-link voltage has a characteristic oscillation with the double of the power grid frequency. Using the measured dc-link voltage directly in the control algorithm results in a grid current reference with an oscillatory amplitude, and, consequently, the grid current will track its reference. Therefore, to avoid this phenomenon, the mean value of the dc-link voltage is used as an input for the PI controller (the reference for the dc-link voltage keeps constant), resulting in a constant signal as an output of the PI controller. This is valid for the steady-state operation, i.e., changing the operating power (DC load side), the amplitude of the oscillation in the dc-link voltage will also change, changing the

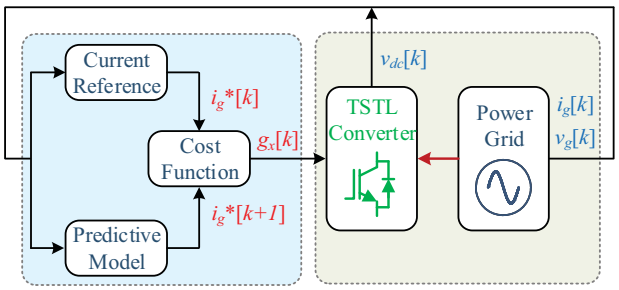

Fig. 2. Structure of the control algorithm.

PI output variable. The reference for the grid current is obtained considering the operating power (measured voltage and current at the dc-side), the output signal from the PI controller, and the power grid voltage. Taking into account that the proposed TSTL-AR converter operates as a linear load, i.e., with a grid current with the same waveform of the power grid voltage. Therefore, it behaves as a resistive load. This can be easily obtained after knowing the values of the active operating power and the root mean square (rms) value of the power grid voltage:

$$R_{TSTL} = \frac{{V_G}^2}{P_{dc}}. \tag{1}$$

By using the equation (1), the reference for the grid current is established from the following relation:

$$i_g{}^* = \frac{1}{R_{TSTL}} v_g \,. \tag{2}$$

Using this strategy, the grid current has the same waveform of the power grid voltage and it is affected by an amplitude defined in accordance with the nominal operating power. In a smart grid context, this strategy is not totally appropriate to be followed, because the negative effects of the power quality problems that appear in the voltage waveform (mainly the harmonics), will be directly reflected in the grid current. Accordingly, due to the impedances in the grid lines, the THD of current will also contribute to aggravate the THD of voltage. As a key feature to mitigate this aspect, instead of using directly the acquired grid voltage, it is used a phase-locked loop (PLL) in order to obtain a unitary sinusoidal signal in phase with the fundamental component of the input signal, i.e., the power grid voltage. The algorithm proposed in [29] was adopted as a single-phase PLL in the TSTL-AR controller. With the PLL, it is also possible to obtain the rms value of the power grid voltage by using a signal that corresponds to the amplitude of the measured voltage. As a result, by using both signals, it is possible to obtain a sinusoidal signal to be used in the control algorithm:

$$i_g{}^* = \sqrt{2}\frac{P_{dc}}{v_{rms}}\, v_{PLL} \,. \tag{3}$$

With the reference for the grid current, a predictive strategy based on a finite control set is applied to decide the state of the proposed TSTL-AR during each sampling period of the control algorithm. The basis for the predictive strategy implemented for the TSTL-AR is described in [30] and [31]. This current control strategy was adopted in detriment of other strategies (e.g., linear PI with sinusoidal pulse-width modulation) due to the simplicity of implementation, as well as the robustness for a large range of operating power [30][32]. In the digital

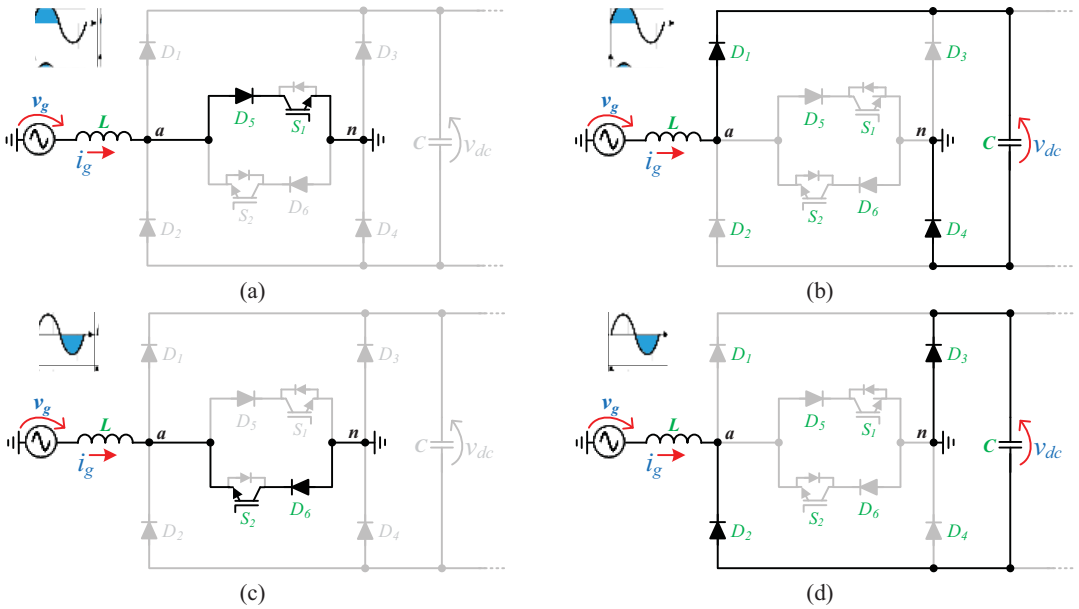

Fig. 3. Operation stages of the proposed two-switch three-level active rectifier (TSTL-AR): (a)-(b) When $v_g > 0$; (c)-(d) When $v_g < 0$.

implementation, the state of the proposed TSTL-AR is decided according to the established reference for the grid current during the period [k, k+1] and the measured current at the instant [k], which stays constant until the instant k+1. Applying the voltage Kirchhoff law and the forward Euler method for the voltage across the inductor, the current $i_g[k+1]$ is obtained from:

$$i_g[k+1] = \frac{v_g[k] - v_{an}[k]}{f_s\, L} + i_g[k]\,, \tag{4}$$

and the voltage established by the proposed TSTL-AR converter (v_{an}), during the period [k, k+1], is decided as a function to minimize the grid current error, i.e., using the quadratic cost function:

$$g[k+1] = \left\| i_g^*[k+1] - i_g[k+1] \right\|^2, \tag{5}$$

where the key objective involves the minimization of the grid current error in steady-state operation. During the positive half-cycle, the voltage v_{an} can adopt the values of 0 (IGBT s_1 on and IGBT s_2 off) or v_{dc} (IGBTs s_1 and s_2 off). On the other hand, during the negative half-cycle, the voltage v_{an} can adopt the values of 0 (IGBT s_2 on and IGBT s_1 off) or -v_{dc} (IGBTs s_1 and s_2 off). The different states of the proposed TSTL-AR are presented in Fig. 3.

III. Analysis and Computational Results

This section introduces a computational analysis of the proposed TSTL-AR, in order to validate the proposed control algorithm and to show its dynamic performance. Therefore, a simulation model was developed in the power electronics software *PSIM*, from *PowerSimTech*. The main characteristics and parameters used in the simulation model are presented in Table I. The simulation results were acquired with a time-step of 1 µs. Fig. 4 shows the controlled variables of the proposed TSTL-AR during a steady-state operation. As a consequence of the proposed control algorithm, the grid current (i_g) is sinusoidal and the converter operates with unitary power factor. It should be highlighted that a grid voltage (v_g) having a THD value of 3.9% was considered as a realistic operating condition for the TSTL-AR. The three distinct voltage levels (v_{an}) defined by the TSTL-AR are evidently identified and are in conformity with the following description: during the positive half-cycle the voltage assumes the values of 0 and +v_{dc} and during the negative half-cycle assumes the values of 0 and –v_{dc}. In this figure (Fig. 4), it can also be seen that the dc-link voltage is controlled to its reference voltage (in this case 400 V, in order to be superior to the maximum of the power grid voltage), presenting the natural oscillation with the double of the frequency of the power grid voltage.

TABLE I. Main Characteristics and Parameters used in the Simulation Model.

Characteristic / Parameter	Label	Value	Unit
Power Grid Voltage	v_g	230	V
Power Grid Voltage THD	THDv	3.9	%
Power Grid Frequency	f_g	50	Hz
Maximum Grid Current THD	THDi	2.5	%
Maximum Operating Power	P_g	3.5	kW
Power Factor	PF	0.99	-
Dc-link Voltage	v_{dc}	400	V
Maximum Switching Frequency	f_{sw}	20	kHz
Sampling Frequency	f_s	40	kHz
L Passive Filter (ac-side)	L	5	mH
C Passive Filter (dc-side)	C	3	mF

Aiming to evaluate the dynamic behavior of the proposed TSTL-AR for different operating powers (1 kW, 2.5 kW and 3.5 kW) and its response towards abrupt variations in the operating power, Fig. 5 shows a comprehensive comparison between the grid current (i_g) and its reference (i_g*). Fig. 5(b) shows a comparison when the operating power increases from 1 kW to 3.5 kW, where the grid current (i_g) reaches its reference with a time delay of 250 µs, i.e., representing 1.25%

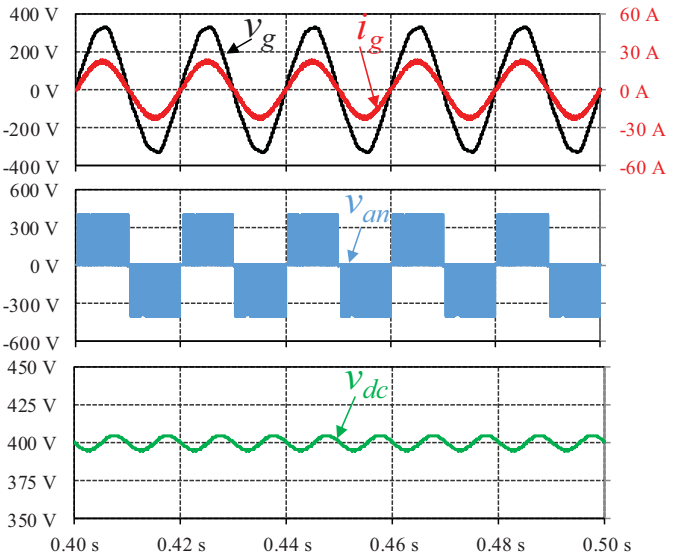

Fig. 4. Main variables of the proposed TSTL-AR during its normal operation: Grid voltage (v_g) and current (i_g); Voltage established downstream the passive filter (v_{an}); Voltage at the dc-link (v_{dc}).

of the voltage period. On the other hand, Fig. 5(c) shows a comparison when the operating power decreases from 3.5 kW to 2.5 kW, where the grid current (i_g) reaches its reference with a time delay of 500 µs, i.e., representing 2.5% of the voltage period. As demonstrated, in both situations (increase and decrease of operating power), the grid current tracks its reference with a fast response and without perturbations affecting the power quality. Moreover, it can be observed a sinusoidal grid current during the three operating power levels, as well as a unitary power factor. A comparison with the classical PFC converter (diode full-bridge ac-dc with a dc-dc boost-type) was established, aiming to verify the estimated efficiency from 0 to a maximum operating power of 3.5 kW. The thermal model for power semiconductors, available in the *PSIM* software, was used and the same parameters were considered for both converters, as well as similar control algorithms based on a finite control set model predictive. As shown in Fig. 6, the proposed TSTL-AR presents a better-estimated efficiency for all the operating power levels, reaching a maximum efficiency of 95.8% and representing a relevant topology for grid-connected electrical appliances in smart grids.

IV. Experimental Validation

This section aims to support the experimental validation of the proposed TSTL-AR and its control algorithm, a dedicated laboratory prototype was developed, including the power and control stages as shown in Fig. 7. The digital control stage is constituted by a C2000 digital signal processor (DSP) from *Texas Instruments* (model F28335) and by a set of control boards used for the voltages and currents acquisition (through an external analog-to-digital ADC converter), as well as to control the IGBTs drivers. On the other hand, the power stage is constituted by the proposed TSTL-AR with IGBTs from *Fairchild Semiconductor* (model FGA25N120FTDTU) and fast recovery diodes from *Littelfuse Power Semiconductors* (model DUR6060W), as well as by IGBT gate-drive

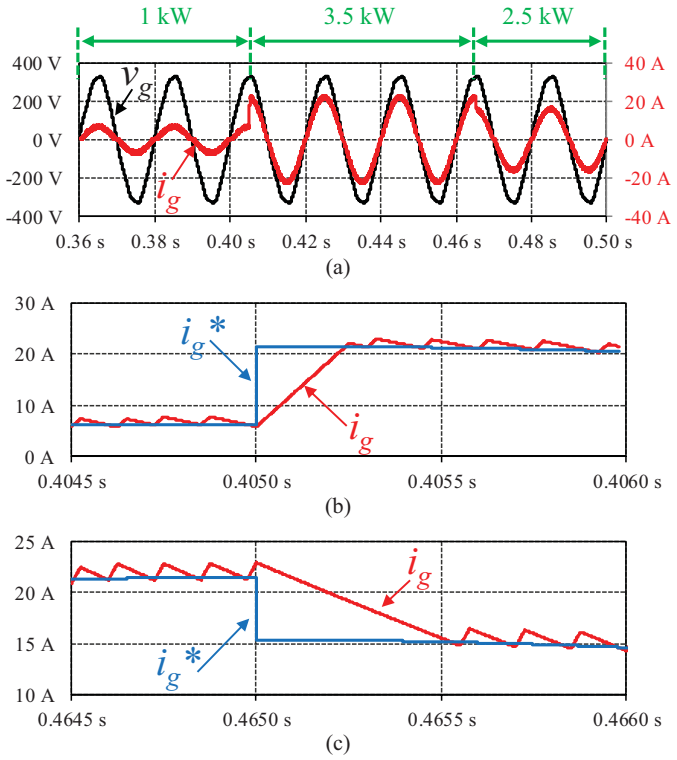

Fig. 5. Dynamic operation of the proposed TSTL-AR: (a) Overview for different operating powers; (b) Detail of the power increase; (c) Detail of the power decrease.

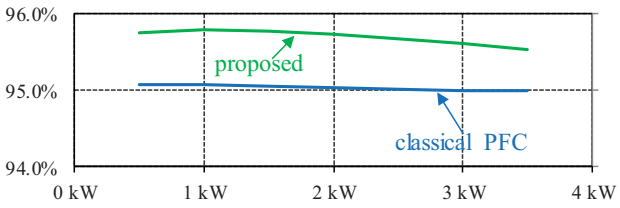

Fig. 6. Comparison in terms of estimated efficiency (from 0 to 3.5 kW) between the proposed TSTL-AR and the classical PFC.

optocouplers from *Avago* (model HCPL3120) and Hall-effect voltage and current transducers.

The digital control algorithm, implemented in a low-level C code, is executed with a sampling frequency of 40 kHz. The time required to implement the core tasks of the control algorithm is presented in Table II. The digital filter to extract the mean value of the dc-link voltage is the task that requires more time to be executed, and the cost function is the faster task implemented. Through a power quality analyzer from *Fluke* (model 435), Fig. 8 shows the spectral analysis and the THD value of the grid current. The results shown in Fig. 8(a) were obtained before the IGBTs turn-on, i.e., only considering the operation of the diode-bridge rectifier, and the results in Fig. 8(b) were obtained after the IGBTs turn-on. As it can be seen, the 3th, 5th, and 7th harmonics were practically eliminated and the THD was reduced from 59.9% to 6.3%, validating the advantages of the proposed TSTL-AR. Fig. 9(a) shows the experimental results in the ac-side, illustrating that the grid current (i_g) has a sinusoidal waveform, even when it is connected to a power grid with a significant voltage (v_g) THD

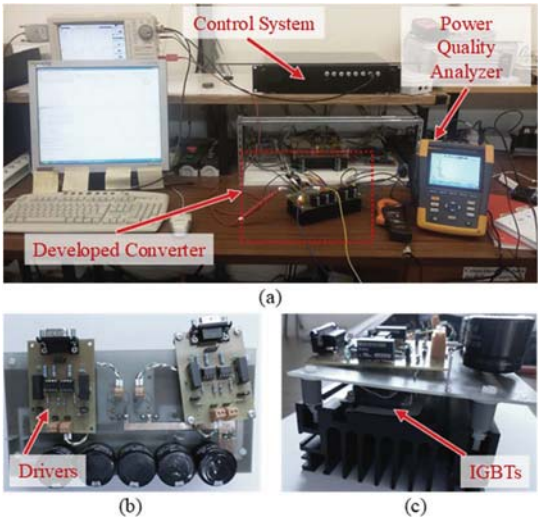

Fig. 7. Developed system: (a) Laboratorial workbench; (b) Developed TSTS-AR prototype; (c) Detail of the developed TSTS-AR prototype.

TABLE II. TIME REQUIRED TO IMPLEMENT THE CONTROL ALGORITHM.

TASK	TIME
Signals acquisition from ADCs	0.69 µs
PLL implementation	0.82 µs
Digital filter for the dc-link voltage	0.90 µs
Dc-link voltage control	0.55 µs
Establishment for the current reference	0.82 µs
Cost Function	0.50 µs
IGBTs state selection	0.80 µs

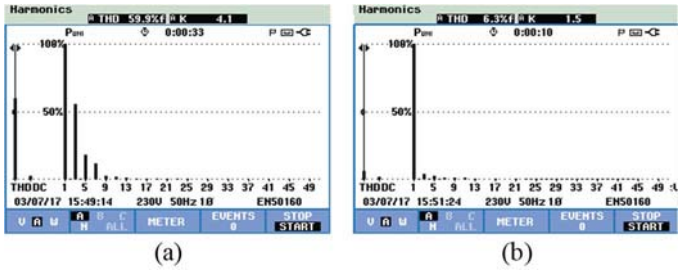

Fig. 8. Spectral analysis and THD value of the grid current: (a) Before the IGBTs turn on; (b) After the IGBTs turn on.

value. As expected, both variables are in phase, meaning an operation with a unitary power factor. A detail of the grid current in contrast with the gate-emitter voltage of the IGBT s_1 is presented in Fig. 9(b).

In this experimental result, it is possible to identify the non-fixed switching frequency, which is a natural characteristic of the finite control set model predictive control. In this detailed case, a maximum switching frequency of 10 kHz was measured. In order to verify the gate signals of the IGBTs during a period of the power grid voltage (20 ms), Fig. 10 shows the grid current (i_g), the gate-emitter voltage of both IGBTs s_1 and s_2, and the power grid voltage (v_g). As shown, the obtained results are in accordance with the described operation in the control algorithm?m, i.e., the IGBT s_1 is switched during the positive half-cycle and the IGBT s_2 is switched in the other half-cycle.

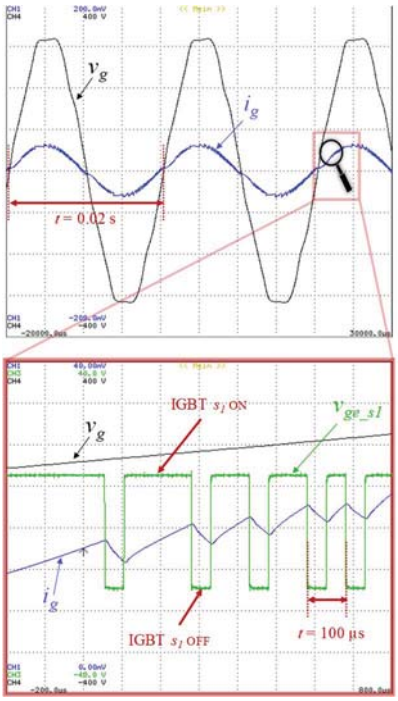

Fig. 9. Experimental results: Grid voltage (v_g), grid current (i_g) and gate-emitter voltage of the IGBT s_1 (v_{ge_s1}).

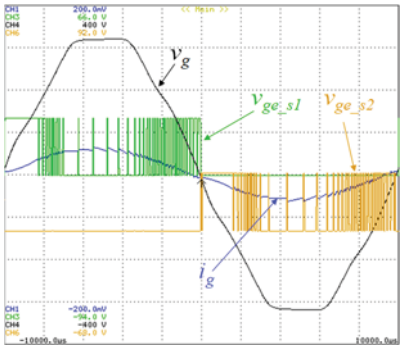

Fig. 10. Experimental results: Grid voltage (v_g), grid current (i_g), gate emitter voltage of the IGBT s_1 (v_{ge_s1}) and gate emitter voltage of the IGBT s_2 (v_{ge_s2}).

V. CONCLUSION

A novel two-switch three-level active rectifier (TSTL-AR) is proposed as an important contribution to ensure power quality aspects of grid-connected electrical appliances in smart grids. The principle of operation is presented in detail along the paper, including an exhaustive description about the control algorithm, mainly, based on the dc-link voltage control, the reference for the grid current, and the predictive current control. A laboratory prototype was developed and an experimental validation was performed, allowing to acquire the most relevant results. As demonstrated along the paper, the proposed TSTL-AR operates with sinusoidal grid current, reduced value of total harmonic distortion, controlled dc-link voltage, and unitary power factor, representing an attractive alternative for the classical PFC converter for grid-connected electrical appliances in smart grids.

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