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Comparative Analysis Between Different Approaches for Single-Phase PLLs

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***Abstract*—This paper presents a comparative analysis between two distinct synchronizing circuits, which are usually applied as the core of control algorithms for single-phase power quality applications. One of these synchronizing circuits corresponds to a single-phase Phase-Locked Loop (PLL), implemented in α-β coordinates ($\alpha\beta$-PLL), whereas the other one corresponds to the Enhanced PLL (E-PLL). The major contribution of this paper is to present a single-phase PLL oriented to power quality applications, with a very simple structure, capable to be synchronized with the fundamental component of an input signal (voltage or current), even considering substantial disturbances, such as, frequency deviations, phase shifts, harmonic components and amplitude variations. Simulation and experimental results, involving these two synchronizing circuits submitted to three different test cases, are provided in order to compare their transient and steady-state performance. Moreover, it is also presented a comparison involving the processing speed and memory requirements of these synchronizing circuits in the DSP TMS320F28335.**

***Index Terms*—Phase-Locked Loop (PLL), $\alpha\beta$-PLL, Enhanced PLL (E-PLL), Digital Signal Processor (DSP), Power Quality.**

I. Introduction

SYNCHRONIZING CIRCUITS are essential to grid connected power electronics equipments, namely on those related with power quality applications, where they can be applied to help identifying power quality events [1]-[5]. Basically, synchronizing circuits are applied in control algorithms of active power conditioners, such as active power filters [6][7], uninterruptable power supplies [8][9][10], dynamic voltage restorers [11], power factor correction converters [12][13], EV battery chargers [14][15], and grid interface of renewables [16][17][18]. These applications are, increasingly, considered in the context of micro-grids, where the harmonic propagation and the dynamic phase deviation occurs frequently [19][20][21]. Indeed, such issues compromise the accurate measurement of active and reactive power, reinforcing the necessity of using synchronizing circuits capable of identifying, correctly, the phase-angle of a specific harmonic component. In fact, the aforementioned active power conditioners comprise control algorithms that extract, in real time, the fundamental component of the ac-mains voltage or current. Moreover, synchronizing circuits are able to identify, in real-time, undesirable components of the input signal. Unfortunately, frequency-domain mathematical tools, for example, the Discrete Fourier Transform (DFT), are unreliable whenever it is required to cope with frequency deviations or unknown harmonic components [22]. It is worth to mention that synchronizing circuits can also be applied in power quality measurement instruments, as described in [23], where they are designed to evaluate the fundamental frequency, in order to set a convenient sampling rate. Furthermore, synchronizing circuits are also a desirable alternative to spectral analysis algorithms, which are restricted to an observation window, ruled by the IEC 61000-4-30 standard. In accordance to [23], spectral analysis algorithms do not allow an accurate evaluation of the fundamental frequency.

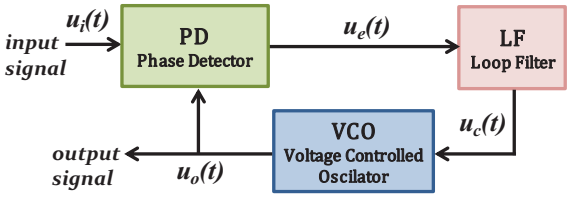

Fig. 1. Block diagram of an analog PLL (Phase-Locked Loop).

Given the wide range of applications for synchronizing circuits, and being the Phase-Locked Loop (PLL) the most used synchronizing circuit, due to its adaptability to different conditions [24], this paper presents a relevant and comprehensive comparison between two PLL schemes: The Enhanced PLL (E-PLL) [22], [25]-[28], and the PLL implemented in α-β coordinates ($\alpha\beta$-PLL) [29][30] modified to single-phase circuits. The $\alpha\beta$-PLL corresponds to a pPLL type and can be understood as a type of Synchronous Reference Frame-PLL (SRF-PLL) [31]-[32]. On the other hand, the E-PLL can be considered as a Quadrature Signal Generation-Based PLL (QSG-PLL) [33]. Both PLL circuits are derived from the classical structure of an analog PLL, i.e., constituted by a Phase Detector (PD), a Loop Filter (LF) and a Voltage Controlled Oscillator (VCO) [33]. This basic structure can be observed in Fig. 1. The E-PLL and the $\alpha\beta$-PLL share similar LF and VCO structures, being the PD method the distinctive feature.

Essentially, single-phase synchronizing circuits have an undesirable behavior, which consists in the fact that their internal control signals present oscillatory components when occurs a disturbance in the input signal. These oscillatory components remain in the internal signals, while the new steady-state condition is not reached, resulting in an oscillating

error in the output signal. It can occur even when the input signal is composed only by a fundamental component. This behavior may compromise the effectiveness of active power conditioners, if these single-phase synchronizing circuits are included in their control systems. An alternative solution to overcome such problem corresponds to the use of low-pass [34] or notch filters [35]. Nevertheless, this solution may compromise the transient response of the PLL and, furthermore, do not assure the entire elimination of the harmonic components.

In this context, this paper presents a single-phase synchronizing PLL circuit, with a very simple structure, based on α-β coordinates. When compared with the conventional PLL circuits, as contribution to improve the state-of-the-art, the PLL based on α-β coordinates presents a faster response time and it is capable of avoiding the use of low-pass filters to overcome the problem of oscillatory components in the internal control signals, which is observed in QSG-PLLs when transients occur. The main contribution of this paper is a single-phase PLL oriented to power quality applications, presenting a very simple structure, which can be synchronized with the fundamental component of an input signal, even when the input signal has substantial disturbances (e.g., frequency deviations, phase-shifts, harmonic components and amplitude variations). A comparative analysis between the PLL based on α-β coordinates and the E-PLL is presented.

As aforementioned in this section, according to [33], the single-phase PLLs are classified into 2 main different types: QSG-PLLs and pPLLs. Based on this classification, the E-PLL corresponds to a QSG-PLL type, whereas the $\alpha\beta$-PLL corresponds to a pPLL type. It is important to comment that there are other QSG-PLLs such as those based on the Second Order Generalized Integrators (SOGI-PLL) [36] or even those based on All-Pass Filters (APF-PLL) [37]. Due to this reason, the E-PLL and $\alpha\beta$-PLL were chosen to be compared based on different substantial disturbances, such as, frequency deviations, harmonic distortions, phase jumps and amplitude variations. In all of these test cases, the $\alpha\beta$-PLL presented a better transient response. Furthermore, it is possible to assure that the $\alpha\beta$-PLL presents lower computational burden, once the phase detection can be implemented through a Look-Up-Table (LUT), or similar approaches, where the 90º delay of the auxiliary signal is determined based on the average component of the internal angular frequency. This average component can be updated at half-cycle period of the fundamental frequency comprehended in the input signal. On the other hand, is also possible to conclude that the $\alpha\beta$-PLL requires more memory space to implement the auxiliary arrays to its phase detection method. These issues are exploited in this paper. All of the test cases were performed by simulation and experimental results. Moreover, each processing time is also presented, as well as the memory resources needed to implement each PLL circuit on the DSP TMS320F28335. This paper presents further development to the work presented in [5], where these PLLs were tested on a controller of a custom power device, and compensation characteristics were evaluated.

II. Overview of the PLLs

Each block shown in Fig. 1 has a distinct function. The PD (Phase Detector) block outputs a signal ($u_e(t)$) that represents the phase difference between the input signal ($u_i(t)$) and the PLL output signal ($u_o(t)$). The LF (Loop Filter) block, for a given input ($u_e(t)$), outputs a "correction" signal ($u_c(t)$), which is used by the VCO (Voltage Controlled Oscillator) block that generates the PLL output. The tracked fundamental angular frequency ($\omega_o(t)$) of the input signal ($u_i(t)$) is given by:

$$\omega_o(t) = \omega_c + u_i(t), \quad (1)$$

where ω_c is a constant value that corresponds to a pre-determined center angular frequency (usually the electrical grid angular frequency).

A. The Single-Phase E-PLL

The Enhanced PLL (E-PLL) synchronizing circuit [22], [25]-[28], can be described as a multiplier-based PLL [4]. The distinctive feature of this circuit is the incorporation of an amplitude control loop, which is included in the PD block, as it can be seen in Fig. 2.

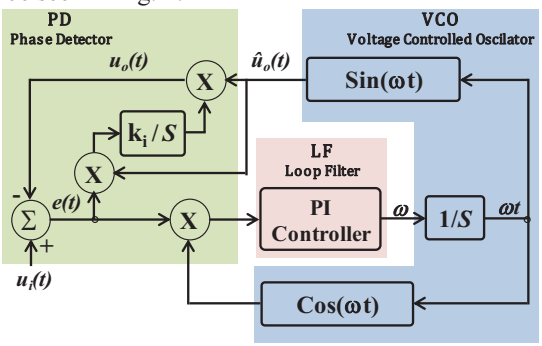

Fig. 2. Block diagram of the Enhanced PLL (E-PLL).

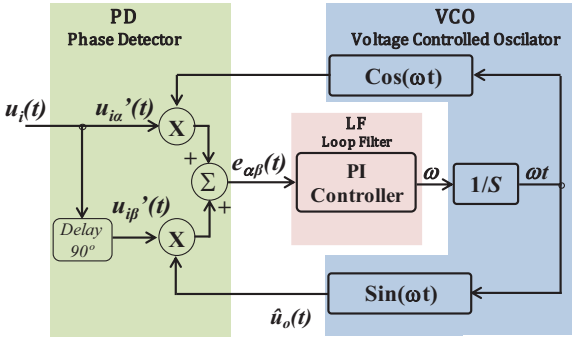

Fig. 3. Block diagram of the $\alpha\beta$-PLL.

Having control circuits to determine amplitude, phase and frequency, this PLL is able to detect harmonic components of a given input. However, the existence of this amplitude control loop increases the complexity of the E-PLL. Moreover, it is worth to comment that, in some applications, amplitude is not a relevant information. For those applications, the unity vector of the output signal ($\hat{u}_o(t)$) can be used, since it carries frequency and phase information. Then, this unity vector can be multiplied by a gain, which is equal to the nominal voltage

amplitude of a given power system. Thus, the output signal ($u_o(t)$) is the fundamental component of the input signal ($u_i(t)$). This can be useful in control algorithms of Active Power Filters [6][7] and DVRs [11].

The VCO block is constituted by a time integrator that generates a ramp varying from 0 to 2π rad. This ramp, with period equivalent to the tracked fundamental angular frequency (ω_o), is fed to sine and cosine generators. The fundamental frequency tracking is performed by the LF block, which consists of a PI controller. The VCO block and the LF block are the cornerstones of the E-PLL circuit.

B. The Single-Phase αβ-PLL

The αβ-PLL shown in Fig. 3 is an adaptation for single-phase power systems of the PLL presented in [29], initially proposed to three-phase systems. Its concepts are based on the instantaneous power theory (*pq*-theory) [38].

In this particular case, due to the use of a single-phase voltage or current as input, the transformation to α-β coordinates is a fictitious one, where the input signal $u_i(t)$ corresponds to the α component ($u_{i\alpha}'(t)$), and the β component is generated by lagging the signal in 90° ($u_{i\beta}'(t)$). By creating a fictitious α-β frame for single-phase power systems is not an unidentified approach, as it can be seen in [5]. The 90º lagging signal can be obtained by analog or digital circuits. In a digital implementation, the delay can be easily implemented through the use of a First-In First-Out (FIFO) memory structure, with size of one fourth of the number of samples in a period of the input signal. This method is even simpler since LUT, or other approach, was not applied, resulting in a negligible processing time. However, if the frequency of the input signal presents several changes, this PLL produces a phase-angle error, once the applied delay to α-β components is different from 90º. This issue is analyzed in Section III, and reinforced through simulation and experimental results.

The output of the sine block is the unity vector $\hat{u}_o(t)$, which has the same phase angle and frequency of the fundamental component of the input signal, $u_i(t)$, when the error signal, $e_{\alpha\beta}(t)$, reaches the zero value.

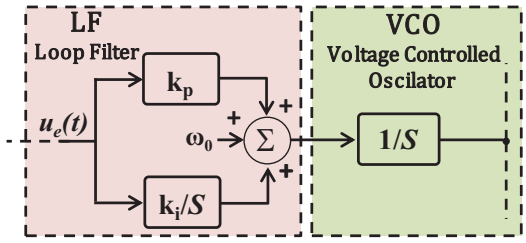

Fig. 4. LF block and VCO block time integrator.

III. Linear Model of the PLLs

As described in section II, both E-PLL and αβ-PLL schemes share similar LF and VCO structures, represented in Fig. 4.

The output of the PI controller corresponds to the fundamental angular frequency of the system voltage (in rad/s), and it is also the input of the VCO time integrator, which generates a resettable ramp from 0 to 2π rad. The PI controller is designed such that oscillating components, which may appear at the error signal, do not compromise its performance. It is worth to comment that some oscillating components that still remain at the tracked frequency (output of the PI controller) are also minimized when this signal is integrated. For the E-PLL, shown in Fig. 2, the input signal, $u_i(t)$, and the output signal, $u_o(t)$, are represented by the following equations:

$$u_i(t) = U_i \sin(\omega_1 t + \varphi_1); \tag{2}$$

$$u_o(t) = U_o \sin(\omega_2 t + \varphi_2). \tag{3}$$

Assuming that the amplitude control loop has reached its steady-state condition, the amplitude values U_i and U_o are equal. Thus, the signal error, $e(t)$, can be written as:

$$e(t) = U\left(\sin(\omega_1 t + \varphi_1) - \sin(\omega_2 t + \varphi_2)\right), \tag{4}$$

where U is equal to U_i and U_o. The control signal $e(t)$ corresponds to one of the inputs of the vector product, which constitutes the last stage of the PD block of the E-PLL. The other input is the unit vector, $\hat{u}_o(t)$, which corresponds to:

$$\hat{u}_o(t) = \cos(\omega_2 t + \varphi_2). \tag{5}$$

The output of the PD block, which corresponds to the product involving $e(t)$ and $\hat{u}_o(t)$, is given by:

$$u_e(t) = U\begin{Bmatrix} \sin(\omega_1 t + \varphi_1)\cos(\omega_2 t + \varphi_2) - \\ \sin(\omega_2 t + \varphi_2)\cos(\omega_2 t + \varphi_2) \end{Bmatrix}. \tag{6}$$

Expanding the internal products at equation (6), the control signal $u_e(t)$ is equal to:

$$u_e(t) = \frac{U}{2}\begin{Bmatrix} \sin[(\omega_1+\omega_2)t + (\varphi_1+\varphi_2)] + \\ \sin[(\omega_1-\omega_2)t + (\varphi_1-\varphi_2)] + \\ \sin(\varphi_1-\varphi_2) \end{Bmatrix}. \tag{7}$$

When the E-PLL is nearly locked at center angular frequency (i.e., $\omega_1 \approx \omega_2 \approx \omega_C$), the control signal $u_e(t)$ is reduced to an average component plus oscillating components at 2ω, with the input voltage ($u_i(t)$) only presenting a fundamental component. These average and oscillating components are given by:

$$u_e(t) = \frac{U}{2}\begin{Bmatrix} \sin(2\omega_C t)[\cos(\varphi_1+\varphi_2) - \cos(2\varphi_2)] + \\ \cos(2\omega_C t)[\sin(\varphi_1+\varphi_2) - \sin(2\varphi_2)] + \\ \sin(\varphi_1-\varphi_2) \end{Bmatrix}. \tag{8}$$

Considering small phase-angle deviations, it is possible to assume the following conditions:

$$\sin(\phi_1 + \phi_2) - \sin(2\phi_2) = \phi_1 - \phi_2 ; \tag{9}$$

$$\sin(\phi_1 - \phi_2) = \phi_1 - \phi_2 ; \tag{10}$$

$$\cos(\phi_1 + \phi_2) - \cos(2\phi_2) = 0 . \tag{11}$$

Based on the aforementioned conditions, and assuming that U is normalized to unity, the control signal $u_e(t)$ can be linearized through the following equation:

$$U_E(S) = \left[\varphi_1(S) - \varphi_2(S)\right]\left[\frac{S^2 + 2S + 4\omega_C^2}{2S^2 + 8\omega_C^2}\right]. \tag{12}$$

Including the Loop Filter (LF) and the Voltage Controlled Oscillator (VCO), the linearized behavior of the E-PLL is described by the simplified block diagram shown in Fig. 5.

It is worth to comment that when the E-PLL tracks correctly the phase angle of $u_i(t)$ (i.e., $\phi_1 \approx \phi_2 \approx \phi$), both average and oscillating components, presented in (8), are reduced to zero. Thus, it can be verified that there is no residual oscillating component at $u_e(t)$ when the E-PLL reaches its steady-state condition. Such condition just occurs if $u_i(t)$ is composed only by a fundamental component, i.e., without harmonics.

For the $\alpha\beta$-PLL illustrated in Fig. 3, the input voltage $u_i(t)$ is normalized to present a unitary amplitude. Therefore, $u_{i\alpha}'(t)$ and $u_{i\beta}'(t)$ are represented by the following equations:

$$u_{i\alpha}'(t) = \sin(\omega_1 t + \varphi_1); \tag{13}$$

$$u_{i\beta}'(t) = \sin(\omega_1 t + \varphi_1 - \pi/2) = -\cos(\omega_1 t + \varphi_1). \tag{14}$$

The control signal $e_{\alpha\beta}(t)$ is given by:

$$\begin{aligned} e_{\alpha\beta}(t) &= u_{i\alpha}'(t)\cos(\omega_2 t + \varphi_2) + u_{i\beta}'(t)\sin(\omega_2 t + \varphi_2) = \\ &= \sin(\omega_1 t + \varphi_1)\cos(\omega_2 t + \varphi_2) - \\ &- \cos(\omega_1 t + \varphi_1)\sin(\omega_2 t + \varphi_2); \end{aligned} \tag{15}$$

where $\sin(\omega_1 t + \phi_1)$ and $\sin(\omega_2 t + \phi_2)$ are internal control signals. Expanding the internal products at equation (15), the control signal $e_{\alpha\beta}(t)$ is equal to:

$$e_{\alpha\beta}(t) = \frac{1}{2}\left\{\begin{array}{l} \sin[(\omega_1+\omega_2)t + (\varphi_1+\varphi_2)] - \\ -\sin[(\omega_1+\omega_2)t + (\varphi_1+\varphi_2)] + \\ +2\sin[(\omega_1-\omega_2)t + (\varphi_1-\varphi_2)] \end{array}\right\}. \tag{16}$$

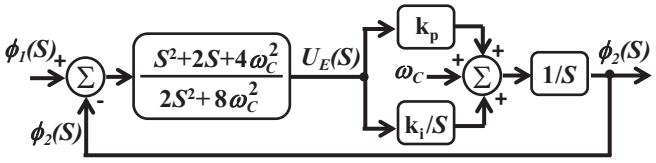

Fig. 5. Linear model for the E-PLL.

When the $\alpha\beta$-PLL is nearly locked at the center angular frequency (i.e., $\omega_1 \approx \omega_2 \approx \omega_C$), the control signal $e_{\alpha\beta}(t)$ is reduced to an average component, since the oscillating components at $2\omega t$ are cancelled. Thus, the value of $e_{\alpha\beta}(t)$ is given by:

$$e_{\alpha\beta}(t) = \sin(\varphi_1 - \varphi_2). \tag{17}$$

Finally, when the $\alpha\beta$-PLL tracks correctly the phase angle of $u_i(t)$ (i.e., $\phi_1 \approx \phi_2 \approx \phi$), the control signal $e_{\alpha\beta}(t)$ is reduced to zero and the PLL reaches its steady state condition. The signal $e_{\alpha\beta}(t)$ is linearized considering small phase-angle deviations, and its linear representation is given by:

$$E_{\alpha\beta}(S) = (\varphi_1(S) - \varphi_2(S)). \tag{18}$$

In a similar way as the one applied to obtain the E-PLL linear model, the linearized behavior of the $\alpha\beta$-PLL is described by the simplified block diagram shown in Fig. 6. It is relevant to note that these linear models can be employed just when the input signal is composed only by its fundamental component. The inclusion of linear models is to highlight the second-harmonic oscillating component when a transient occurs. In relation to the E-PLL, its linear model may be applied to analyze disturbances involving frequency or phase-angle deviations. On the other hand, the linear model of the $\alpha\beta$-PLL only may be applied to analyze phase-angle deviations. For any other condition, all of the aforementioned mathematical treatment must be redone. Thus, to better understand the behavior of these synchronizing circuits, it is introduced, in sequence, a mathematical analysis of both PLL circuits under some power quality disturbances.

A. Voltage Sags/Swells

Considering this disturbance as a transient one, it is assumed as initial condition that both PLL circuits are synchronized with the input signal, such that:

$$u_0(t) = u_i(t) = U\sin(\omega_1 t + \varphi_1). \tag{19}$$

Now, when this transient event occurs, the input signal, $u_i(t)$, is equal to:

$$u_i(t) = K\sin(\omega_1 t + \varphi_1). \tag{20}$$

In this condition, while the amplitude loop of the E-PLL does not reach this new amplitude value, it appears an oscillating component at $2\omega_1 t$. Indeed, as it can be obtained from Fig. 2, the input at the integrator is given by:

$$\begin{aligned} e(t)\cdot\hat{u}_0(t) &= (K-U)\sin(\omega_1 t + \varphi_1)\sin(\omega_1 t + \varphi_1) = \\ &= \frac{(K-U)}{2}\left[1 - \cos(2\omega_1 t + 2\varphi_1)\right]. \end{aligned} \tag{21}$$

Therefore, only when the average value becomes zero, the signal produced by the E-PLL is equal to $K\sin(\omega_1 t + \phi_1)$ and, as a consequence, the oscillating component at $2\omega_1 t$ is extinguished.

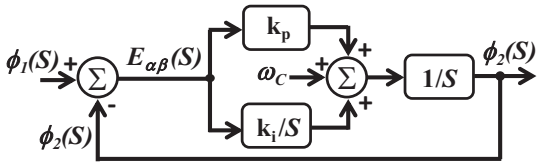

Fig. 6. Linear model for the $\alpha\beta$ -PLL

On the other hand, the $\alpha\beta$-PLL does not present any oscillating component when this disturbance occurs. It can easily be verified through the control signal $e_{\alpha\beta}(t)$, which one, in this transient, is given by:

$$\begin{aligned} e_{\alpha\beta}(t) &= K\sin(\omega_1 t + \phi_1)\cos(\omega_1 t + \phi_1) - \\ &- K\cos(\omega_1 t + \phi_1)\sin(\omega_1 t + \phi_1). \end{aligned} \tag{22}$$

Thus, in comparison with the E-PLL, it can be noted that the $\alpha\beta$-PLL provides a better performance for active power conditioners when applied to compensate amplitude variations of the system voltage.

B. Frequency Deviations

Although there are very strict regulations for frequency deviations, this disturbance may occur in weak power systems as, for example, islanded electrical power systems. Based on the aforementioned analysis, it is possible to note that the

E-PLL is capable to track the frequency and phase angle of the input signal. However, for the $\alpha\beta$-PLL circuit, illustrated on Fig. 3, the generated signals presents a phase angle error in comparison with the input signal. Indeed, when occurs a frequency deviation, the control signal $u_{i\beta}'(t)$ is no more 90º delayed from $u_{i\alpha}'(t)$, as it should be. In this case, $u_{i\alpha}'(t)$ and $u_{i\beta}'(t)$ are given by:

$$\begin{cases} u_{i\alpha}'(t) = sin(\omega_3 t + \varphi_3) \\ u_{i\beta}'(t) = sin(\omega_3 t + \varphi_3 - \delta); \end{cases} \tag{23}$$

where ω_3 corresponds to the new angular frequency of the input signal. As a consequence, the control signal $e_{\alpha\beta}(t)$ presents an oscillating component at $2\omega_3$, plus an average component different from the one presented in equation (17). This is demonstrated as follows:

$$\begin{aligned} e_{\alpha\beta}(t) = {} & sin(\omega_3 t + \varphi_3)\, cos(\omega_1 t + \varphi_1) + \\ & + cos(\omega_3 t + \varphi_3 - \delta)\, sin(\omega_1 t + \varphi_1). \end{aligned} \tag{24}$$

Expanding the internal products at equation (24), the control signal $e_{\alpha\beta}(t)$ is equal to:

$$e_{\alpha\beta}(t) = \frac{1}{2} \begin{Bmatrix} sin[(\omega_3 + \omega_1)t + (\varphi_3 + \varphi_1)] - \\ - sin[(\omega_3 - \omega_1)t + (\varphi_3 - \varphi_1)] + \\ + cos[(\omega_3 - \omega_1)t + (\varphi_3 - \delta - \varphi_1)] - \\ - cos[(\omega_3 + \omega_1)t + (\varphi_3 - \delta + \varphi_1)] \end{Bmatrix}. \tag{25}$$

In this case, when the $\alpha\beta$-PLL is nearly locked at the new angular frequency (i.e., $\omega_1 \approx \omega_3$), the control signal $e_{\alpha\beta}(t)$ still presents oscillating and average components. These components are given by:

$$e_{\alpha\beta}(t) = \frac{1}{2} \begin{Bmatrix} sin[(2\omega_3)t + (\varphi_3 + \varphi_1)] - \\ - sin[(\varphi_3 - \varphi_1)] + cos[(\varphi_3 - \delta - \varphi_1)] + \\ + cos[(2\omega_3)t + (\varphi_3 - \delta + \varphi_1)] \end{Bmatrix}. \tag{26}$$

Due to the use of the PI controller, together with an integrator, this oscillating component, observed at $e_{\alpha\beta}(t)$, is minimized and, moreover, this average component is eliminated, which leads to:

$$sin(\varphi_3 - \varphi_1) = cos(\varphi_3 - \delta - \varphi_1). \tag{27}$$

Based on equation (27) it can be noted that ϕ_3 and ϕ_1 are equal only if $\delta = 90º$. Thus, in this case, the internal angular frequency presents a small ripple, leading to phase deviations of the output signal. In literature there are proposals to overcome this drawback as those introduced in [39] and [40] for instance, which consists in dynamically adjusting the number of samples per cycle in order to achieve a constant 90º delay at the fundamental frequency with the FIFO strategy. Nevertheless, in the great majority of power systems, where frequency deviations are very strict, the $\alpha\beta$-PLL with constant sampling frequency is still suitable to be used in control algorithms for active power conditioners.

C. Harmonics

Based on the aforementioned analysis, it may be noted that the introduction of harmonic components in the input signal results in oscillating components in $u_e(t)$ for the E-PLL, and also in $e_{\alpha\beta}(t)$ for the $\alpha\beta$-PLL. However, considering that the fundamental component of $u_i(t)$ is usually substantially greater than the harmonic components, it is possible to ensure that both PLL circuits are suitable to correctly detect the angular frequency and phase angle of the fundamental component. On the other hand, it is important to note that, since these oscillating components may appear at the signals produced by the E-PLL and $\alpha\beta$-PLL, it is possible to reduce them by adjusting the internal PI parameters of these PLL circuits, but it results in a slower dynamic response. Hence, it is necessary to establish the best compromise between the dynamic response time and the harmonic distortion level of the output signal.

IV. Simulation Results

In order to better observe the behavior of the E-PLL and $\alpha\beta$-PLL circuits under different operation conditions, including transient events, three different simulated test cases are introduced in this section. These simulations were performed using PSIM software.

For the three test cases the internal PI parameters (k_p and k_i) of both PLL circuits are equal to 100 and 3,000, respectively, and the amplitude loop of the E-PLL presents an internal gain equal to 20. These parameters were obtained through offline simulations, considering the performance of both PLLs under a range involving different combinations of these internal parameters. Indeed, in situations, where it is not possible to predict the characteristic of the input signal, a feasible method to tune the PI parameters consists in submitting both PLL circuits to a range of different values. Basically, in this method, it must be established the characteristics of the input signal, as well as a desired condition of the produced signal. Thus, the employed constraint was a produced signal with a total harmonic distortion (THD) below 3%, considering an input signal with a THD over 70% (which corresponds to a distortion level only common for current signals). It is important to comment that, for all simulation results, the angular frequencies were normalized by a constant equal to 200. This normalization was done to provide a better view of the angular frequencies together with the other control signals.

In the first test case, the input signal ($v_i(t)$) is composed only by a fundamental component. At time $t = 2.005$ s it is introduced a disturbance, such that the input signal presents its amplitude decreased by 50% (a voltage sag event). In this test case, the input signal is given by:

$$\begin{aligned} & v_i(t) = sin\,(100\,\pi\,t) \qquad (t < 2.000\ s) \\ & v_i(t) = 0.5 \cdot sin\,(100\,\pi\,t) \qquad (t \geq 2.005\ s) \end{aligned} \tag{28}$$

Fig. 7 and Fig. 8 present the transient response of the two PLL schemes due to this disturbance. In Fig. 7 is illustrated the input signal (v_i) together with the control signals ωt_{E_PLL}, ω_{E_PLL} and v_{E_PLL} for the E-PLL during the time interval when this disturbance occurs. As expected, the control signal ω_{E_PLL} presents an oscillatory component at 2ω, while the new

amplitude is not reached. Due to the considered PI parameters, the E-PLL reaches its new steady-state condition only 162 ms after this disturbance occurs. In Fig. 8, is illustrated the input signal (v_i) together with the control signals $\omega t_{\alpha\beta\_PLL}$, $\omega_{\alpha\beta\_PLL}$ and $v_{\alpha\beta\_PLL}$ for the $\alpha\beta$-PLL under the same conditions. The $\alpha\beta$-PLL presents a much faster response to this disturbance, and reaches its steady state condition in a time period equal to 5.1 ms (approximately a quarter of a 50 Hz cycle).

In the second test case, the input signal (v_i) presents, at the time instant $t = 1$ s, a frequency deviation from 50 Hz to 45 Hz. This 45 Hz frequency value was chosen because it corresponds to the lowest acceptable value of under frequency (usually caused by severe system overload) in 50 Hz electrical power systems, since for lower frequency values, power plants are removed from the power system [41]. Again, in this test case the input signal waveform is only composed by a fundamental component with unitary amplitude, which corresponds to:

$$\begin{aligned} v_i(t) &= sin\,(100\,\pi\,t) \quad (t < 1.0\ s) \\ v_i(t) &= sin\,(90\,\pi\,t) \quad (t \geq 1.0\ s) \end{aligned} \tag{29}$$

In Fig. 9 is illustrated the input signal (v_i) and the angular frequency (in rad/s) determined from both synchronizing circuits, denominated as ω_{E_PLL} and $\omega_{\alpha\beta\_PLL}$. As expected, when the disturbance occurs, the control signal ω_{E_PLL} presents an oscillatory component at 2ω while the new angular frequency is not reached, whereas $\omega_{\alpha\beta\_PLL}$ remains with this oscillatory component permanently, since the input signal $u_{i\beta'}(t)$ is no more 90º shifted from $u_{i\alpha'}(t)$.

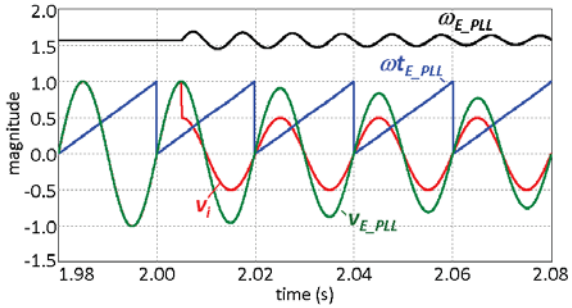

Fig. 7. Input signal (v_i) and control signals ωt_{E_PLL}, ω_{E_PLL} and v_{E_PLL} produced by the E-PLL in response to a voltage sag (first test case).

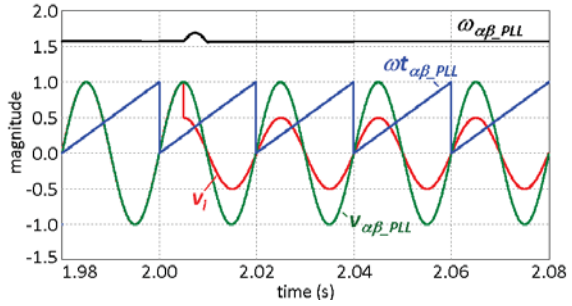

Fig. 8. Input signal (v_i) and control signals $\omega t_{\alpha\beta\_PLL}$, $\omega_{\alpha\beta\_PLL}$ and $v_{\alpha\beta\_PLL}$ produced by the αβ-PLL in response to a voltage sag (first test case).

In Fig. 10 is illustrated the input signal (v_i) together with the control signals ωt_{E_PLL}, ω_{E_PLL} and v_{E_PLL}, with the E-PLL under steady-state condition. At this condition, the output (v_{E_PLL}) and the input (v_i) signals are tracked, with the angular frequency presenting an average value only.

In Fig. 11 is showed the input signal (v_i) together with the control signals $\omega t_{\alpha\beta\_PLL}$, $\omega_{\alpha\beta\_PLL}$ and $v_{\alpha\beta\_PLL}$, with the $\alpha\beta$-PLL under steady-state condition. At this condition, the output ($v_{\alpha\beta\_PLL}$) and the input (v_i) signals present a phase-angle error equal to 3.3º, with the angular frequency presenting an average value plus an oscillating component at 2ω. It is important to comment that, even with the presence of this oscillating component at $\omega_{\alpha\beta\_PLL}$, the integrator located at the output of the PI controller acts as a low-pass filter, such that $v_{\alpha\beta\text{-}PLL}$ presents a very low THD (less than 0.5%).

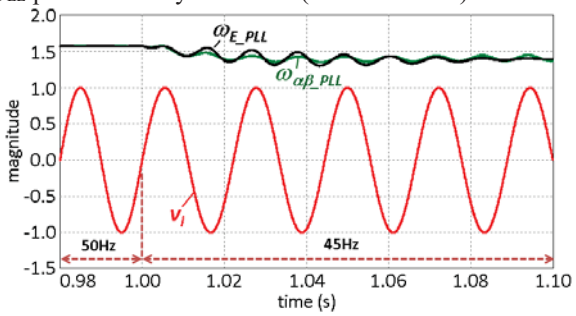

Fig. 9. Angular frequencies ($\omega_{E\text{-}PLL}$ and $\omega_{\alpha\beta\text{-}PLL}$) for both PLLs tracking an input signal (v_i) with a frequency drop from 50 Hz to 45 Hz (second test case).

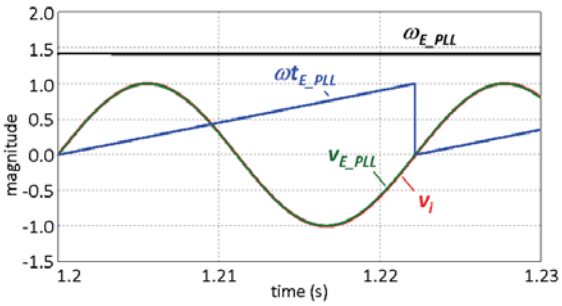

Fig. 10. Input signal (v_i) and control signals $\omega t_{E\text{-}PLL}$, $\omega_{E\text{-}PLL}$ and $v_{E\text{-}PLL}$ produced by the E-PLL in steady-state (second test case).

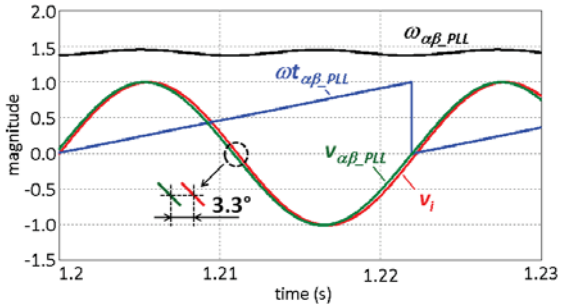

Fig. 11. Input signal (v_i) and control signals $\omega t_{\alpha\beta\text{-}PLL}$, $\omega_{\alpha\beta\text{-}PLL}$ and $v_{\alpha\beta\text{-}PLL}$ produced by the $\alpha\beta$-PLL in steady-state (second test case).

In the third test case, it is imposed a disturbance such that the input signal (v_i) presents different waveforms before and after the transient. Before the transient, the input signal presents a waveform similar to the current drained by a diode bridge rectifier with DC-load composed by a RC parallel circuit. This is a typical current waveform of many types of single-phase home and office nonlinear loads, which presents harmonics of various orders, especially 3rd order harmonics. The signal used in this test case presents a THD of 73%, and its fundamental component ($v_{i1}(t)$) is given by:

$$v_{i1}(t) = 0.5 \cdot sin\,(100\,\pi\,t - 21.5°) \quad (t < 1.0\ s) \tag{30}$$

In Fig. 12 is illustrated the input signal (v_i) together with the control signals ωt_{E_PLL}, ω_{E_PLL} and v_{E_PLL}, at the time period before the occurrence of this disturbance. Due to the harmonic components in the input signal, the angular frequency ω_{E_PLL} is composed by average plus oscillating components. Nevertheless, as already observed in Fig. 2, the E-PLL presents an integrator at the output of the PI controller which can be considered as a low pass filter, and as a consequence, the THD of v_{E_PLL} is minimized to 2.7%.

In Fig. 13 is showed the input signal (v_i) together with the control signals $\omega t_{\alpha\beta\_PLL}$, $\omega_{\alpha\beta\_PLL}$ and $v_{\alpha\beta\_PLL}$, at the time period before the waveform modification. In this case, the angular frequency $\omega_{\alpha\beta\_PLL}$ is also composed by average and oscillating components. However, in comparison with ω_{E_PLL}, the oscillating components in $\omega_{\alpha\beta\_PLL}$ are lower, and as a consequence, the THD observed at $v_{\alpha\beta\_PLL}$ corresponds to only 1.3%. Thus, in this third test case, it can be concluded that the $\alpha\beta$-PLL is less sensitive to harmonic distortion in comparison with the E-PLL.

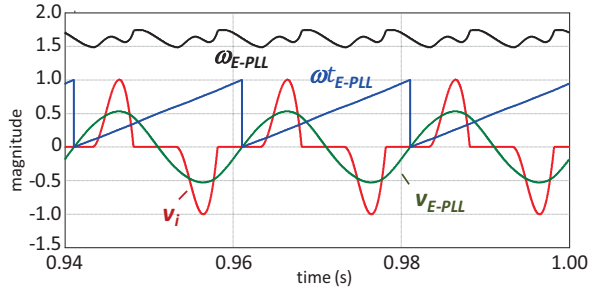

Fig. 12. E-PLL control signals ωt_{E_PLL}, ω_{E_PLL} and v_{E_PLL} before the waveform modification of the input signal (v_i) (third test case).

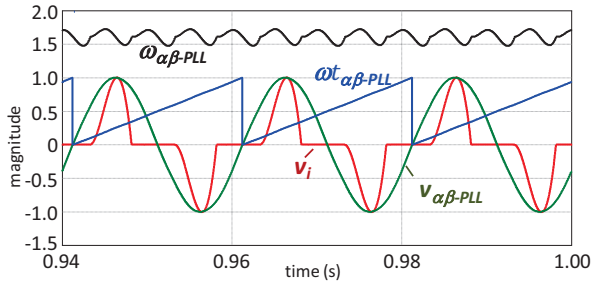

Fig. 13. $\alpha\beta$-PLL control signals $\omega t_{\alpha\beta\_PLL}$, $\omega_{\alpha\beta\_PLL}$ and $v_{\alpha\beta\_PLL}$ before the waveform modification of the input signal (v_i) (third test case).

As it can be noted in Fig. 14 and Fig. 15, at the time instant $t = 1.0$ s the waveform of the input signal is modified, such that its THD is reduced from 73% to 28%, presenting a fundamental component equal to:

$$v_{i1}(t) = 0.8 \cdot sin\,(100\,\pi\,t + 10.4°) \quad (t \geq 1.0\ s) \tag{31}$$

According to the waveforms illustrated in Fig. 14, after the time transient when the input signal has its waveform modified, the E-PLL takes almost 5 cycles to track the new fundamental component. After this time interval, the output signal (v_{E_PLL}) is tracked with the fundamental component of the input signal (v_{i_fund}), presenting a THD equal to 1.7%. An alternative to reduce this time interval consists in increasing the gain considered in the amplitude loop, which can be made if it is acceptable to have a higher harmonic distortion at v_{E_PLL}.

The last simulation result is shown in Fig. 15, with the $\alpha\beta$-PLL being submitted to this same disturbance. Based on the control signal $\omega_{\alpha\beta\text{-}PLL}$, it takes approximately 2 cycles of $v_{\alpha\beta\text{-}PLL}$ to be synchronized with v_{i_fund}, presenting a THD equal to 1.3%. Based on this third test case, it can be considered that the $\alpha\beta$-PLL is more suitable to be employed in active power conditioners to provide dynamic compensation. Fig. 16 shows the $\alpha\beta$-PLL phase-angle for different frequency deviations from 50 Hz to 45 Hz with increments of 0.5 Hz.

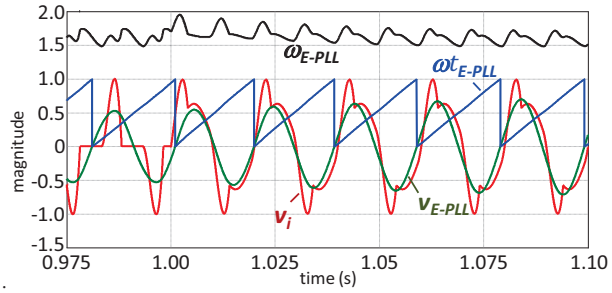

Fig. 14. E-PLL control signals ωt_{E_PLL}, ω_{E_PLL} and v_{E_PLL} when the waveform of the input signal (v_i) is modified (third test case).

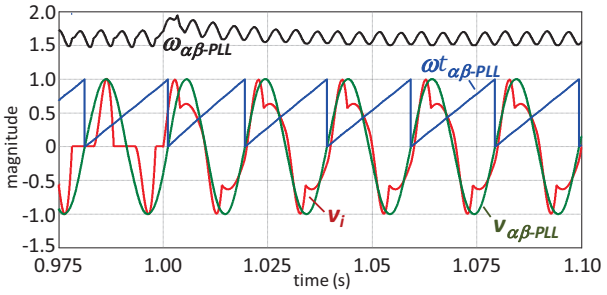

Fig. 15. $\alpha\beta$-PLL control signals $\omega t_{\alpha\beta\_PLL}$, $\omega_{\alpha\beta\_PLL}$ and $v_{\alpha\beta\_PLL}$ when the waveform of the input signal (v_i) is modified (third test case).

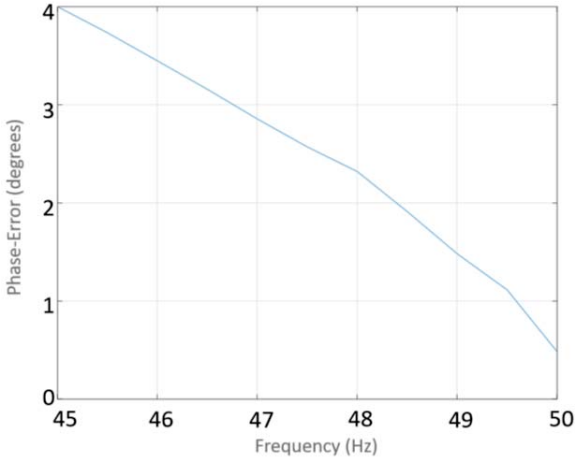

Fig. 16. $\alpha\beta$-PLL phase-angle for different frequency deviations from 50 Hz to 45 Hz with increments of 0.5 Hz.

V. Experimental Results

In order to obtain useful experimental results to assess the performance of both E-PLL and $\alpha\beta$-PLL algorithms, responding to different transients and disturbances in their

input signal, a personal computer was used to store a look-up table with data points achieved from the simulation software. These values were transmitted at a constant rate of 100 kSPS to a 16 bits D/A (Digital to Analog) converter of a data acquisition board NI PCI-6229 from *National Instruments*. The conversion result was then fed to the internal A/D (Analog to Digital) converter of a DSP TMS320F28335 from *Texas Instruments*, where the PLL algorithms were implemented. The DSP was connected to a 4 channel 12 bits D/A, allowing real time analysis with the capture of the PLL waveforms using a digital scope. This implementation allows subjecting both PLLs to voltage sags, phase shifts, frequency deviations, and also to distorted signals, similar to the ones applied in the simulation analyses. All the calculations of the PLL algorithms, implemented in the DSP, are done based on the IEEE 32 bits floating point format. Using this hardware-setup where implemented three test cases similar to those observed in the simulation results.

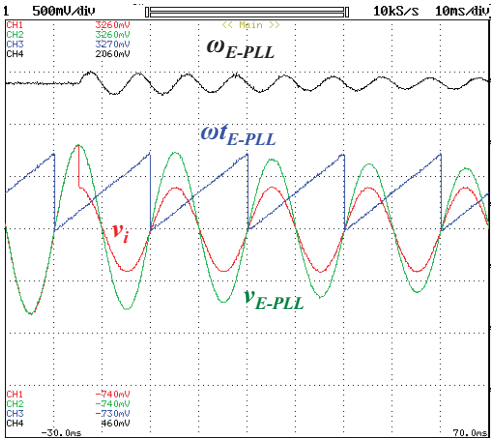

Fig. 17 Input signal (v_i) and control signals $\omega t_{E\text{-}PLL}$, $\omega_{E\text{-}PLL}$ and $v_{E\text{-}PLL}$ produced by the E-PLL in response to a voltage sag (first test case).

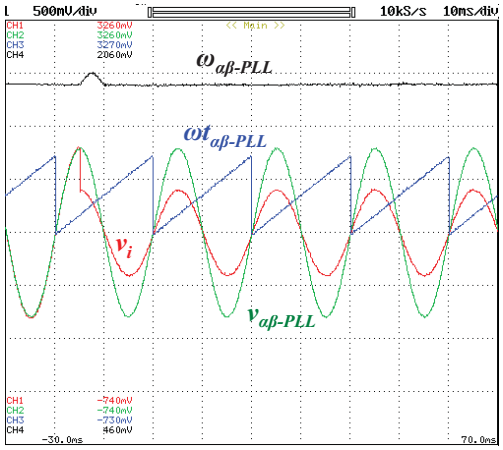

Fig. 18 Input signal (v_i) and control signals $\omega t_{\alpha\beta\text{-}PLL}$, $\omega_{\alpha\beta\text{-}PLL}$ and $v_{ab\text{-}PLL}$ produced by the $\alpha\beta$-PLL in response to a voltage sag (first test case).

The experimental results involving the first test case are presented in Fig. 17 and Fig. 18. In Fig. 17 is illustrated the input signal (v_i) together with the control signals ωt_{E_PLL}, ω_{E_PLL} and v_{E_PLL} for the E-PLL during the time interval in which a sag occurs. As expected, when the disturbance occurs, the control signal $\omega_{E\text{-}PLL}$ presents an oscillatory component at 2ω, while the new amplitude is not reached. In Fig. 18 is illustrated the input signal (v_i) together with the control signals $\omega t_{\alpha\beta\_PLL}$, $\omega_{\alpha\beta\_PLL}$ and $v_{\alpha\beta\_PLL}$ for the $\alpha\beta$-PLL under the same conditions. As expected, and previously observed through the simulation results, the $\alpha\beta$-PLL responds quickly to the disturbance, reaching its steady state condition in 5.1 ms.

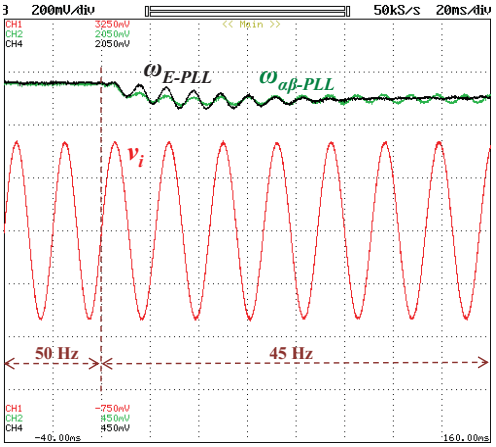

Fig. 19. Angular frequencies ($\omega_{E\text{-}PLL}$ and $\omega_{\alpha\beta\text{-}PLL}$) for both PLLs tracking an input signal (v_i) with a frequency drop from 50 Hz to 45 Hz (second test case).

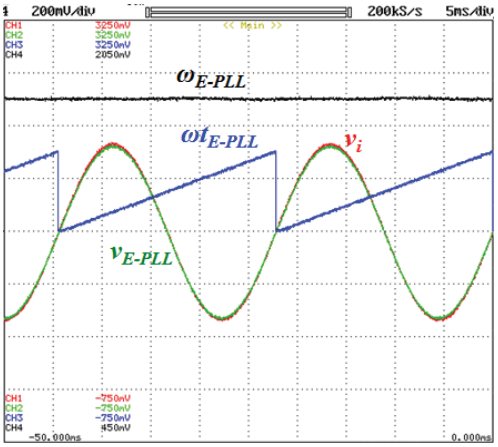

Fig. 20. Input signal (v_i) and control signals $\omega t_{E\text{-}PLL}$, $\omega_{E\text{-}PLL}$ and $v_{E\text{-}PLL}$ produced by the E-PLL in steady-state (second test case).

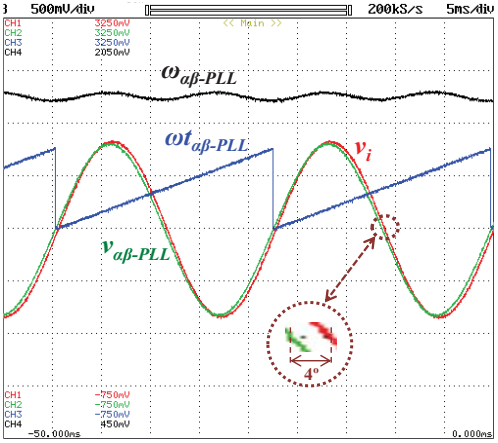

Fig. 21. Input signal (v_i) and control signals $\omega t_{\alpha\beta\text{-}PLL}$, $\omega_{\alpha\beta\text{-}PLL}$ and $v_{\alpha\beta\text{-}PLL}$ produced by the $\alpha\beta$-PLL in steady-state (second test case).

The responses of both PLL circuits considering a frequency deviation disturbance (second test case) are presented in Fig. 19, Fig. 20 and Fig. 21. In Fig. 19 is shown the angular frequency of both PLL circuits at the time transient when the input signal presents a frequency drop from 50 Hz to 45 Hz. As already observed in Fig. 9, the control signal ω_{E_PLL} presents an oscillatory component at 2ω while the new angular frequency is not reached and, on the other hand, $\omega_{\alpha\beta\_PLL}$ remains with this oscillatory component at 2ω, once the input signals of the $\alpha\beta$-PLL are no more 90º shifted from each other.

The remaining results of this second test case are shown in Fig. 20, and Fig. 21, respectively, for the E-PLL and $\alpha\beta$-PLL circuits under steady-state condition. At this condition, the output signal produced by the E-PLL (v_{E_PLL}) is synchronized with the input signal (v_i), whereas the output signal produced by the $\alpha\beta$-PLL (v_{E_PLL}) is 4º delayed from v_i. In this test case, both output signals produced by these PLL circuits present low THD (less than 0.5%). From these results, it can be concluded that in weak power systems, where considerable frequency deviations may occur, the E-PLL is more suitable to be used in comparison with the $\alpha\beta$-PLL.

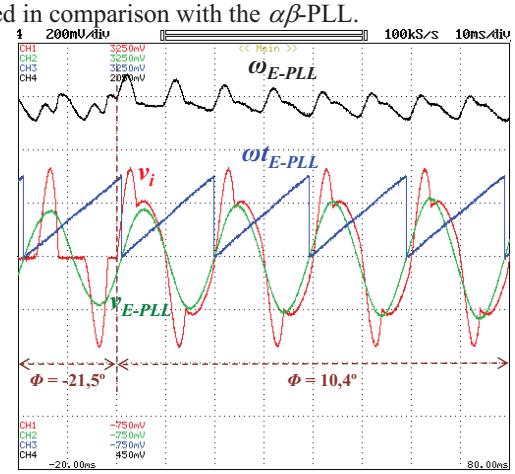

Fig. 22 E-PLL control signals $\omega t_{E\text{-}PLL}$, $\omega_{E\text{-}PLL}$ and $v_{E\text{-}PLL}$ when the waveform of the input signal (v_i) is modified (third test case).

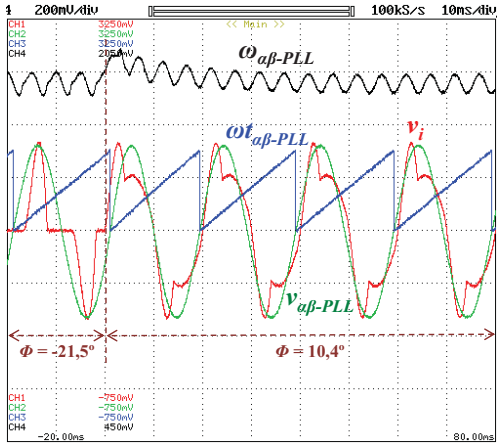

Fig. 23 $\alpha\beta$-PLL control signals $\omega t_{\alpha\beta\text{-}PLL}$, $\omega_{\alpha\beta\text{-}PLL}$ and $v_{\alpha\beta\text{-}PLL}$ when the waveform of the input signal (v_i) is modified (third test case).

The experimental results illustrated in Fig. 22 and Fig. 23 correspond to the third test case, where the waveform of the input signal is abruptly modified. In conformity with the simulation results introduced in Fig. 14 and Fig. 15, the experimental results show that the $\alpha\beta$-PLL presents a faster response in synchronizing with the input signal. The signals produced by both PLLs present a THD below 2%, as expected based on the applied internal parameters.

VI. Results Summary

In this paper the E-PLL and $\alpha\beta$-PLL synchronizing circuits for single-phase power systems were assessed in three different test cases. The simulation and experimental results, obtained from these tests, are summarized in the next tables.

Table I presents a summary of the obtained results from the first test case, where the input signal of the E-PLL and $\alpha\beta$-PLL schemes experience a 50% sag (i.e., the amplitude of the input signal suffers an abrupt drop to 50% of its nominal value). In the first row are presented the steady-state results for both PLL schemes in response to a unitary amplitude 50 Hz sinusoidal signal, which corresponds to the center frequency of the PLLs. Based on the obtained results, it is possible to observe that both PLLs perfectly track the input signal. The phase error of the two PLLs is almost zero, and the output signal is almost a perfect sine wave, presenting a very-low THD (close to 0.4%). The second row summarizes the behavior of the PLLs in response to a disturbance in the input signal, which corresponds to an amplitude drop to 50% of the nominal value. In this test case, the $\alpha\beta$-PLL takes 5.1 ms to reach the steady-state again, whereas the E-PLL takes 162 ms. The maximum errors in terms of frequency and phase, during the transient are very similar for both PLLs. According to the results shown in the third row, which summarizes the steady-state response of the PLLs to the input signal with 50% of the nominal amplitude, it is possible to conclude that both PLLs correctly track the input signal, producing an output signal with a very low THD, and without phase error.

Table II presents a summary of the obtained results from the second test case, where the input signal of the E-PLL and $\alpha\beta$-PLL schemes experience an abrupt frequency deviation. In the first row are presented the steady-state results for both PLLs in response to a 50 Hz sinusoidal signal with unitary amplitude, and as expected, the obtained results were the same of the previous test under the same conditions (first row of Table I). The second row condenses the behavior of the PLLs in response to a frequency drop from 50 Hz to 45 Hz. The E-PLL takes 115 ms to be synchronized with the input signal, whereas the $\alpha\beta$-PLL takes 94 ms. Also the maximum errors in terms of frequency and phase, during the transient, are slightly better to the $\alpha\beta$-PLL than to the E-PLL. In the third row, it is shown the steady-state response of the PLLs to a 45 Hz sinusoidal signal. In this case, the E-PLL perfectly tracks the input signal, whereas the $\alpha\beta$-PLL presents a peak-to-peak phase error of 2º and an average phase error of -4º. The output signals, for both PLLs, present a small THD (lower than 0.5%).

Table III summarizes the results obtained in the third test case, where the E-PLL and $\alpha\beta$-PLL synchronizing circuits are submitted to highly distorted input signals, which correspond to typical current signals observed in single-phase loads. The first row of this table presents the steady-state response of these PLL circuits to a highly distorted signal, with a THD of 73%. Both PLLs correctly track the fundamental component of the input signal, with the $\alpha\beta$-PLL presenting better results. The peak-to-peak phase error and the THD of the output signal are smaller for the $\alpha\beta$-PLL than for the E-PLL, showing that the $\alpha\beta$-PLL is more immune to harmonics. The results presented in the second row refer to an abrupt change in the waveform of the input signal. The phase of the fundamental component of the input signal changes from -21.5º to 10º. It is observed that the $\alpha\beta$-PLL converges a little faster than the E-PLL. Finally, the third row presents the steady-state response of both PLLs considering an input signal with a THD of 29%. It is possible to note that both PLLs properly track the fundamental of the input signal, however with the $\alpha\beta$-PLL presenting better results, again.

TABLE I
Summary Results: Sinusoidal Signal and 50% Sag

First Test Case		E-PLL	$\alpha\beta$-PLL
Sinusoidal signal 100% amplitude (Steady-state)	Peak-to-peak phase error	0º	0º
	Average phase error	0º	0º
	THD of the output signal	0.4%	0.4%
Amplitude drop from 100% to 50% (Transient)	Settling time	162 ms	5.1 ms
	Maximum frequency during the transient	54 Hz	54 Hz
	Maximum phase error during the transient	0.23º	0.24º
Sinusoidal signal 50% amplitude (Steady-state)	Peak-to-peak phase error	0º	0º
	Average phase error	0º	0º
	THD of the output signal	0.4%	0.4%

TABLE II
Summary Results: Sinusoidal Signal and Frequency Drop

Second Test Case		E-PLL	$\alpha\beta$-PLL
Sinusoidal signal at 50 Hz (Steady-state)	Peak-to-peak phase error	0º	0º
	Average phase error	0º	0º
	THD of the output signal	0.4%	0.4%
Frequency drop from 50 Hz to 45 Hz (Transient)	Settling time	115 ms	94 ms
	Minimum frequency during the transient	41 Hz	43 Hz
	Maximum phase error during the transient	25º	18º
Sinusoidal signal at 45 Hz (Steady-state)	Peak-to-peak phase error	0º	2º
	Average phase error	0º	-4º
	THD of the output signal	0.3%	1%

It is important to highlight that, for these three test cases, the internal PI parameters of the E-PLL and $\alpha\beta$-PLL were kept constant (k_p = 100 and k_i = 3,000), and were selected to a middle term between response time and tolerance to high

distortion in the input signal. Thus, the results presented in this paper for the E-PLL and $\alpha\beta$-PLL cannot be fairly compared with other PLLs observed in the literature, since they were tuned to deal only with low distorted input signals.

In Table IV are presented the necessary memory requirements to implement the E-PLL and $\alpha\beta$-PLL synchronizing circuits in a DSP, indicating the variables types, size and quantity used in each algorithm. The platform used for these assessments was the TMS320F28335, a floating point 32-bit DSP. The input signal is sampled at a fixed rate of 32 kS/s, which gives 640 conversions per electrical grid cycle, at 50 Hz. In the field of memory requirements, the $\alpha\beta$-PLL uses vaster resources due to the scheme used to create the signal $u_{i\beta'}(t)$ lagged 90° from the input signal. This was made by saving 160 samples (corresponding to a quart of one grid cycle at 50 Hz), acquired by the A/D converter of the DSP, in a 16-bit integer array, which its 160 positions are used to generate the fictitious $u_{i\beta'}(t)$.

In order to compare the processing speed of the E-PLL and $\alpha\beta$-PLL, it was used a procedure that consisted in setting a GPIO pin of the DSP at the beginning of the algorithm, and clearing it at the end of the algorithm, for both PLLs. It was measured a similar value of 1.4 μs of processing time for both synchronizing circuits, which corresponds to a reduced processing time.

TABLE III
SUMMARY RESULTS: HIGHLY DISTORTED SIGNALS AND PHASE JUMP

THIRD TEST CASE		E-PLL	$\alpha\beta$-PLL
Current signal with THD% = 73% (Steady-state)	Peak-to-peak phase error	3.4º	2.2º
	Average phase error	0º	0º
	THD of the output signal	2.3%	1.3%
Phase jump from -21.5º to 10.4º (Transient)	Settling time	130 ms	110 ms
	Minimum frequency during the transient	44 Hz	37 Hz
	Maximum phase error	12º	9º
Current signal with THD% = 29% (Steady-state)	Peak-to-peak phase error	2.2º	1.7º
	Average phase error	0º	0º
	THD of the output signal	1.7%	1.3%

TABLE IV
SYNCHRONIZING CIRCUITS MEMORY REQUIREMENTS

Variable Type	Required Memory Space	
	E-PLL	$\alpha\beta$-PLL
Floating point	(15 x 32) = 480 bits	(12 x 32) = 384 bits
Integer array	-	(160 x 16) = 2,560 bits
TOTAL	480 bits	2,944 bits

VII. CONCLUSIONS

This paper makes a comparison between two distinct PLL circuits for single-phase applications: the E-PLL, and a single-phase PLL implemented in α-β coordinates modified for single-phase applications, the $\alpha\beta$-PLL. This comparison is reasoned in both simulation and experimental results, and by exploring the linear model of the PLLs through a mathematical analysis.

It is shown, in section III, that the E-PLL and $\alpha\beta$-PLL present some differences in their linear models. Based on this analysis it was possible to note that the E-PLL presents a transient oscillatory component in 2ω, even when the input signal is only composed by a fundamental component. Such characteristic is not present in the $\alpha\beta$-PLL, as it is shown through mathematical analysis, and is reinforced through simulation and experimental results.

Simulation and experimental results provide some insight about the functioning of these two PLLs, as well as some comparison basis. It was concluded that the $\alpha\beta$-PLL has a faster response to phase-shifts. Both PLLs present similar response to input signals with harmonic distortion. The $\alpha\beta$-PLL presents some error in frequency tracking due to the scheme used in the creation of the fictitious α-β coordinates. Nevertheless, this problem may be overcome by a dynamic adjustment of the number of samples per grid cycle, as introduced in [39]. Considering that exist very restricting norms, as for example, the European norm EN 50160 [41], which present a very strict regulation about frequency deviations, this negative aspect observed at the $\alpha\beta$-PLL can be neglected. Indeed, frequency deviations over 1% are only acceptable in islander electrical grids. For all of the other disturbances applied to the input signal, the $\alpha\beta$-PLL presented a faster transient time interval to reach the steady-state condition, with the produced signal presenting a lower harmonic distortion in comparison with the one produced by E-PLL (see Table III).

It is also presented an evaluation of the computational performance of these two PLLs, namely regarding memory requirements and processing times. Both PLLs present similar reduced processing times, however the $\alpha\beta$-PLL presents higher memory needs.

In an overall analysis, it can be verified that the single-phase $\alpha\beta$-PLL presents a good performance, showing low sensitive for most of the disturbances applied to the input signal, which makes it very attractive to single-phase Power Quality applications.

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