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A Three-Phase Four-Wire Unified Power Quality Conditioner Without Series Transformers

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***Abstract* – This work presents a topology for a Unified Power Quality Conditioner (UPQC), without series transformers, connected to a three-phase four-wire electrical grid. Based on the proposed power topology, the UPQC is able to compensate unbalanced-and harmonic-components, power factor and short-duration voltage variations (voltage sag/swell). In other words this UPQC consists in a universal solution capable to mitigate most power quality problems in an electrical installation. The applied control algorithms are based on instantaneous power definitions (active and non-active currents), together with a robust synchronizing circuit (PLL), to detect the phase angle of the fundamental positive-sequence component of the system voltage. A trustworthy model of the proposed UPQC was investigated in order to verify its performance under power quality problems observed at the load currents and system voltages.**

***Index Terms*—UPQC topology, power quality, custom power conditioners, instantaneous active and non-active currents.**

I. INTRODUCTION

TRANSFORMERLESS power conditioners have been widely proposed as dynamic voltage restorers [1]-[4], static compensators [6]-[9], hybrid active filters [10], interface with renewable energy sources [11]-[14] and to connect active power conditioners in medium voltage systems [5]-[9]. Particularly the efforts directed to avoid employing power transformers to connect series conditioners with the power grid brings a considerable improvement. Indeed, power transformers are not suitable to deal with high-frequency harmonic components. Usually, when transformers are employed together with power converters, they need to be oversized due to these harmonic components that they are submitted.

However, converters connected in series with the power grid, without power transformers, present some restrictions to be employed. In fact, the series connection requires that the converter be capable to produce controlled voltages without causing short-circuits between phases. The applied alternative comprehends in employing three single-phase converters, where each converter presents its own dc-link. In this configuration, unless the dc-link is composed by energy sources, it is not possible to establish an energy exchange between the phases, which makes unfeasible the compensation of the unbalanced components.

The same drawback occurs with UPQC conditioners without series transformers. These conditioners, when employed in three-phase electrical grids, are composed by single-phase back-to-back structures and, moreover, the shunt converter is connected together with transformers. These transformers are required to avoid short-circuit between the phases. The UPQC topologies without series transformers, introduced in literature [5][6], are only analyzed in three-phase three-wire power grids, in a scenario presenting only balanced loads. This characteristic was necessary, since they are not suitable to compensate unbalanced components since there is no exchange of energy between the phases.

Thus, this paper proposes a topology for a UPQC without series transformers, which is able to compensate unbalanced-and harmonic-components in a three-phase four-wire electrical grid. As illustrated in Fig. 1, the UPQC topology is comprehended by 3 power modules, where each module presents a back-to-back converter. The shunt converter consists on a two-level four-branch topology, which enables the energy exchange between the phases. These aspects consist of the main contribution of this work. Simulations involving the proposed UPQC in a three-phase four-wire electrical grid are presented in order to observe its performance under power quality disturbances.

II. SYSTEM CONFIGURATION

According to the UPQC electrical diagram, illustrated in Fig. 1, i_{La}, i_{Lb}, i_{Lc} are the load currents, i_{Fa_k}, i_{Fb_k}, i_{Fc_k}, i_{Fn_k} (for k = 1,2,3) the shunt-converter currents, and i_{Sa}, i_{Sb}, i_{Sc} the compensated system currents. The system voltages are represented by v_{Sa}, v_{Sb}, v_{Sc}, the series-converter voltages by v_{Fa}, v_{Fb}, v_{Fc}, and the compensated load voltages by v_{La}, v_{Lb}, v_{Lc}.

The load is composed by a three-phase 6-pulse diode rectifier plus a single-phase diode rectifier connected between phase "c" and the neutral wire. It demands a 20 kVA with a 0.7 power factor. The system impedance is constituted by inductances of 0.8 mH, resulting in a short-circuit power equal to 40 p.u.

As highlighted in Fig. 1, the UPQC topology is composed by 3 back-to-back modules. Each one of them consists in a two-level four-branch topology (connected in shunt with the power grid), together with a single-phase full-bridge topology (connected in series with the power grid). The shunt converters present a 10 kHz switching frequency (pwm switching technique), whereas the series converters a 20 kHz switching frequency (unipolar-pwm switching technique). Each one of these back-to-back converters presents their own dc-link, with an 11200 uF capacitor employed as the energy store element. The dc-link voltages are represented in Fig. 1 as v_{dc1}, v_{dc2}, and v_{dc3}.

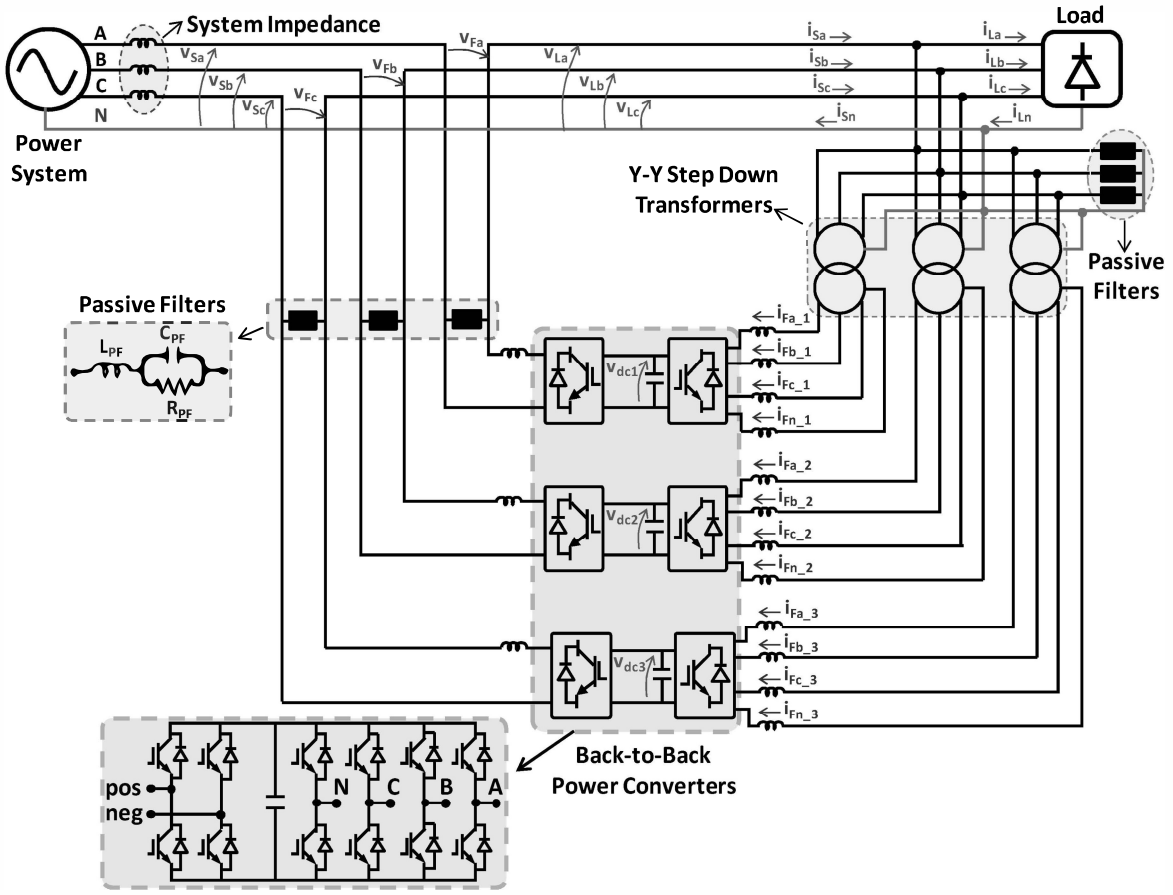

Fig. 1 – Electrical diagram of the proposed three-phase four-wire UPQC without series transformers.

Three 10 kVA three-phase step-down (Y-Y) transformers (230 V//57.5 V) are connected together with the shunt converters, providing galvanic isolation between the power converters and the electrical grid. As a consequence, short-circuits at the series conditioner terminals are avoided, allowing them to be connected without transformers. Considering a UPQC properly operation, these transformers are submitted to voltages that are balanced, regulated and with a very low harmonic distortion.

Passive filters (RLC circuits), are applied to minimize high-frequency switching harmonics generated by the converters. The employed topology of these passive filters is highlighted in Fig. 1. Based on their frequency response, illustrated in Fig. 2 and Fig. 3, they were tuned according to the switching frequency of the UPQC converters. The three-phase passive filter, employed together with the shunt converter, is connected at high-voltage terminal of the transformers, and are comprehended by L_{pf} (0.1 mH), R_{pf} (100 Ω) and C_{pf} (2.5 μF). On the other hand, three single-phase passive filters are connected at the terminals of the series converters, and are comprised by L_{pf} (0.05 mH), R_{pf} (100 Ω), C_{pf} (1.25 μF).

In sequence, it is presented the control algorithms applied to determine, in real time, the reference voltages and currents to be produced by the series-and shunt-converters.

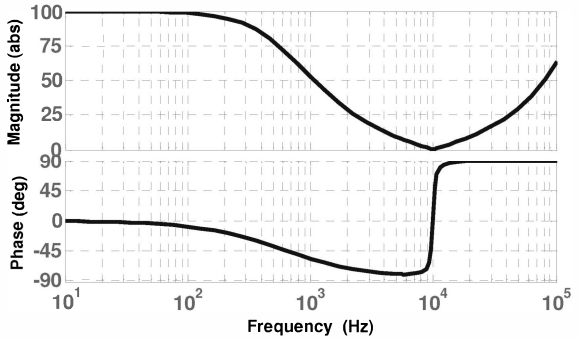

Fig. 2 – Frequency response of the passive filters employed together with the shunt converters.

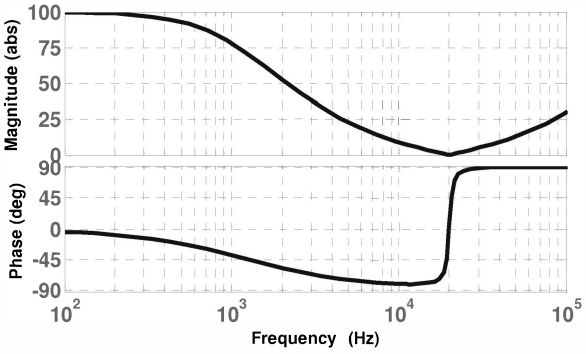

Fig. 3 – Frequency response of the passive filters employed together with the series converters.

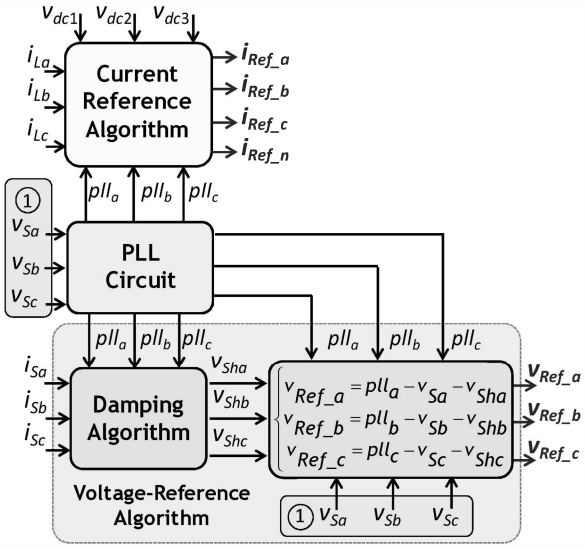

Fig. 4 – Block diagram of the UPQC control algorithms.

III. CONTROL ALGORITHMS

A block diagrams involving all of the UPQC control algorithms is illustrated in Fig. 4. These control algorithms are derived from the concepts involving the active and non-active current components, together with a synchronizing circuit PLL (Phase-Locked-Loop) [15].

The PLL circuit uses the system voltages (v_{Sa}, v_{Sb}, v_{Sc}) as inputs and its outputs are the signals pll_a, pll_b and pll_c. These calculated output signals have sinusoidal waveforms with unitary magnitude, which are in phase with the fundamental positive-sequence component of the system voltages.

The control block "Voltage-Reference Algorithm" calculates the compensating voltage references v_{Ref_a}, v_{Ref_b}, and v_{Ref_c} that are synthesized by the series converter of the UPQC. The inputs of this block are the PLL output signals, the supply voltages v_{Sa}, v_{Sb}, v_{Sc}, and the source currents i_{Sa}, i_{Sb}, i_{Sc}.

The control block "Current-Reference Algorithm" determines the compensating current references i_{Ref_a}, i_{Ref_b}, i_{Ref_c} and i_{Ref_n} that are used in the PWM control of the shunt converter. The inputs of this control block are the load currents i_{La}, i_{Lb}, i_{Lc}, the dc-link v_{dc1}, v_{dc2}, v_{dc3} and the PLL output signals. These current references carry the information needed to properly generate the shunt-conditioner currents i_{Fa_k}, i_{Fb_k}, i_{Fc_k}, and i_{Fn_k}, for k = 1, 2, 3, which compensate the load currents.

A. *Current-Reference Algorithm*

The control block "Current-Reference Algorithm" (Fig. 5) is responsible for calculating the compensating current references to be produced by the shunt converter of the UPQC. The main objective of the shunt converter is to compensate the non-active current and harmonics of the load current, and keep the dc-link voltages regulated. Considering the 3 shunt converters and the voltage relations of the transformers, the compensating current references must be multiplied by a factor equal to 4/3, as indicated in Fig. 5.

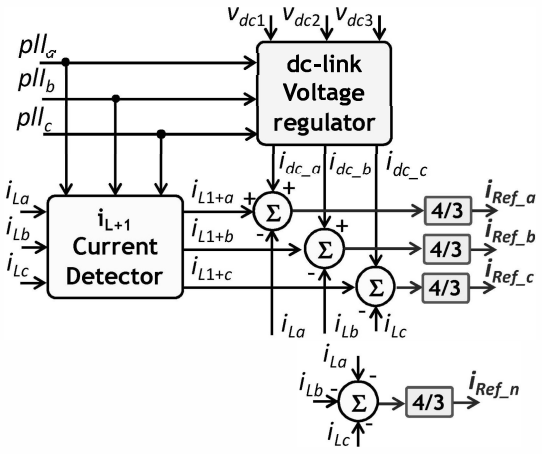

Fig. 5 – Block diagram "Current-Reference Algorithm".

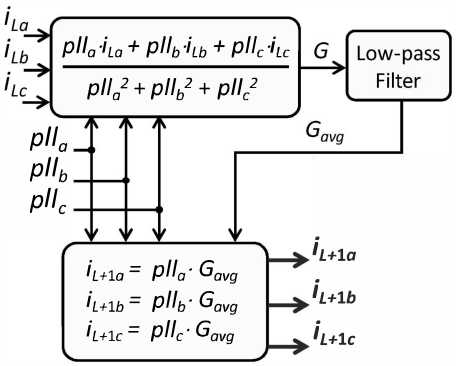

Fig. 6 – Block diagram "i_{L+1} Current Detector".

The control signals i_{dc_a}, i_{dc_b}, i_{dc_c} are determined by the control block "DC-Link Voltage Controller" (Fig. 5). Basically these control signals correspond to sinusoids, presenting only fundamental positive-sequence component, that are in phase or in counter-phase with the voltages. They force the shunt converters to draw energy from the power system to compensate for losses and to keep the dc-link capacitors voltages regulated.

The fundamental active current of the load, represented in Fig. 5 and in Fig. 6 as i_{L1+a}, i_{L1+b}, i_{L1+c}, corresponds to the fundamental positive-sequence component of the load current that is in phase with the load voltage. These current components are determined through the control block "i_{L+1} Current Detector", illustrated in Fig. 6. It is worth to comment that these current components, together with the compensated load voltages, do not produce zero-sequence power. Thus, they do not carry any zero-sequence component and, as a consequence, the reference neutral current (i_{Ref_n}) can be directly determined from the load currents as indicated in Fig. 5.

B. *Voltage-Reference Algorithm*

The control algorithm to determine the compensating voltage references is illustrated in Fig. 4 and Fig. 7. In this algorithm, the calculation of the amplitude of the fundamental positive-sequence voltage is suppressed. Indeed, If the system voltages are normalized such that an unity amplitude

represents its nominal value, this normalized voltage signal can be directly compared with the PLL outputs pll_a, pll_b, pll_c, to achieve the compensating voltage references. In this case, the difference between the PLL outputs and the normalized voltages includes also sags or swells, as well as unbalances and distortions, which may be affecting the supply voltage.

Due to possible resonance phenomena involving the system impedance together with the passive filters, it is advisable to provide auxiliary damping method. This is the main reason for including a damping algorithm in the series converter controller, as shown in Fig. 7. The goal is to determine, in real time, the non-active current currents that may arise in the source currents (i_{Sa}, i_{Sb}, i_{Sc}) and force the series converter to apply a compensating voltage component in counter phase to these current components. In other words, the series active filter behaves as a "harmonic resistor" between the source and the load.

Therefore, the compensating voltage references calculated as shown in Fig. 4 forces the series converter of the UPQC to compensate all sags, swell, voltage unbalance and harmonics in the supply voltage, ensuring a high quality voltage to the load (right side of the UPQC). Additionally, it provides harmonic current damping to the whole system.

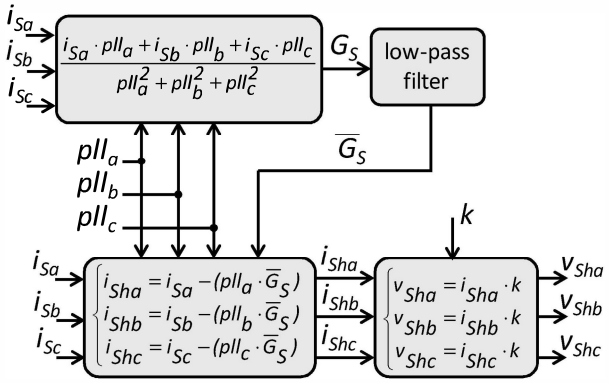

Fig. 7 – Block diagram "Damping Algorithm".

IV. SIMULATION RESULTS

A test case was conceived to analyze the performance of the proposed system through simulations. These simulations were carried out using PSCAD/EMTDC. The simulation interval was 1.5 s, with a fixed time step of 2.5 µs.

The simulation starts with the system voltages unbalanced and sinusoidal (without any distortions), and the loads are connected at $t = 0.1$ s. Initially both shunt-and series converters of the UPQC are turned off, with all of the power switches (IGBTs) opened. At t = 0.15 s, the shunt converters are connected with the power grid and, through the anti-parallel diodes, the dc-link capacitors are charged to 180 V, approximately. It is important to comment that, at this time, only the shunt converters are connected, since the series converters are bypassed through circuit breakers.

At $t = 0.2$ s the shunt converter starts switching, as illustrated in Fig. 8. At this time, the harmonic components of the system currents are compensated and the neutral current is decreased to zero. Initially these system currents present their amplitude above from what is expected. It occurs due to the shunt converters that are consuming active power to increase the dc-link voltages to their rated value of 300 V. Moreover, it can be seen that still remains an unbalance component, resulted from the unbalanced-components voltage drop at the passive components.

From the time period $0.25\text{ s} < t < 0.28$ s, the series converters are connected with the power grid and, at t = 0.3 s, they are turned on, as it can be seen in Fig. 9. As expected, when the series converters are turned on, the unbalanced components observed in the load voltages are entirely compensated.

Another simulation result involving the time transients when the shunt-and series-converters are turned on is showed in Fig. 10. As aforementioned explained, the compensated system currents, presents amplitude value above from what is expected. As just as the dc-link voltages reach their rated value, the amplitude of the system currents is decreased.

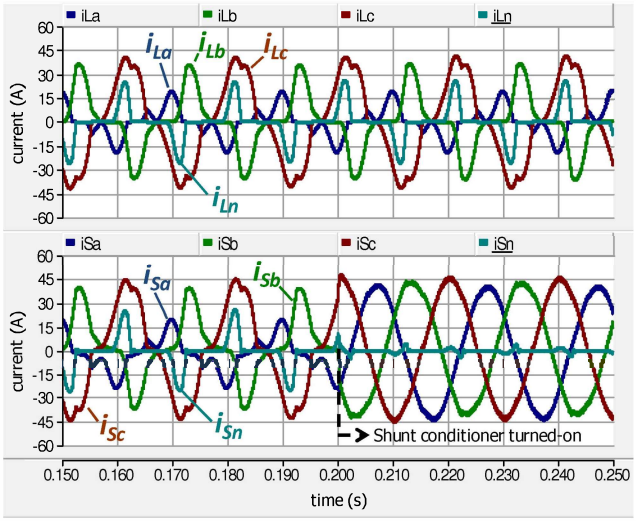

Fig. 8 – Load-and system-currents at the time transient when the shunt conditioner is turned-on.

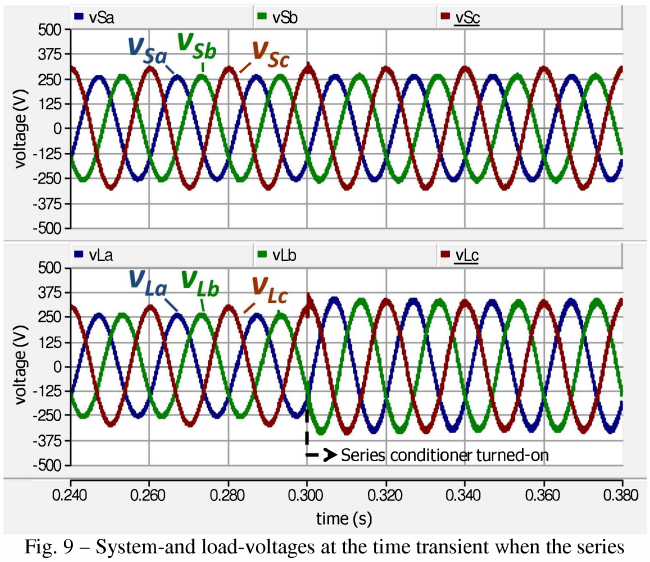

Fig. 9 – System-and load-voltages at the time transient when the series conditioner is turned-on.

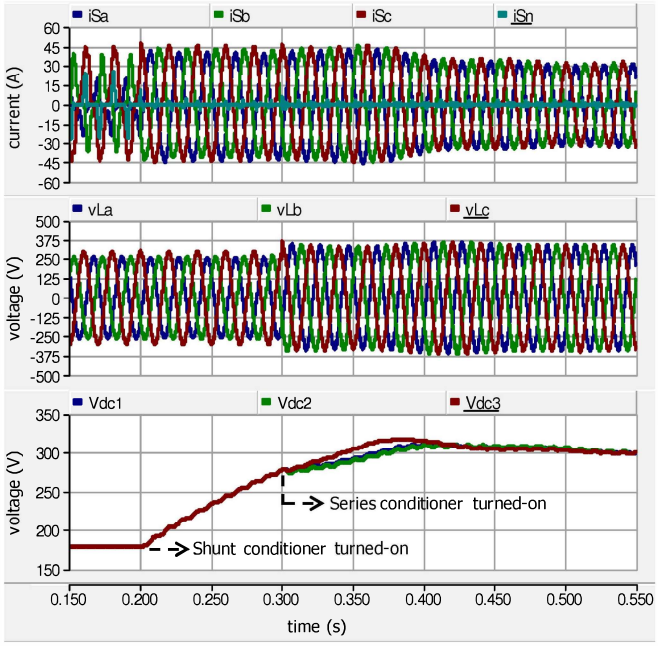

Fig. 10 – System currents, load voltages and dc-link voltages at the time transient when the series-and shunt-conditioners are turned-on.

Still analyzing the simulation results presented in Fig. 10, it can be noted that the amplitude of the load voltages increases to their rated value (peak value of 325 V) according to the increment of dc-link voltages to 300 V. This transient occurs for a 100 ms time period (from 300 ms to 400 ms). After this time transient, the system currents and the load voltages are balanced and regulated.

In Fig. 11 it is illustrated the system-and load-voltages at the time transient when a voltage sag occurs ($0.9\ \text{s} < t < 1.0\ \text{s}$). In this time period, the system voltages present a worst condition, with a negative-sequence component plus a 30% voltage sag. On the other hand, the compensated load voltages remain balanced. However, their amplitude starts decreasing and presents the lower value of 312 V (peak value) at $t = 0.95$ s. After that, the amplitude is increased to 325 V.

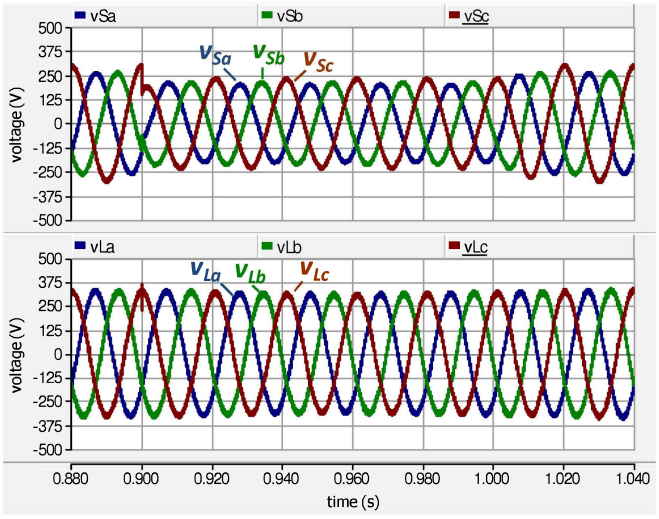

Fig. 11 – System-and load-voltages at the time period when a voltage sag occurs.

Another simulation result introduced to analyze the UPQC behavior at this time transient is presented in Fig. 12. Just as the series converters start compensating the voltage sag, there is a decrement of the dc-link voltages and, as a consequence, the active current drained by the shunt converters is increased from 30 A (peak value) to 45 A (peak value).

In Fig. 13 it is presented the system currents, load voltages and the dc-link voltages with the UPQC under steady state condition. At this time period the compensated voltages and currents are balanced and regulated at their nominal values, the harmonic components are minimized and the power factor is compensated. These aspects are highlighted in Table I and Table II.

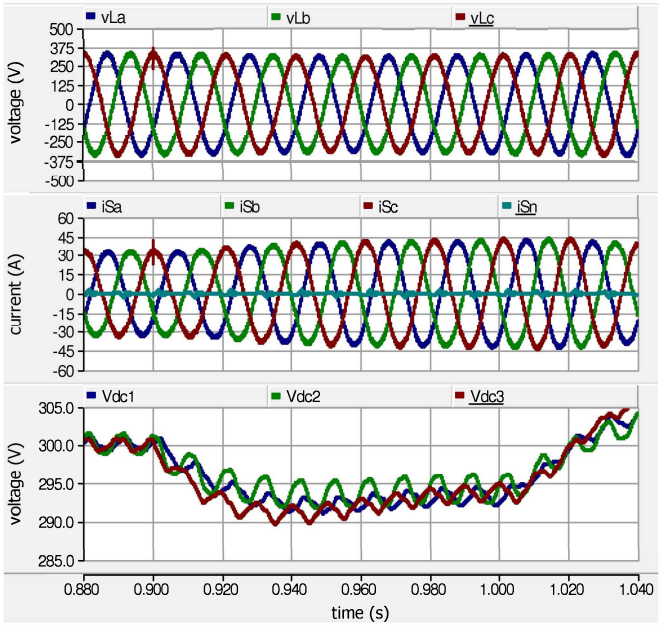

Fig. 12 – Load voltages, system currents and dc-link voltages at the time transient when a voltage sag occurs.

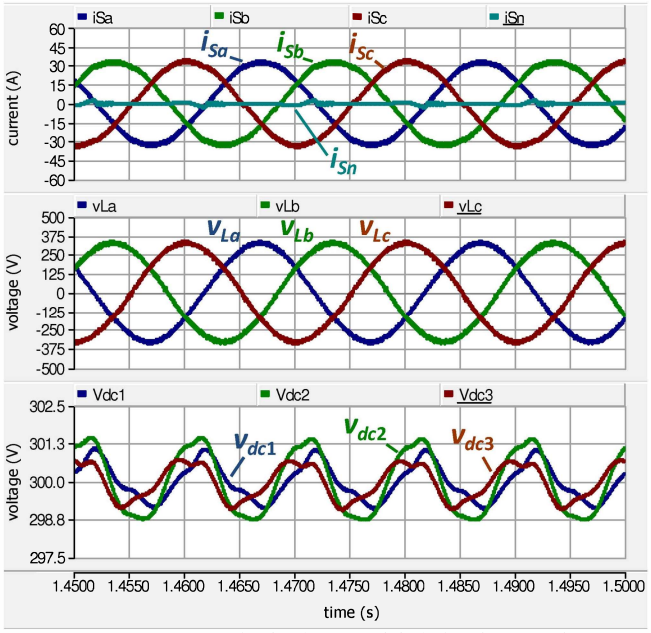

Fig. 13 – System currents, load voltages and dc-link voltages with UPQC operating under steady-state condition.

TABLE I

UPQC Performance – Load-and System-Currents

Load Currents		System Currents	
Amplitude (rms) fund. component	**THD (%)**	**Amplitude (rms) fund. component**	**THD (%)**
i_{La} = 10.05 A	i_{La} = 41.03%	i_{Sa} = 23.16 A	i_{Sa} = 1.60%
i_{Lb} = 20.64 A	i_{Lb} = 30.56%	i_{Sb} = 23.51 A	i_{Sb} = 2.32%
i_{Lc} = 23.01 A	i_{Lc} = 24.06%	i_{Sc} = 23.53 A	i_{Sc} = 2.33%
i_{Ln} = 7.56 A	i_{Ln} = 106%	i_{Sn} = 0.00 A	i_{Sn} = -----

TABLE II

UPQC Performance – Load-and System-Voltages

Load Voltages Amplitude (rms)	System Voltages Amplitude (rms)
v_{La} = 229.97 V	v_{Sa} = 182.40 V
v_{Lb} = 232.37 V	v_{Sb} = 183.76 V
v_{Lc} = 229.94 V	v_{Sc} = 211.80 V

V. CONCLUSIONS

A three-phase four-wire Unified Power Quality Conditioner (UPQC) was presented. The performance of this topology was analyzed through simulation results, in a three-phase four-wire electrical system with the load currents presenting harmonic-and unbalanced-components, and with the system voltages having unbalanced components. Moreover, it was introduced a 30% short-duration voltage sag.

In this scenario, the proposed UPQC presented a good performance, compensating the non-active components of the load currents plus the unbalanced components of the system voltages. However, improvements on the dynamics of the control algorithms are necessary to provide a better performance, especially during the occurrence of short-time disturbances.

The continuity of this work is directed to the research on new possible topologies for the back-to-back converters, on a deeper analysis of these control algorithms in a hardware-in-the-loop architecture, and in a possible development of a laboratorial prototype.

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