



Article

# Fabrication of Pre-Structured Substrates and Growth of CIGS Micro-Absorbers

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**Abstract:** Second-generation thin-film Cu(In, Ga)Se<sub>2</sub> (CIGS) solar cells are a well-established photovoltaic technology with a record power conversion efficiency of 23.6%. However, their reliance on critical raw materials, such as In and Ga, requires new approaches to reduce the amount of critical raw materials employed. The micro-concentrator concept involves the combination of thin-film photovoltaic technology with concentrator photovoltaic technology. This approach reduces the size of the solar cell to the micrometer range and uses optical concentration to collect sunlight from a larger area, focusing it onto micro solar cells. This work is devoted to the development of a process for manufacturing pre-structured substrates with regular arrays of holes with 200 and 250 μm diameters inside a SiO<sub>x</sub> insulating matrix. Subsequently, a Cu–In–Ga precursor is deposited by sputtering, followed by photoresist lift-off and the application of a Cu–In–Ga thermal annealing at 500 °C to improve precursor quality and assess pre-structured substrate stability under elevated temperatures. Finally, a two-stage selenization process leads to the formation of CIGS absorber micro-dots. This study presents in detail the fabrication process and explores the feasibility of a bottom-up approach using pre-structured substrates, addressing challenges encountered during fabrication and providing insights for future improvements in CIGS absorber materials.



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**Keywords:** CIGS; thin-film photovoltaics; micro-concentrator photovoltaics; sputtering; micro solar cell

## 1. Introduction

From 2021 to 2022, global photovoltaic installations increased from 175 GW to 240 GW, an overall growth of 65 GW. China dominated the market, installing 106 GW in 2022, corresponding to 44% of the global market. The European Union followed, installing 38.7 GW, led by Spain (8.1 GW), Germany (7.5 GW), Poland (4.9 GW), and the Netherlands (3.9 GW) [1]. For 2023, analysts project a substantial increase, estimating that photovoltaic installations could reach approximately 440 GW, double that of 2022 [2]. In 2021, crystalline-silicon (c-Si) photovoltaics represented a 95% share of production [3]. This technology achieved record efficiencies of 26.8% for mono-crystalline, 24.4% for multi-crystalline, and 27.6% for concentrator mono-crystalline [4,5]. To further enhance efficiency, new PV cell architectures like PERC (Passivated Emitter and Rear Cell) [6] have been explored. The main difference from a typical monocrystalline silicon cell lies in the inclusion of a passivation layer (a dielectric material) on the back cell's surface, promoting an increase in the efficiency of the PV solar cell. Thin-film solar cells have emerged as a compelling and cost-efficient alternative to c-Si. Recently, Keller et al. [7] reported a 23.6% record efficiency for non-concentrated (Ag,Cu)(In,Ga)Se<sub>2</sub> solar cells by introducing Ag into the absorber, implementing a Ga profile with a high concentration of Ga close to the back contact and lower concentration closer to the CdS buffer layer, and a post-deposition treatment with RbF. Ward et al. [8] presented CIGS concentrator cells grown by physical evaporation using a modified three-stage process, achieving an efficiency of 20.8% under 1 sun and a record

efficiency of 23.3% at 14.7 suns. Furthermore, CdTe solar cells have achieved an efficiency of 22.3% [5].

Concentrator photovoltaic (CPV) technology uses optical elements such as mirrors and/or lenses to concentrate light onto small and highly efficient solar cells [9], aiming to enhance overall performance. An ideal CPV system incorporates cost-efficient concentrating optics to reduce the active solar cell area, enabling the use of more expensive, high-efficiency solar cells [10]. Remarkable efficiencies of 47.6% at 665 suns [11] and 30.8% at 61 suns [12] have been achieved for four-junction (GaInP/GaInAs; GaInAsP/GaInAs) and flexible GaAs solar cells, respectively.

To enhance power conversion efficiency (PCE), reduce material usage, and lower costs, micro-concentrator photovoltaics (micro-CPVs) have been intensively investigated in recent years [10,13,14]. The micro-CPV concept consists of reducing the solar cells' lateral dimensions to the range of hundreds of micrometers, resulting in cell areas below  $1 \text{ mm}^2$  [14,15]. Thin-film micro-CPVs present several advantages over conventional CPVs and other technologies, including enhanced cell performance, material savings, efficient thermal management, reduced series resistance losses, and thinner modules [16]. Through simulations, Sadewasser et al. [17] demonstrated that micro-concentrator solar cells offer a substantial advantage over regular CPV devices. The smaller size of devices leads to improved heat management, and for micro solar cells with a diameter of  $<200 \text{ }\mu\text{m}$ , the temperature can be kept at less than  $10 \text{ }^\circ\text{C}$  above the temperature of a flat panel solar cell. Paire et al. [18] showed that reducing cell size to the micrometric range allows better thermal evacuation due to a higher surface-to-volume ratio and reduced resistance losses. The microcells showed a 4% absolute improvement in efficiency at a concentration ratio of  $\times 120$ , increasing from 13% to 17%. Under a concentration of  $\times 1000$ , the microcells with a diameter under  $50 \text{ }\mu\text{m}$  had a temperature increase of less than 20 K.

In recent years, CIGS micro-CPVs have attracted increasing attention, and significant progress has been made, demonstrating the feasibility of the CIGS micro-concentrator concept. The required micro-CIGS solar cells can be fabricated using either a top-down or bottom-up approach.

The top-down approach involves isolating the microcells within a large-area solar cell by shadowing, selective deposition, or isolation. Paire et al. [19] fabricated a device with a glass–Mo–CIGS–CdS–ZnO structure featuring a 15-micrometer-diameter active area, with an efficiency of 17% at  $\times 120$ . The microcells were created by depositing a 400-nanometer-thick insulating  $\text{SiO}_2$  layer and a 20 nm/300 nm Ti/Au bilayer on top of the buffer layer. The holes in the  $\text{SiO}_2$  layer were defined by photolithography, after which the ZnO window layer was deposited. In 2013, Paire [20] prepared the CIGS absorber by co-evaporation, creating microcells with a 50-micrometer diameter using photolithography and achieving an efficiency of 21.3% at  $\times 475$ . In a subsequent study [21], CIGS mesa microcells were fabricated through chemical etching. First, an array of patterned photoresist was coated on the cell surface. Then, the front window and CdS layers were etched with a hydrochloric acid solution. Finally, the CIGS layer was chemically etched with a bromine-based solution. The resulting devices exhibited an average absolute efficiency increase of 2% per concentration decade up to approximately 1000 suns. Reinhold et al. [22] developed lamellar-shaped micro solar cells with monolithic interconnects through standard P1, P2, and P3 scribes. This patterning allows a serial connection of single solar cells to form a solar module. The Mo back contact was divided with a P1-scribe, followed by a P2-scribe into the CIGS layer. Finally, a P3-scribe separates the front contact between two cells. The P1-scribe was made using a laser, while the P2 and P3 were mechanically scribed. The lamellar microcells can have an absolute 3.8% efficiency increase under concentrated white light.

In the bottom-up approach, the absorber is locally grown in patterned/defined areas by using masks, patterned substrates, or pre-structured substrates, thereby reducing the usage of critical materials. While various methods can be used to deposit large-area CIGS absorbers, not all allow for local absorber growth. According to the literature, material-efficient deposition methods for CIGS or  $\text{CuInSe}_2$  (CIS) micro-absorbers include electrodeposition, physical vapor

deposition (PVD), and laser-induced forward transfer. Ringleb et al. [23] demonstrated the growth of CIS and CIGS by nucleation of In droplets on laser-patterned substrates during physical vapor deposition and by laser-induced forward transfer (LIFT) of Cu, In, and Ga precursor layers. Efficiencies of 3.06% at 3 suns and 3.36% at 20 suns were achieved for the CIS and CIGS microcells from the nucleation approach, while the CIGS microcells from the LIFT approach reached 0.237% at 20 suns. Heidmann et al. [24] were able to grow CIS micro-absorbers without using patterned substrates by local growth of In islands on Mo-coated glass by PVD, followed by deposition of copper and subsequent selenization, reaching an efficiency of 2.9% under 1 sun and 3.1% at 3 suns. Correia et al. [25] deposited CIS on patterned substrates by electrodeposition, achieving an efficiency of 4.8% under 1 sun. Siopa et al. [26] electrodeposited CIGS absorber layers of 500- and 1500-nanometers-thick into micro-patterned substrates. The microcells demonstrated an increase in efficiencies, reaching 4.8% at 33 suns for the 500-nanometer-thick layer and 5.2% at 3 suns for the 1500-nanometer-thick layer. Table 1 provides a summary of both top-down and bottom-up fabrication approaches for CIGS micro solar cells.

**Table 1.** Summary of top-down and bottom-up fabrication approaches of CIGS micro solar cells.

Fabrication	Deposition Method	Material	Size of Micro Solar Cell ( $\mu\text{m}$ )	Efficiency under 1 Sun (%)	Efficiency under Concentration (%)	Reference
<b>Top-Down</b>						
Photolithography after buffer	Co-evaporation	Cu(In,Ga)Se <sub>2</sub>	15	13	17 ( $\times 120$ )	[19]
Photolithography after i-ZnO	Co-evaporation	Cu(In,Ga)Se <sub>2</sub>	15	~14	~17	[18]
			25	~11.5	~16.5 ( $\times 120$ )	
			50	~13	~16.5	
Photolithography after i-ZnO	Co-evaporation	Cu(In,Ga)Se <sub>2</sub>	50	16.3	21.3 ( $\times 475$ )	[15]
Photolithography and chemical etching	Co-evaporation	Cu(In,Ga)Se <sub>2</sub>	40	~13	~17 ( $\times 100$ )	[21]
			250	~11.5	~15 ( $\times 40$ )	
P1, P2, and P3 scribing	Co-evaporation	Cu(In,Ga)Se <sub>2</sub>	1000 *	13.5	15 ( $\times 6$ )	[22]
			500 *	11.8	14.6 ( $\times 8$ )	
			750 (dot-shaped)	13.6	17.6 ( $\times 51$ )	
<b>Bottom-Up</b>						
Patterned substrate	PVD	CuInSe <sub>2</sub>	40–60	2.9	3.1 ( $\times 3$ )	[24]
Laser-patterned substrate	Nucleation (PVD)	CuInSe <sub>2</sub>	~400	2.9	3.06 ( $\times 3$ )	[23]
		Cu(In,Ga)Se <sub>2</sub>		1.4	3.36 ( $\times 20$ )	
Laser-patterned substrate	LIFT	Cu(In,Ga)Se <sub>2</sub>	~490	0.15	0.237 ( $\times 20$ )	[23]
Patterned substrate	Area-selective electrodeposition	CuInSe <sub>2</sub>	200	4.8	-	[25]
Patterned substrate	Area-selective electrodeposition	Cu(In,Ga)Se <sub>2</sub>	200	4.8	5.2 ( $\times 3$ )	[26]

\* lateral cell width.

Despite the numerous potential benefits, micro-CPVs also present challenges that need to be addressed. Domínguez et al. [14] have described difficulties related to the components' size, emphasizing the crucial need for accuracy and precision in manufacturing, manipulation, alignment, and connection of the microcells and micro-optics. Furthermore, the size of these elements can limit the use of specific tools. Achieving large-scale production at low cost requires the development of enabling manufacturing processes already used in the industries for parallel assembly and interconnection of solar cells, such as self-assembly or inkjet printing, along with large-area optical fabrication methods like hot embossing or casting. Additionally, exploring unconventional optical architectures or reconsidering conventional concepts previously discarded due to high material consumption or high bulk absorption at standard CPV might be viable alternatives. An investigation of CIGS micro-CPVs will enable further understanding of the cell materials' quality, physical and photovoltaic parameters, as well as their operation principles and limitations. This work aims to present a bottom-up approach for the fabrication of pre-structured substrates developed through photolithography and the growth of CIGS micro-absorbers. This study

details the process step-by-step, highlighting key parameters and outlining considerations in substrate fabrication.

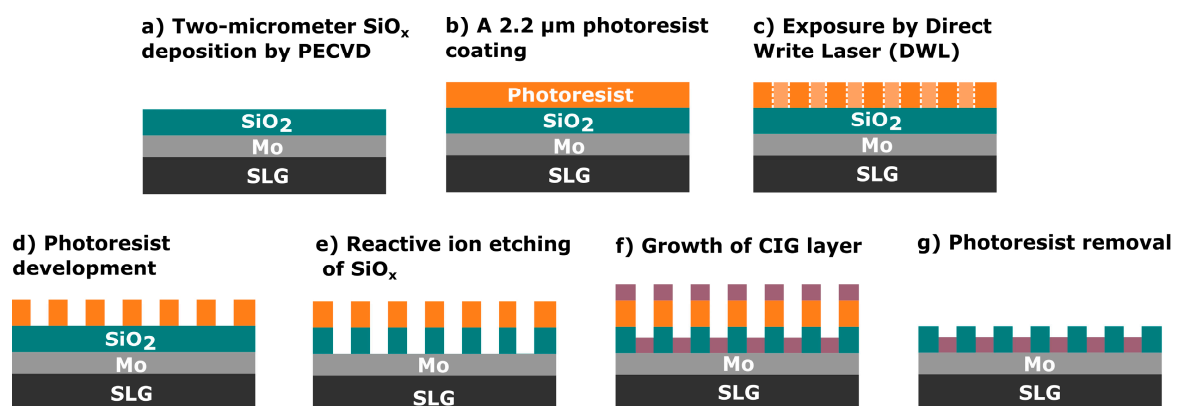
## 2. Materials and Methods

Fabrication started with cleaning 1-millimeter-thick soda–lime glass (SLG) substrates using ultrasonic baths with detergent and deionized water. In the first bath, deionized water at room temperature was used with 3 mL of detergent (MicroSon, Fisherbrand™, Fisher Scientific, Landsmeer, The Netherlands) for 10 min. The second bath was performed at 60 °C with detergent for 10 min. From the third to sixth bath, no detergent was used.

Next, a 500-nanometer-thick Mo back contact bilayer was deposited onto the cleaned SLG substrates by DC magnetron sputtering in the STAR (Sputtering for Advanced Research) sputter-deposition system [27]. To achieve good adhesion of the Mo film to the SLG substrate, a 100-nanometer layer was deposited at 1 Pa pressure, followed by a 400-nanometer layer deposited under a pressure of 0.7 Pa to ensure good conductivity.

### 2.1. Pre-Structured Substrate Fabrication

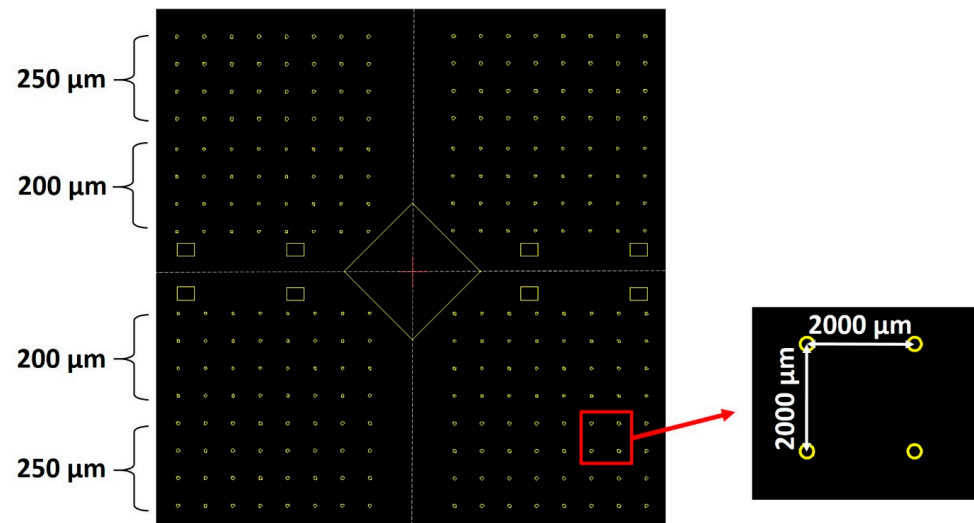
The pre-structured substrates (Figure 1) were fabricated in a cleanroom environment, primarily designed for Si wafers, requiring adaptations for using  $5 \times 5 \text{ cm}^2$  SLG substrates. The process began with another cleaning step in an ultrasonic bath with acetone, followed by several isopropyl alcohol (IPA) and deionized water rinses. Then, the substrate was vapor-primed in an oven (310TA, Yield Engineering Systems, Inc., Fremont, CA, USA) to remove water and organic residues.



**Figure 1.** Schematic of the fabrication process of the pre-structured substrates.

Next, a 2-micrometer-thick  $\text{SiO}_x$  layer was deposited using plasma-enhanced chemical vapor deposition (MPX CVD Module, SPTS Technologies Ltd., Newport, UK) at 300 °C, with a  $\sim 45 \text{ nm/min}$  deposition rate. Afterward, the substrate SLG–Mo– $\text{SiO}_x$  is vapor primed with hexamethyldisilazane (HMDS) in the oven prior to the photoresist coating to enhance adhesion to the substrate. Then, a 2200-nanometer-thick positive photoresist layer (AZ4110, Merck KGaA, Darmstadt, Germany) was spin-coated onto the  $\text{SiO}_x$  layer. The micro-dot pattern was exposed by a direct write laser (DWL 2000, Heidelberg Instruments GmbH, Heidelberg, Germany) lithography system, using a laser power of 120 mW and 405 nm wavelength, followed by the photoresist development (AZ400K 1:4, Merck KGaA, Darmstadt, Germany). Alternatively, a mask aligner (MA6BA6, Suss MicroTec, Garching, Germany) was also used for pattern exposure. The DWL creates high-resolution patterns by laser writing directly onto photoresist-coated samples, whereas the mask aligner requires a physical mask to transfer the pattern. In this case, the mask aligner exposure was performed using a 405 nm wavelength and a low-resolution acetate mask instead of a high-resolution acetate or hard mask. The mask aligner had an exposure time of seconds, whereas, for the DWL, it was at least 10 min. The pattern matrix consisted of circular areas of 200- and

250-micrometer diameters with a 2000-micrometer pitch (Figure 2). Furthermore, a test area of 0.012 mm<sup>2</sup> was incorporated for characterization purposes.



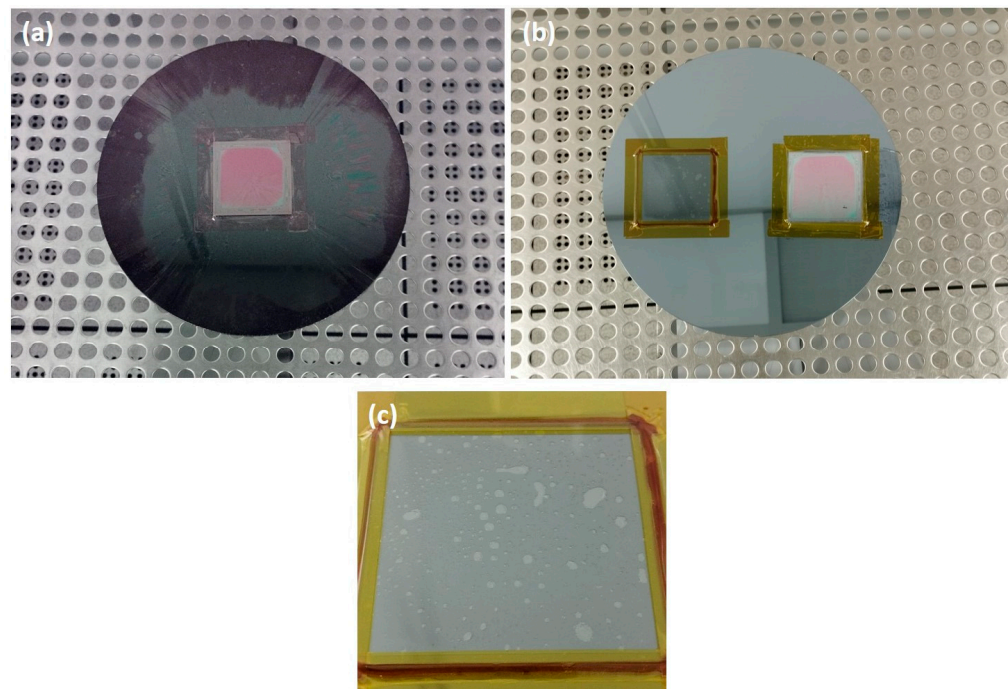
**Figure 2.** CAD design of the micro-dots pattern matrix. The rectangular shapes represent testing areas for thin film and/or device characterizations.

Subsequently, the micro-holes were etched through the SiO<sub>x</sub> layer by reactive ion etching (RIE) (APS Module, SPTS, Technologies Ltd., Newport, UK) until reaching the Mo back contact layer, which was confirmed through optical microscope inspections and profilometer measurements. Once the etching is completed, two routes can be considered to finish the substrate and deposit the Cu–In–Ga (CIG) precursor. In the first, employed in this work, a CIG layer was grown by sputtering followed by photoresist lift-off, leaving the SiO<sub>x</sub> layer with the CIG inside the micro-holes. Subsequently, a plasma asher (M360, PVA TePla America Inc., Corona, CA, USA) was used to remove any residual photoresist. The lifted-off material can be subjected to recovery and recycling processes to produce new targets or to separate the CIG materials [28]. The second route involves area-selective deposition or local growth methods, such as electrodeposition [25,26,29], which are recommended for material saving. In this approach, the photoresist removal is performed after the deposition process.

## 2.2. Structuring the Substrate

To accommodate the use of 5 × 5 cm<sup>2</sup> SLG substrates in the cleanroom, where most tools are prepared to handle 8-inch diameter Si wafers, specific sample-mounting adaptations were necessary for the SiO<sub>x</sub> deposition, photoresist coating and development (Figure 3a), and SiO<sub>x</sub> etching (Figure 3b,c).

For photoresist coating, the SLG–Mo–SiO<sub>x</sub> substrate is fixed on a Si wafer with Kapton tape (Figure 3a). Afterward, for SiO<sub>x</sub> RIE, a crystalbond wax was used between the Si wafer and the SLG pre-structured substrate for good thermal uniformity. Kapton tape was placed around the substrate to fix it against the Si wafer and maintain the wax (which melts during the SiO<sub>x</sub> etching process) between the SLG and the Si support wafer (Figure 3b). Also, the pre-structured substrate was mounted on a Si wafer next to an un-processed SLG substrate for proper weight distribution and effective wafer handling in the RIE tool.



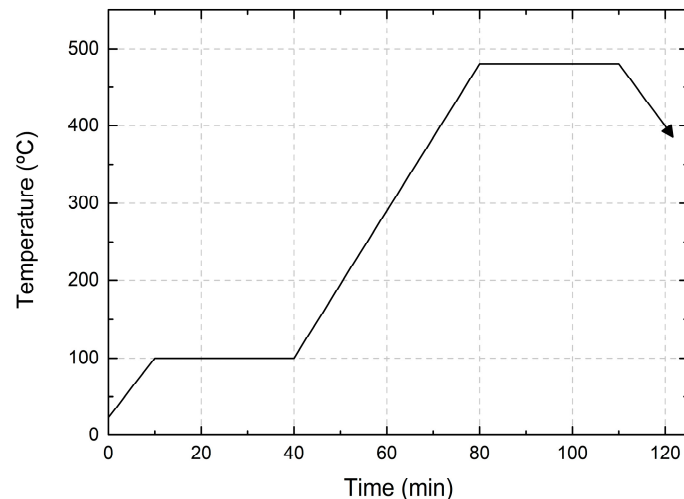
**Figure 3.** SLG–Mo–SiO<sub>x</sub> substrate mounted on standard Si wafer used for (a) photoresist coating and development; (b) SLG–Mo–SiO<sub>x</sub> substrate mounted next to a bare SLG substrate for RIE; (c) close-up of trapped air bubbles in the bare SLG substrate mounted with wax for RIE.

### 2.3. CIG Precursor Deposition followed by 2-Stage Selenization

The CIG precursor was deposited from a ternary CIG target (50:35:15 at%, Testbourne) by the magnetron sputtering system STAR [27] at 1.5 W/cm<sup>2</sup> power density under Ar atmosphere at a working pressure of 0.55 Pa. Subsequently, the resist was removed by lift-off with acetone followed by plasma asher treatment to eliminate any residual photoresist, leaving the SiO<sub>x</sub> layer with the CIG micro-dots. To prevent Mo oxidation, which starts at 300 °C, a low-temperature plasma asher process was employed.

Thermal annealing was introduced prior to selenization to remove any possible photoresist incorporated into the CIG micro-dot during sputtering [30], to improve the precursor quality. Hence, the sample was placed inside a vacuum pot and placed on a heating plate. To prevent contamination, nitrogen was purged and pumped three times into the pot. Then, the hotplate temperature was set to 500 °C and kept for 30 min once the desired temperature was reached. It is important to note that the temperature inside the vacuum pot was lower than the nominal temperature at the hot plate.

The CIG precursor was selenized inside a closed graphite box with 50 mg of Se pellets, and loaded inside a quartz tube to obtain the CIGS absorber. The tube underwent a few cycles of nitrogen and argon purging and pumping to minimize the risk of oxygen contamination. During the 2-stage selenization process, in the first stage, the temperature was kept at 100 °C for 30 min to homogenize the precursors. Subsequently, the temperature was increased to 480 °C for 30 min. Once the process was complete, the furnace was cooled down to below 130 °C. A continuous flow of 100 sccm of Ar was maintained throughout the entire process. Furthermore, both heating and cooling ramps were fixed at a slope of 10 and 20 °C/min, respectively. The heating profile of the selenization process is shown in Figure 4. Furthermore, after selenization, a KCN etching (5%) was performed, followed by CdS buffer layer deposition using a chemical bath.



**Figure 4.** Heating profile for 2-stage selenization.

#### 2.4. Characterization Methods

The electrical properties of the Mo bilayer were evaluated through 4-point probe measurements before and after the fabrication process to ensure the integrity and functionality of the film. To confirm the dimensions and depth of the micro-holes, optical microscope images and profilometer measurements were conducted during the fabrication process.

The morphologies and elemental composition analysis of the as-deposited CIG precursor, annealed ones, and CIGS micro-dots were obtained by scanning electron microscopy (SEM) and energy-dispersive X-ray spectroscopy (EDX) in a FEI Quanta 650 FEG (FEI Company, Hillsboro, OR, USA) SEM coupled with an EDX detector. Raman spectroscopy was performed using a confocal Raman microscope (WITec Alpha 300 R, WITec Wissenschaftliche Instrumente und Technologie GmbH, Ulm, Germany) using a 532 nm laser excitation.

### 3. Results and Discussion

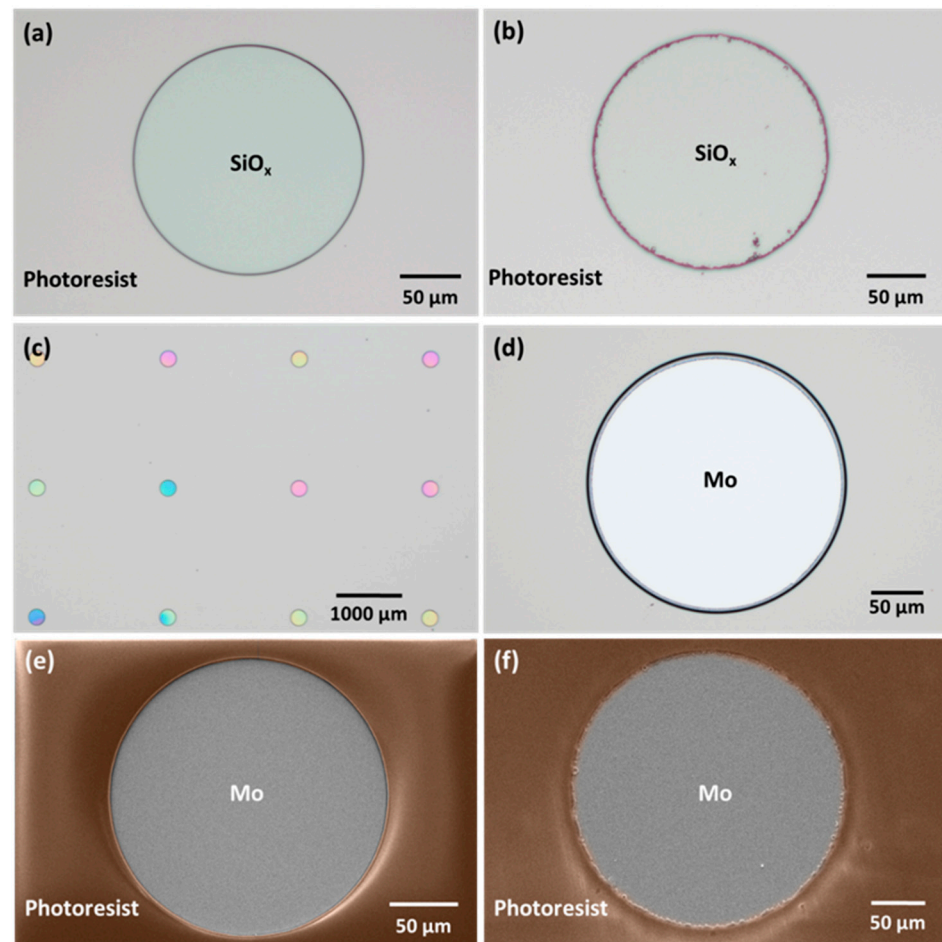
#### 3.1. Pre-Structured Substrate

To ensure a well-conducting back contact for the CIGS solar cell, the sheet resistance of the Mo bilayer was measured both before and after the fabrication. This measurement also confirms that the  $\text{SiO}_x$  layer was properly etched, reaching the Mo layer. A consistent sheet resistance of  $(1.5 \pm 0.3)$  Ohm/sq was measured before and after the fabrication, confirming the integrity of the electrical properties of the Mo film.

The choice of tools for the photoresist exposure of the pattern significantly influences the definition and resolution of the micro-holes in the fabrication process. The photoresist exposure using DWL yielded a higher resolution compared to that achieved with a mask aligner, as illustrated in Figure 5a,b. In the latter case, the final pattern's low resolution can be explained by the intrinsic low resolution of the acetate-printed photomask coupled with the non-optimal contact between the acetate and the glass slide supporting it for mask aligner use. The SEM micrographs show the successful transfer of the mask pattern to the photoresist using DWL (Figure 5e) and the mask aligner (Figure 5f), along with the resulting micro-holes after  $\text{SiO}_x$  etching.

During the RIE process, optical microscopy inspection and profilometer measurements were conducted after each run to verify if the  $\text{SiO}_x$  was completely etched. In Figure 5c, the micro-holes exhibit different colors, indicating slight variations in the  $\text{SiO}_x$  layer thickness after a  $\text{SiO}_x$  etching run. Figure 5d shows a fully etched micro-hole. In some cases, additional  $\text{SiO}_x$  etching runs were necessary to achieve the desired results. While the etching rate of  $\text{SiO}_x$  on standard Si wafers is typically 274 nm/min, on this substrate, the etching rate decreased and became non-uniform, requiring further characterization after each run. This discrepancy could be ascribed to the uneven wax spread during the sample mounting and to trapped air bubbles (Figure 3c), which may lead to thermal non-

uniformity and variations in the etching rate. It is crucial to note that the etching process was performed multiple times, with each run lasting a maximum of 4 min, as etching for a longer time can result in the photoresist burning.



**Figure 5.** Optical images of micro-holes exposed with (a) DWL and (b) mask aligner. Micro-holes after (c)  $\text{SiO}_x$  etching run (different colors indicate variations in the  $\text{SiO}_x$  layer thickness) and (d) completely etched. SEM micrographs of micro-holes exposed with (e) DWL and (f) mask aligner after  $\text{SiO}_x$  etching.

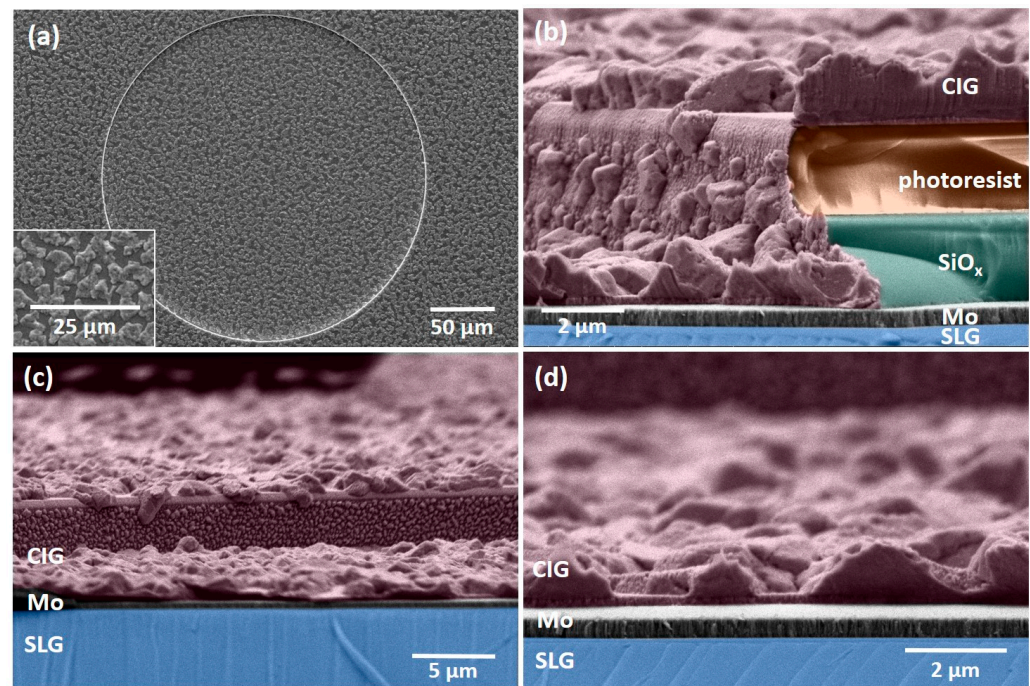
### 3.2. CIGS Growth

Figure 6 shows the surface and cross-sectional micrographs of sputtered CIG precursor micro-dots prior to the photoresist removal. The CIG precursor exhibits a rough surface, with Cu–In-rich grains/islands distributed on the film’s surface. The elemental ratios  $\text{CGI} = [\text{Cu}]/([\text{In}] + [\text{Ga}])$  and  $\text{GGI} = [\text{Ga}]/([\text{Ga}] + [\text{In}])$  were determined through EDX measurements. The target composition corresponds to the CGI and GGI ratios of 1 and 0.3, respectively. However, due to the sputtering target usage and potential cross-contamination from other targets, these ratios can vary in the deposited films. Consequently, the aimed CIG precursor ratios are defined as  $0.7 < \text{CGI} < 1$  and  $0.2 < \text{GGI} < 0.3$ . The precursor film is found to be Cu-poor, with a CGI of  $0.88 \pm 0.04$  and GGI of  $0.26 \pm 0.02$ , both within the desired ranges. SEM micrographs and EDX measurements were performed at the same micro-dots after thermal annealing and selenization to obtain reliable data.

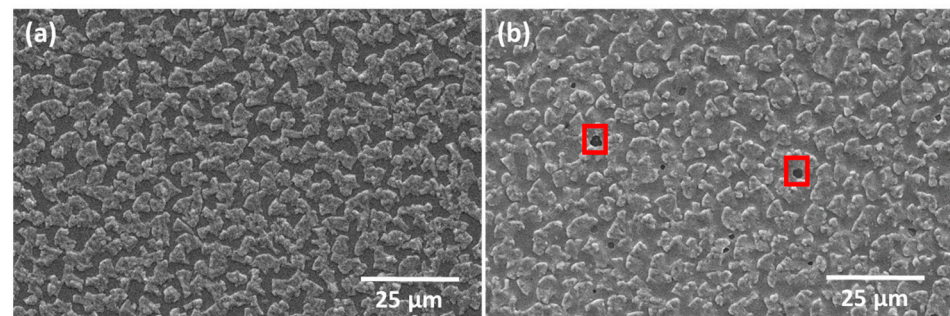
Figure 7 shows SEM micrographs of the as-deposited CIG film (Figure 7a) and annealed at  $500^\circ\text{C}$  (Figure 7b). In the annealed CIG film, the Cu–In-rich grains appear less distinct compared to the as-deposited CIG, and small areas reveal Mo exposure, which could be related to the degassing of photoresist incorporated during CIG sputtering or debris that was not completely removed after RIE. Notably, the  $\text{SiO}_x$  layer remained intact



after the annealing process. The average CGI and GGI ratios for the analyzed micro-dots are  $0.84 \pm 0.05$  and  $0.28 \pm 0.03$ , respectively, falling within the expected ranges.



**Figure 6.** (a) Surface SEM micrograph of CIG precursor micro-dot before photoresist removal acquired at 20 kV; (b–d) cross-sectional SEM micrographs of CIG micro-dot in the  $\text{SiO}_x$ -photoresist matrix acquired at 5 kV. Colors were added in post-processing to improve clarity.

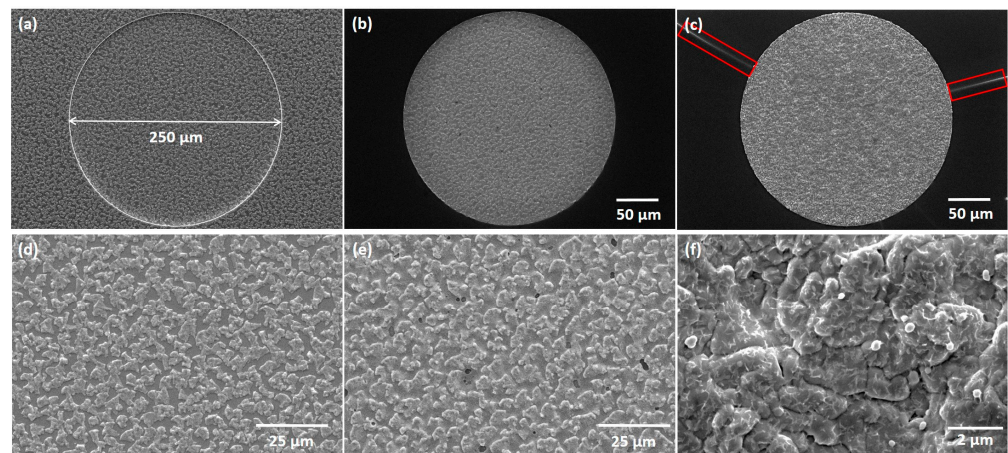


**Figure 7.** SEM micrographs of (a) as-deposited CIG and (b) after thermal annealing at 500 °C. Red squares highlight exposed Mo areas.

The thermally annealed CIG film underwent a two-stage selenization process at 100 and 480 °C. The SEM micrographs showcase the as-deposited CIG precursor (Figure 8a–d), annealed at 500 °C (Figure 8b–e), and the resulting CIGS micro-dots (Figure 8c–f). The surface of the CIGS micro-dot appears rough and homogenous throughout the micro-dot. It is important to highlight that Figure 8f was acquired following the CdS deposition. A summarized elemental composition is presented in Table 2. The CGI ratio was slightly higher than desired, which can be detrimental to the absorber quality. In high-efficiency solar cells, the CIGS absorber requires a low Ga atomic ratio, approximately 0.2–0.3, and a CGI ratio within the range of 0.88–0.92 [31].

In Figure 9, the Raman spectra of a CIGS micro-absorber reveal dominant peaks centered at about 175 and 300  $\text{cm}^{-1}$ . The peak at 175  $\text{cm}^{-1}$  corresponds to the A1 Raman peak of CIGS, associated with the presence of the I-II-VI<sub>2</sub> chalcopyrite compounds [32]. This peak has a full width at half maximum (FWHM) of 6.5  $\text{cm}^{-1}$ , indicating a high crystalline quality of the CIGS layer, which is slightly higher but comparable to the FWHM

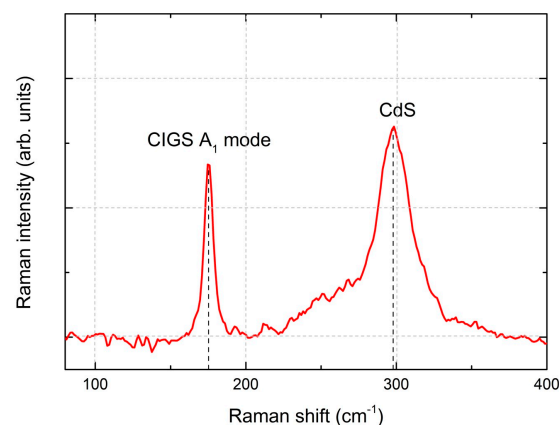
of  $3.7 \text{ cm}^{-1}$  obtained from a reference single crystal Si sample. Furthermore, the shoulder near  $260 \text{ cm}^{-1}$  could be attributed to the presence of Cu-Se compounds such as CuSe or  $\text{Cu}_2\text{Se}$  [32,33]. The peak at  $300 \text{ cm}^{-1}$  has been identified as the main Raman peak from the CdS buffer layer. After the selenization process, the  $\text{SiO}_x$  layer exhibited some cracking (see red rectangles in Figure 8c), whereas the CIGS micro-dots appeared to remain intact. Given the absence of damage after thermal annealing and in comparable samples after selenization, we hypothesize that mechanical stress incurred during the sample's breaking into smaller pieces led to cracks during selenization.



**Figure 8.** Top-view and up-close SEM micrographs of (a–d) as-deposited CIG, (b–e) annealed at  $500 \text{ }^\circ\text{C}$ , and (c–f) selenized. SEM micrograph (f) acquired after CdS deposition. Red rectangles highlight cracking in the  $\text{SiO}_x$  film.

**Table 2.** Elemental compositions of the as-deposited, annealed, and CIGS films.

Sample	Composition (at %)				Ratios	
	Cu	In	Ga	Se	CGI	GGI
CIG	$46 \pm 1.9$	$38 \pm 1.8$	$13 \pm 1.0$	-	$0.88 \pm 0.04$	$0.26 \pm 0.02$
CIG500	$45 \pm 1.7$	$39 \pm 1.7$	$15 \pm 1.8$	-	$0.84 \pm 0.04$	$0.28 \pm 0.03$
CIGS	$24 \pm 0.8$	$20 \pm 1.5$	$5 \pm 1.5$	$50 \pm 0.9$	$1.00 \pm 0.04$	$0.20 \pm 0.06$



**Figure 9.** Raman spectrum of CIGS micro-absorber film after KCN (5%) etching and CdS deposition.

#### 4. Conclusions

In this study, we present a detailed fabrication process and successfully demonstrate the feasibility of employing a bottom-up approach using pre-structured substrates devel-

oped through photolithography for micro-concentrator applications. This approach allows easy modifications to the pattern design for different structures and geometries.

The choice of method for photoresist exposure significantly influences the resolution and definition of the micro-holes, with a direct-write laser resulting in higher resolution compared to a mask aligner. The use of a high-resolution acetate or hard mask should improve the exposure resolution but in both cases no modifications to the pattern designs are possible.

While the fabrication process required some adaptations, the major challenge was encountered during the  $\text{SiO}_x$  etching process, which required intensive inspection after each run and sometimes multiple etching runs to achieve the desired depth to reach the Mo layer.

CIGS micro-absorbers were prepared via sputtering of the CIG precursor into a patterned  $\text{SiO}_x$  matrix, followed by lift-off, thermal annealing at 500 °C, and a two-stage selenization process. The results indicate that both the as-deposited and annealed CIG films were Cu-poor, with CGI ratios of 0.88 and 0.84, respectively. The surface of the as-deposited CIG film exhibited roughness, characterized by CIG grains throughout the film. Subsequent thermal annealing at 500 °C led to less pronounced grains. After the two-stage selenization, the CIGS film had a CGI ratio of 1 and exhibited Raman spectra with a dominant A1 mode peak at  $175 \text{ cm}^{-1}$ , observed in I-III-VI<sub>2</sub> chalcopyrite compounds. In future work, we aim to improve the CIGS absorber material by optimizing the two-stage selenization temperature and to produce complete CIGS microcells by depositing buffer and window layers.

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