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A Novel Fixed Switching Frequency Control Strategy Applied to an Improved Five-Level Active Rectifier

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***Abstract*—A novel fixed switching frequency control strategy applied to an improved five-level active rectifier (iFLAR) is proposed. The operation with fixed switching frequency represents a powerful advantage, since the range of the produced harmonics is well identified, and it is possible to design passive filters to mitigate such harmonics. The experimental validation shows that the control strategy allows attaining an ac-side current with reduced total harmonic distortion and high power factor, which is an attractive influence for grid-connected electrical appliances. This contribution is even more relevant with the new paradigm of smart grids where higher levels of power quality are required. A theoretical analysis of the control strategy and the details of its implementation in a digital signal processor are presented. The control scheme and the developed iFLAR were experimentally confirmed using a laboratorial prototype, showing its benefits in terms of accuracy, reduced total harmonic distortion and high power factor.**

Keywords*—Active Rectifier; Five-Level Converter; Digital Control, Power Quality, Smart Grids.

I. INTRODUCTION

Active rectifiers are emerging in the industrial electronics market as a dominant solution to mitigate power quality problems, giving a low value of total harmonic distortion in the ac-side current, operation with high power factor, and controlled dc-side voltage. The advantages of these features are notorious when compared with the traditional passive rectifiers [1][2], both for single- and three-phase grid interfaces [3][4][5][6].

An exhaustive review about improved unidirectional and bidirectional active rectifiers is presented in [5], where buck- and boost-type topologies are highlighted, including a characterization in terms of multilevel, interleaved, and isolated operation. Since classical active rectifiers are composed by a passive ac-dc converter followed by an active dc-dc converter, a review about the most classical dc-dc converters employed in active rectifiers is presented in [7]. These topologies are denominated as power-factor-correction (PFC). Combining classical passive rectifiers and PFC topologies allows to obtain new characteristics for the active rectifiers, such as the bridgeless, dual-boost, interleaved, or multilevel topologies. Some of these examples are presented in [8], [9], [10], [11], and [12]. Among these characteristics, multilevel topologies have more notoriety, since increasing the voltage levels allows to improve the obtained ac-side grid current with a reduced value for the coupling passive filters [13].

The essential multilevel topologies and control strategies, as well as the main industrial applications of multilevel topologies, are reviewed in [14] and [15]. By establishing a criterion between the number of voltage levels and the required hardware (e.g., sensors, signal conditioning, and gate-drivers), single-phase five-level topologies are an attractive solution for numerous industrial applications as demonstrated by several five-level topologies that were previously proposed for multiple purposes. Some of these examples are: (a) the cascade flying capacitor topology for motor drivers proposed in [16]; (b) the multiple-pole diode-clamped structure for indirect ac-ac converters proposed in [17]; (c) the Vienna-type and the bridgeless topology for electric vehicles battery chargers presented, respectively, in [18] and [19]; (d) the T-type topology for applications of power generating units proposed in [20]; (e) the H-bridge structure for shunt active power filters proposed in [21]; (f) the generic two dc-link topology presented in [22]; (g) and the double dc-link topology, the cascade dc-link topology, the interleaved-based topology, the multiple-pole Vienna topology proposed in [23], [24], [25], and [26], respectively. Among them, five-level topologies with a single dc-side output (even with a split dc-link) are the most convenient for active rectifiers, since this is useful to interface a dc-dc converter, or a set of dc-dc converters, for instance, in the case of a dc grid [27].

Concerning five-level topologies, an improved five-level active rectifier (iFLAR) with a split dc-link and with a fixed switching frequency current control strategy is proposed in this paper, where the circuit topology is presented in Fig. 1. A similar topology, also switched at fixed frequency, is investigated in [28], however, the bidirectional cell is composed by a diode full-bridge and by a switching device, representing a disadvantage facing the proposed in this paper. In this case, in order to produce the voltage level $v_{dc}/2$, the current flows by two diodes and by the switching device,

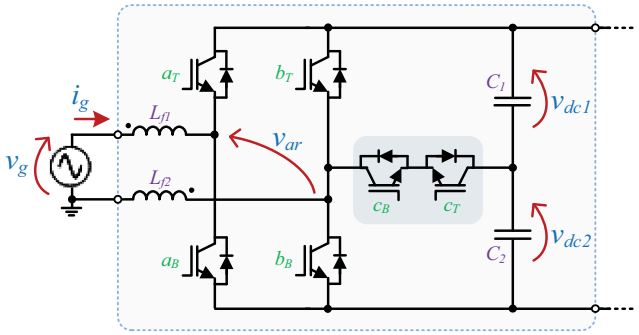

Fig. 1. Topology of the improved five-level active rectifier (iFLAR).

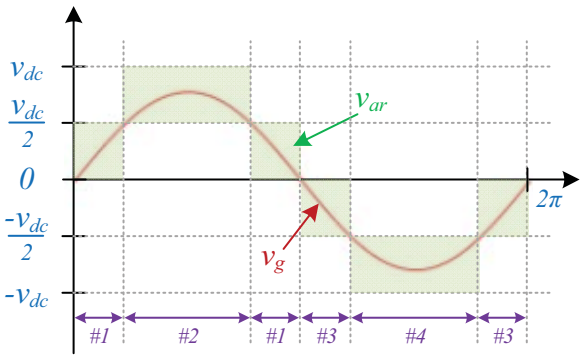

Fig. 2. Defined voltage regions (#1 to #4) according to the different voltage levels and the grid voltage (v_g).

representing the main disadvantage of this topology, since the proposed one (cf. Fig. 1) only uses a switching device and a diode for the same purpose of producing the level $+v_{dc}/2$. The proposed topology is considered as new, since an alternative is proposed for the bipolar bidirectional cell of this five-level structure. Aiming to mitigate this effect, an improved topology is proposed in [29] for unidirectional operation and a similar improved topology is proposed in [30] for bidirectional operation. However, in both traditional cases of the literature, the switching frequency is variable and the bidirectional cell is composed by two diodes and two switching devices, where, in order to produce the voltage level $v_{dc}/2$, the current flows through a diode and a switching device. In this case, the number of required diodes and switching devices is the double comparing with the proposed topology (cf. Fig. 1), representing a relevant disadvantage. Summarizing, a topology with reduced number of semiconductors and switched at fixed frequency are the main advantages of the proposed iFLAR fronting the aforementioned topologies available in the state-of-the-art.

The paper is organized as follows: Section II presents a theoretical analysis of the proposed iFLAR; Section III introduces the digital implementation of the control strategy for the iFLAR; Section IV shows the obtained results during the experimental verification; Section V ends the paper with the conclusions.

II. Theoretical Analysis

As shown in Fig. 1, the iFLAR is established by an active full-bridge ac-dc converter and by a bipolar and bidirectional cell connected between the split dc-link and the neutral leg of the ac-dc converter. As aforementioned (cf. section I), the main advantage of this topology lies in the bipolar and bidirectional cell, since only two switching devices are used (in this case, IGBTs). When operating as active rectifier, four regions are possible to define the iFLAR state in order to establish the five voltage levels. Fig. 2 shows the regions (defined as #1 to #4) according to the different voltage levels and the grid voltage (v_g). The different regions and the state of each IGBT are summarized in table I. As shown, the IGBTs a_T and a_B are switched at the grid voltage frequency, the IGBTs b_T and b_B are only used to produce the voltage level 0, and the IGBTs c_T and c_B are only used to produce the voltage level $+v_{dc}/2$, representing an attractive tactic to reduce the switching losses. Summarizing, in each region, to change the level of the produced voltage, it is necessary to change the status of only one IGBT.

Considering a pulse-width modulation (PWM) with a single unipolar triangular carrier, it is necessary to adopt a strategy for the reference of voltage (cf. v_{ar}* in Fig. 1) in order to define the status of the six IGBTs. Fig. 3 shows the

TABLE I
DIFFERENT REGIONS AND STATE OF EACH IGBT FOR PRODUCING THE FIVE VOLTAGE LEVELS

	Region	a_T	a_B	b_T	b_B	c_T	c_B	v_{ar}
$v_g > 0$	#1	ON	OFF	ON	OFF	OFF	OFF	0
		ON	OFF	OFF	OFF	ON	OFF	$v_{dc}/2$
	#2	ON	OFF	OFF	OFF	ON	OFF	$v_{dc}/2$
		ON	OFF	OFF	OFF	OFF	OFF	v_{dc}
$v_g < 0$	#3	OFF	ON	OFF	ON	OFF	OFF	0
		OFF	ON	OFF	OFF	OFF	ON	$v_{dc}/2$
	#4	OFF	ON	OFF	OFF	OFF	ON	$v_{dc}/2$
		OFF	ON	OFF	OFF	OFF	OFF	v_{dc}

adopted strategy, where the original reference voltage (v_{ar}*), determined by the current control strategy is modified and decomposed in two signals to be compared with the PWM carrier. The sum of the signals v_{ar2}* and v_{ar3}* results in the original signal v_{ar}*. The signal v_{ar1}* is used to control the IGBTs a_T and a_B at the grid voltage frequency. The results shown in Fig. 3 were obtained from a computer simulation performed with the PSIM software in order to illustrate the principle of operation of the iFLAR. In this specific case, a switching frequency of 2 kHz was selected in order to be possible to visualize the PWM carrier and the reference voltage signals (v_{ar1}*, v_{ar2}* and v_{ar3}*), as well as the gate-pulse pattern of the IGBTs.

By examining in detail Fig. 3, it is noticeable that the voltage signal v_{ar1}* is used to define the status of the IGBTs a_T and a_B. Throughout the positive half-cycle, the voltage signal v_{ar2}* is compared with the PWM carrier to define the status of the IGBTs b_T and c_B (region #1 with the voltage levels 0 and $+v_{dc}/2$), and the voltage signal v_{ar3}* is compared with the PWM carrier to define the status of the IGBTs b_B and c_T (region #2 with the voltage levels $+v_{dc}/2$ and $+v_{dc}$). It should be noted that the pairs formed by the IGBTs b_T and c_B, as well as b_B and c_T, are switched in a complementary way, i.e., when the IGBT b_T is ON, the IGBT c_B is OFF, and vice-versa. In opposition, throughout the negative half-cycle, the voltage signal v_{ar2}* is compared with the PWM carrier to define the status of the IGBTs b_T and c_B (region #4 with the voltage levels $+v_{dc}/2$ and $+v_{dc}$), and the voltage signal v_{ar3}* is compared with the PWM carrier to define the status of the IGBTs b_B and c_T (region #3 with the voltage levels 0 and $+v_{dc}/2$). Also in this circumstance, it should be noted that the pairs formed by the IGBTs b_T and c_B, as well as b_B and c_T, are switched in a complementary way, i.e., when the IGBT b_T is ON, the IGBT c_B is OFF, and vice-versa.

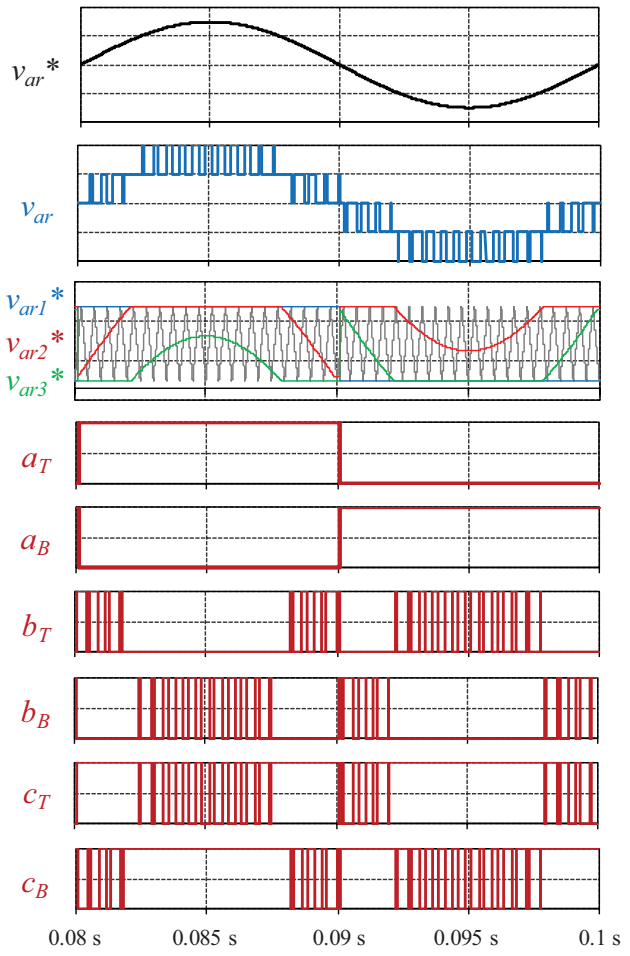

Fig. 3. Adopted strategy for obtaining the IGBTs gate-pulse patterns of the iFLAR using a single unipolar carrier in the PWM.

III. Digital Implementation of the Proposed Control Strategy

The digital implementation of the control strategy for the iFLAR follows the structure offered in Fig. 4. In order to control the dc-link voltages (v_{dc1} and v_{dc2}), two digital proportional-integral (PI) controllers are employed. Taking into account the two dc-link voltages (cf. Fig. 2), v_{dc1} is controlled in the positive half-cycle and v_{dc2} in the negative half-cycle of the grid voltage, allowing to establish balanced voltages in the split dc-link (v_{dc1} and v_{dc2}).

As the iFLAR operates with sinusoidal ac-side current and unitary power factor, only active power can be considered during its operation. Therefore, neglecting the losses, the dc power is equal to the average value of the active power (ac-side). From this assumption, a relation between the ac-side power and the dc-side power can be established as:

$$\frac{1}{m}\sum_{n=1}^{m} v_g[n]\, i_g[n] = p_{dc}[n]\,, \tag{1}$$

where m is selected with the value 800 for a digital sampling frequency of 40 kHz and a grid voltage frequency of 50 Hz, and p_{dc} is the sum of a parcel of power necessary for the dc-link regulation and a parcel of the power consumed by the dc-side load (a dc-dc converter can also be considered, maintaining the same reasoning). For the grid point of view, the iFLAR operates as a linear resistive load, therefore, it can be established:

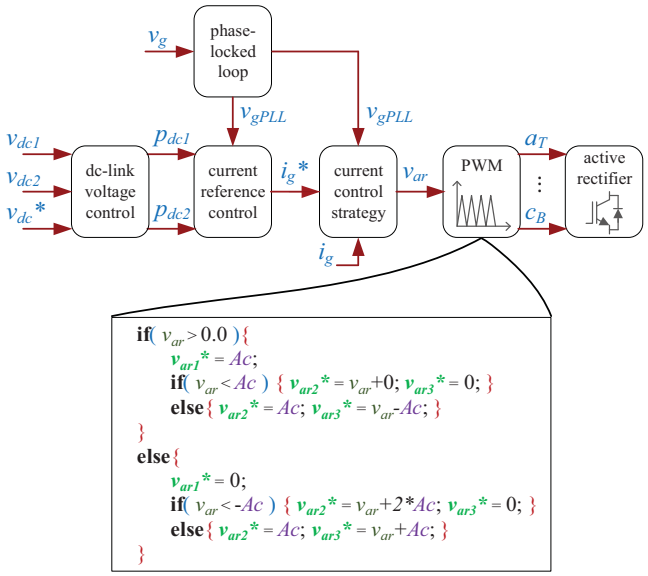

Fig. 4. Digital implementation structure of the iFLAR control strategy and digital codification to obtain the voltage signals v_{ar1}*, v_{ar2}* and v_{ar3}* from the original reference voltage v_{ar}*.

$$\frac{1}{m}\sum_{n=1}^{m} v_g[n]\, i_g[n] = {V_G}^2[n]\,\frac{i_g[n]}{v_g[n]}. \tag{2}$$

By combining (1) and (2), and rearranging in order to the ac-side current (i_g), results in:

$$i_g[n] = p_{dc}[n]\,\frac{v_g[n]}{{V_G}^2[n]}\,, \tag{3}$$

where the value of i_g is the operating current of the iFLAR for a specific value of dc-side power. As aforementioned, the active rectifier operates only with active power, therefore, the ac-side current (i_g) must be sinusoidal, even with a non-sinusoidal grid voltage (v_g). For such objective, a phase-locked loop (PLL) is employed instead of the grid voltage [31]. Thus, in (3), the grid voltage (v_g) is substituted by the resulting sinusoidal signal of 50 Hz from the PLL, which corresponds to its fundamental component:

$$v_{gPLL}[n] = V_G\,\sqrt{2}\,\sin[\emptyset]\,, \tag{4}$$

where Φ is determined by the PLL. The obtained value of i_g from (3) is the reference current (i_g*) for the current control strategy, i.e., the required instantaneous ac-side current for the dc-side operating power. As a consequence, the resultant ac-side current is established by:

$${i_g}^*[n] = p_{dc}[n]\,\frac{\sqrt{2}}{V_G[n]}\sin[\emptyset]\,. \tag{5}$$

By applying the Kirchhoff laws in the ac-side of the iFLAR, as well as the forward Euler discretization method for the derivative of the ac-side current, results in:

$$v_{ar}[n] = \frac{L}{T_s}\,i_g[n] + v_g[n] - \frac{L}{T_s}\,{i_g}^*[n]\,, \tag{6}$$

where v_{ar} is the voltage that the active rectifier must synthesize in order to achieve an ac-side current (i_g) following its reference (i_g*). Therefore, the resultant reference current (i_g*) from (5) is directly applied in (6). After that, v_{ar} is modified in order to obtain three voltage signals (v_{ar1}*, v_{ar2}*, and v_{ar3}*) that are applied to a PWM

with a single unipolar carrier in order to obtain the IGBTs gate-pulse patterns (cf. section II). A detail of the digital implementation in C code to obtain the voltage signals v_{ar1}*, v_{ar2}*, and v_{ar3}* from the original reference voltage v_{ar}* is presented in Fig. 4, where Ac means the amplitude of the PWM carrier. The strategy to modify the original reference voltage (v_{ar}) into the three voltage signals (v_{ar1}*, v_{ar2}*, and v_{ar3}*) was adopted due to the resources of the digital platform used in the experimental validation.

IV. Experimental Verification

Aiming to experimentally evaluate the iFLAR, a prototype was developed and tested in laboratory. Fig. 5(a) shows the workbench, where the iFLAR and the digital control platform are highlighted. Fig. 5(b) and Fig. 5(c) shows some details of the developed prototype, respectively, a view of the split dc-link and a view of the driver boards of the IGBTs. The digital control platform is mainly constituted by a 150 MHz digital signal processor (DSP) (Texas Instruments model F28335) and by an external bipolar 14 bit A/D converter (Maxim model MAX1320), which is used for the ac-side and dc-side signals acquisition, since the DSP internal A/D converters are unipolar. A classical parallel interface was established between the external A/D converter and the DSP. A sampling frequency of 40 kHz was assumed in the digital implementation using a timer interruption, allowing a switching frequency of 20 kHz in the PWM implementation. The power hardware of the iFLAR was developed employing discrete IGBTs (Fairchild Semiconductor model FGA25N120ANTD) and isolated discrete gate-drivers formed by optocouplers HCPL3120. The split dc-link is formed by two sets of capacitors, each one with a capacitance of 2.8 mF, and the coupling filter consists in an inductor of 3 mH. A resistive load was connected at the dc-side to emulate a real operation for the iFLAR.

The experimental results of the control strategy to obtain the IGBTs gate-pulse patterns using a single unipolar carrier of 20 kHz are presented in Fig. 6. These results were obtained using the DSP and an external bipolar D/A converter (Texas Instruments model TLV5610). The first voltage signal (v_{ar1}*) is directly compared with the PWM carrier, since the IGBTs are switched at the grid voltage frequency. This signal is used to control the IGBTs a_T and b_B. On the other side, the voltage signal v_{ar2}* is compared with the PWM carrier to control the IGBTs b_T and c_B, and the voltage signal v_{ar3}* is compared with the PWM carrier to control the IGBTs b_B and c_T. It is important to note that the sum of v_{ar2}* with v_{ar3}* results in the reference voltage (v_{ar}*) calculated by the current control algorithm (cf. section III).

Using the aforementioned strategy of the modified reference voltage (v_{ar}*), the gate-pulse patterns for the six IGBTs are presented in Fig. 7 and in Fig. 8. Fig. 7 shows the experimental results, during 20 ms, of the gate-pulse patterns for the IGBTs a_T, b_T, b_B, and Fig. 8 shows the experimental results, during 20 ms, of the gate-pulse pattern of the IGBTs a_B, c_T and c_B. These results were obtained by directly measuring the gate-emitter voltage of each IGBT in the iFLAR prototype. In this figure, it is possible to observe that the IGBTs are turned-on with a positive voltage (+15 V), and turned-off with a negative voltage (-15 V), which is obtained with the IGBTs gate-drivers circuit.

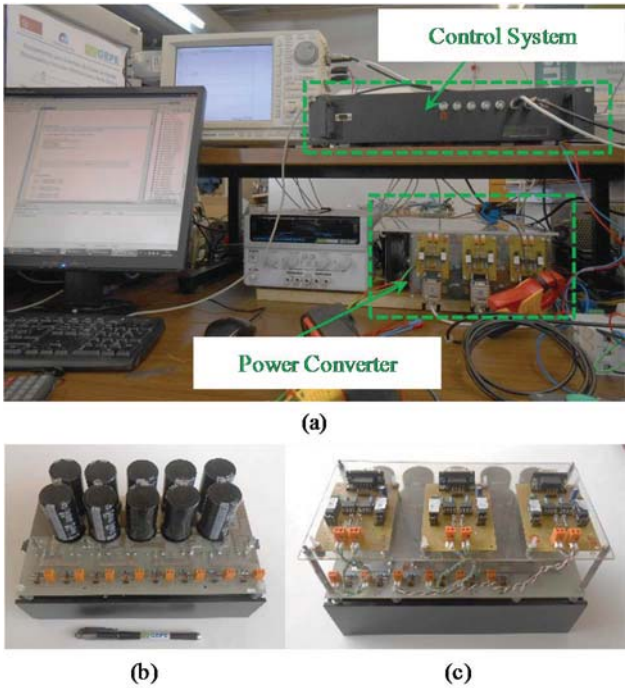

Fig. 5. Developed prototype: (a) Connection in the laboratory workbench; (b) Detail of the split dc-link capacitors; (c) Detail of the driver boards of the IGBTs.

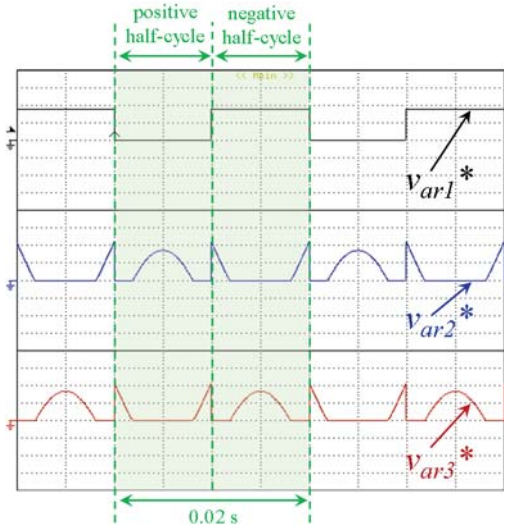

Fig. 6. Experimental results of the control strategy to obtain the IGBTs gate-pulse patterns using a single unipolar carrier.

The experimental results obtained for the voltage v_{ar} (i.e., the voltage established by the iFLAR and measured downstream the grid coupling filter, cf. Fig. 1), for the ac-side current (i_g), and for the grid voltage (v_g) are shown in Fig. 9 in a steady-state operation. By observing this figure, it is possible to identify the five voltage levels ($+v_{dc}$, $+v_{dc}/2$, 0, $-v_{dc}/2$ and $-v_{dc}$) in both positive and negative half-cycles. The measured ac-side current is sinusoidal and in phase with the voltage, i.e., presenting a unitary power factor operation. A total harmonic distortion (THD) of 1.7% and a unitary power factor were measured for a grid voltage of 230 V (with a THD of 3.5%) and an operating active power of 1 kW, both measured with the 435 power quality analyzer from FLUKE. In order to establish a comparison, the THD of a five-level topology was measured and a value of 4% was measured [19], meaning that the proposed topology has an improvement in terms of THD. Since the iFLAR was connected directly to the grid, the voltage v_g has harmonic

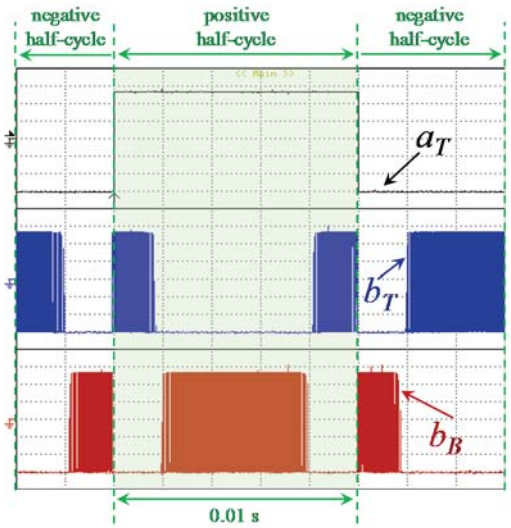

Fig. 7. Experimental results of the gate-pulse patterns for the IGBTs a_T, b_T, and b_B, resultant from the comparison of the modified v_{ar}* with the PWM carrier.

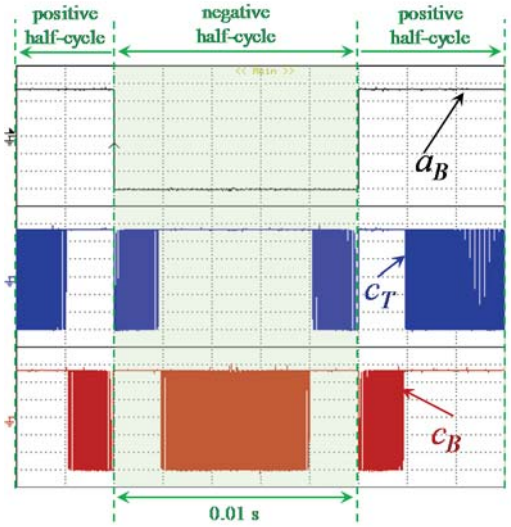

Fig. 8. Experimental results of the gate-pulse patterns for the IGBTs a_B, c_T, and c_B resultant from the comparison of the modified v_{ar}* with the PWM carrier.

distortion, which is affected by the nonlinear appliances also connected in the installation. However, since a PLL is used in the control strategy for the reference current, a sinusoidal ac-side current is achieved. A detailed description of the adopted strategy is presented in section III. Details concerning the switching frequency and the ac-side current ripple are presented in Fig. 10(a) and Fig. 10(b), respectively. As expected, a fixed switching frequency of 20 kHz is obtained for the synthesized current. The measured ac-side current ripple was 0.5 A. The experimental results showing in detail the grid voltage (v_g), the voltage regions where are defined the voltages produced (obtained from the DSP with the D/A converter), the voltage produced by the iFLAR (v_{ar}) and the ac-side current (i_g) are presented in Fig. 11. The obtained results are in accordance with the control description presented in section III. In this figure it is possible to identify the transition from the positive to the negative half-cycle, illustrating that the ac-side current (i_g) crosses the zero at the same time of the grid voltage (v_g), resulting in a unitary power factor.

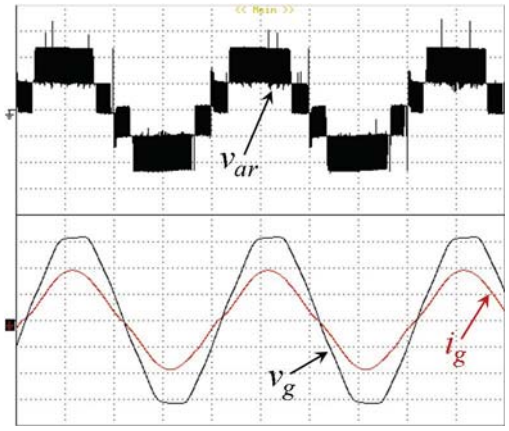

Fig. 9. Experimental results obtained in steady state operation: Voltage produced by the iFLAR (v_{ar} – 200 V/div); Ac-side current (i_g – 5 div/A); Grid voltage (v_g – 100 V/div).

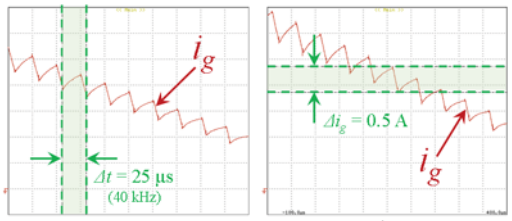

Fig. 10. Experimental results showing in detail: (a) The switching frequency; (b) The ac-side current ripple.

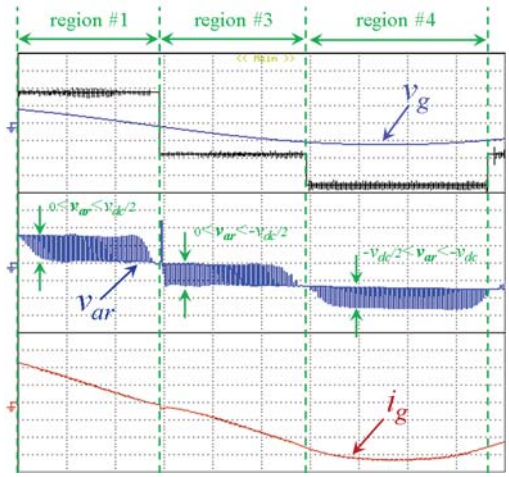

Fig. 11. Experimental results showing in detail the grid voltage (v_g), the voltage regions where are defined the voltage produced (obtained from the DSP with the D/A converter), the voltage produced by the iFLAR (v_{ar}) and the ac-side current.

V. Conclusions

An improved five-level active rectifier (iFLAR), controlled by a strategy based on a fixed switching frequency, is presented. Throughout the paper, a theoretical analysis is presented, showing in detail the principle of operation and the key advantages of the proposed iFLAR in contrast with the most relevant five-level active rectifiers. Details about the digital employment of the control algorithm are presented. The experimental validation is verified using a developed five-level active rectifier, whose details of implementation are presented along the paper. The experimental results show the proper operation of the iFLAR in terms of high levels of power quality, i.e., an operation with unitary power factor and sinusoidal ac-side current, which are attractive contributions for grid connected electrical appliances in smart grids.

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