**Universidade do Minho**
Escola de Engenharia

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# Power Management Circuit: Design and Comparison of Efficient Techniques for Ultra-Low-Power Analog Switch and Rectifier Circuits

Novembro de 2021

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# Power Management Circuit: Design and Comparison of Efficient Techniques for Ultra-Low-Power Analog Switch and Rectifier Circuits

Dissertação de Mestrado

Mestrado Integrado em Engenharia Eletrónica Industrial e Computadores

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Trabalho efetuado sob a orientação do

Professor Luís Gonçalves

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## Statement of Integrity

I hereby declare having conducted this academic work with integrity. I confirm that I have not used plagiarism or any form of undue use of information or falsification of results along the process leading to its elaboration.

I further declare that I have fully acknowledged the Code of Ethical Conduct of the University of Minho.

## Resumo

A presente dissertação de mestrado apresenta um estudo na área de *CMOS* em circuitos analógicos/digitais para extração e conversão de potência adequado para aplicações em *energy harvesting*.

As principais contribuições científicas deste trabalho são: o desenvolvimento de circuitos de baixo consumo energético, tais como um interruptor analógico e um retificador que podem extrair e converter eficientemente a potência de saída do *energy harvester*. Com os dois circuitos apresentados na presente dissertação, é possível alimentar um nó de uma rede de sensores sem fios. Estes circuitos foram projetados utilizando a tecnologia *CMOS* de 130 nm e as respetivas simulações foram realizadas utilizando o software *Cadence Virtuoso Analog Environment*.

Neste trabalho projetou-se novo interruptor analógico para aplicações em *energy harvesting* com especial atenção para a obtenção de um baixo consumo energético. A configuração apresentada consegue atingir uma baixa resistência, quando em condução (ON), e evitar correntes reversas indesejadas provenientes da carga. Os resultados das simulações revelam que o circuito: consome uma potência de 200.8 nW; atinge uma baixa resistência, quando em condução, de 216 Ω; gera uma baixa corrente de fuga de 44 pA. Assim sendo, é possível verificar que este circuito consegue operar com um baixo consumo, baixa tensão e com uma baixa frequência. Para além disso, o mesmo interruptor analógico consegue realizar a técnica de *up-conversion* dentro do circuito de controlo de potência, o que indica a possibilidade de o mesmo contribuir para uma aplicação real com *energy harvesters* vibracionais.

O retificador em CMOS proposto é constituído por dois estágios: um passivo com um conversor de tensão negativa; e um outro estágio com um díodo ativo controlado por um circuito de cancelamento de *threshold*. O primeiro estágio é responsável por retificar completamente o sinal de entrada com uma queda de tensão de 1 mV, enquanto que o último tem a função de reduzir a corrente reversa indesejada, o que consequentemente consegue aumentar a potência transferida para a carga. Deste modo, o circuito consegue atingir uma eficiência em tensão e potência de 99 % e 90%, respetivamente, para um sinal de entrada com 0.45 V de amplitude e para cargas resistivas de valor baixo. Ainda assim, este circuito consegue funcionar a uma banda de frequências desde os 800 Hz até 51.2 kHz, o que se revela ser promissor para a aplicação prática deste projeto.

**Palavras-Chave:** *Energy Harvesting*, circuito de controlo de potência, *Analog Switch*, *CMOS Rectifier,* circuitos de baixo consumo energético.

## Abstract

The master dissertation presents a study in the area of mixed analog/digital CMOS power extraction and conversion circuits for Power Management Circuit (PMC) suitable for energy harvesting applications.

The main contributions of the work are the development of low power circuits, such as an Analog Switch and a Rectifier, that can efficiently extract and convert the output power of the vibrational energy harvester into suitable electric energy for powering a Wireless Sensor Network (WSN) node. The circuit components were fully designed in the standard 130 nm CMOS process, and the respective simulation experiments were carried out using the Cadence Virtuoso Analog Environment.

A new Analog Switch was designed for energy harvesting applications with special consideration for achieving low power consumption. The proposed structure can achieve a reduced ON-resistance and avoid the reverse leakage current from the load. Simulation results reveal a power consumption of about 200.8 nW, a low ON-resistance of 244.6 Ω, and a low leakage current of around 44 pA, which indicates that the analog switch has features of low power consumption, low voltage, and low-frequency operation. Furthermore, this switching circuit is suitable for performing the up-conversion technique in the PMC, which may contribute to the real application of vibrational energy harvesters.

The proposed CMOS Rectifier consists of two stages, one passive stage with a negative voltage converter, and another stage with an active diode controlled by a threshold cancellation circuit. The former stage conducts the signal full-wave rectification with a voltage drop of 1 mV while the latter reduces the reverse leakage current, consequently enhancing the output power delivered to the ohmic load. As a result, the rectifier can achieve a voltage and a power conversion efficiency of over 99 % and 90 %, respectively, for an input voltage of 0.45 V and low ohmic loads. This circuit works for an operating frequency range from 800 Hz to 51.2 kHz, which is promising for practical applications.

**Keywords:** Energy Harvesting, Power Management Circuit, Analog Switch, CMOS Rectifier, low-power consumption circuits.

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## Acronyms

**A**

**AC** Alternating Current.

**AVC** Adaptive Voltage Controller.

**C**

**CMOS** Complementary Metal-Oxide-Semiconductor.

**D**

**DC** Direct Current.

**DIBL** Drain-Induced Barrier Lowering

**DSB** Dynamic Switching Bulk.

**I**

**IC** Integrated Circuit.

**M**

**MEMS** Microelectromechanical Systems.

**MOSFET** Metal-Oxide-Semiconductor Field-Effect Transistor.

**N**

**NMOS** N-type Metal-Oxide-Semiconductor

**NVC** Negative Voltage Converter.

**P**

**PCE** Power Conversion Efficiency.

**PMC** Power Management Circuit

**PMOS** P-type Metal-Oxide-Semiconductor

**R**

**RF** Radio Frequency.

**T**

**TG** Transmission Gate.

**THD** Total Harmonic Distortion.

**V**

**VCE** Voltage Conversion Efficiency.

**VLSI** Very Large-Scale Integration.

**W**

**WSN** Wireless Sensor Network.

# 1 Introduction

During the past years, WSNs have been crucial in supporting continuous environmental monitoring, where sensor nodes are spatially distributed and must remain operational to collect and transfer data from the environment to a base station. As a result, these WSNs have been gaining popularity in many applications, such as environmental monitoring, animal tracking, earth disasters, and health monitoring of civil structures such as bridges and buildings (Fong 2016; Sharma et al. 2010).

WSNs often consist of many sensor nodes distributed in the environment and a gateway node that collects all the data for storage or transmit to a remote server (Fong 2016; Silva, Khan, and Han 2018). In these systems, the sensor nodes are battery-operated devices with the ability to sense the specific environmental parameter required by the application. Then, the device transfers the collected data to the local gateway in order to further process and store it (Adu-Manu et al. 2018). However, throughout this communication process, these nodes consume a high energy level, which reduces its lifetime if using a small battery as the primary supply unit (Chew, Ruan, and Zhu 2019). Furthermore, batteries have been revealed to be a bottleneck to electronic demands and environmental nightmares since some nodes are in hard-to-reach places, leading to high maintenance costs regarding battery replacement. Thus, using a more reliable energy source is vital to efficiently extend the WSN operation time (Ruan, Chew, and Zhu 2017).

Energy harvesting urges as a promise and reliable technology to power these low-power sensor networks (Chew, Ruan, and Zhu 2019). It can power up a self-sustainable WSN by scavenging the necessary power supply from environmentally friendly sources, making it an innovative technology that allows for clean and renewable energy production. It can also be compatible with the current trends and the ongoing depletion of natural resources. Several sources can be used to harvest energy, such as radiant, mechanical, and thermal. Table 1 illustrates the energy-harvesting sources and their corresponding power densities. It can be noticed that the highest power density comes from outside solar cells. However, sensor nodes might be deployed under shaded areas that do not receive much sunlight even during the day and receive no sunlight during the night. This issue affects the operational cycle of the sensor nodes. Furthermore, due to the existence of mechanical vibrations almost everywhere at any time, this type of energy source is an attractive candidate to power these systems (Toshiyoshi et al. 2019).

*Table 1: Energy Harvesting approaches adopted from Adu-Manu (2018).*

| Energy Sources | Types | Energy-Harvesting Method | Power density |
|---|---|---|---|
| Radiant | Solar | Solar cells (indoors) | <10μW/cm$^2$ |
| | | Solar cells (outdoors, sunny days) | 15mW/cm$^2$ |
| | RF | Electromagnetic conversion | 0.1μW/cm$^2$ (GSM) |
| | | Electromagnetic conversion | 0.01μW/cm$^2$ (Wi-Fi) |
| Mechanical | Wind Flow and Hydro | Electromechanical conversion | 16.2μW/cm$^3$ |
| | Acoustic Noise | Piezoelectric | 960nW/cm$^3$ |
| | Motion | Piezoelectric | 330μW/cm$^3$ |
| Thermal | Body heat | Thermoelectric | 40μW/cm$^2$ |

Since it is intended to integrate all these systems (energy harvester + electronic system) in a single chip, the solution is to incorporate MEMS and CMOS (Shu *et al.,* 2006). Therefore, due to their MEMSs compatibility, mechanical vibration energy is commonly explored since it is available in small-scale systems (Guyomar *et al.*,2011). Moreover, due to the high energy density and integration potential, piezoelectric energy harvesters are the most viable approach for designing self-powered small-scale devices (Shu and Lien 2006; N. Chen et al. 2017; Adu-Manu et al. 2018). Nevertheless, in real-world applications, ambient vibrations are unpredictable, time-varying, and low amplitude, which can be concluded that the scavenged energy cannot be directly applied to WSN (Dong et al. 2019; Guyomar et

al. 2007). Thus, some concerns must be taken to the energy harvester's output signal's properties when powering electronic systems or charging batteries, such as low-power signals, random fluctuations, and AC output signals.

Considering the characteristics mentioned above that restrict the available power of the energy harvesting system, a PMC, as shown in Figure 1, was proposed to overcome these limitations (P. Li et al. 2014; 2019). This PMC needs to extract efficiently, convert, store, regulate and manage the scavenged energy from the harvester to maximize the amount of energy transferred under various ambient conditions (Chew, Ruan, and Zhu 2019). The overall aim of this circuit is to extend the lifetime of the sensor networks while having a low power consumption.

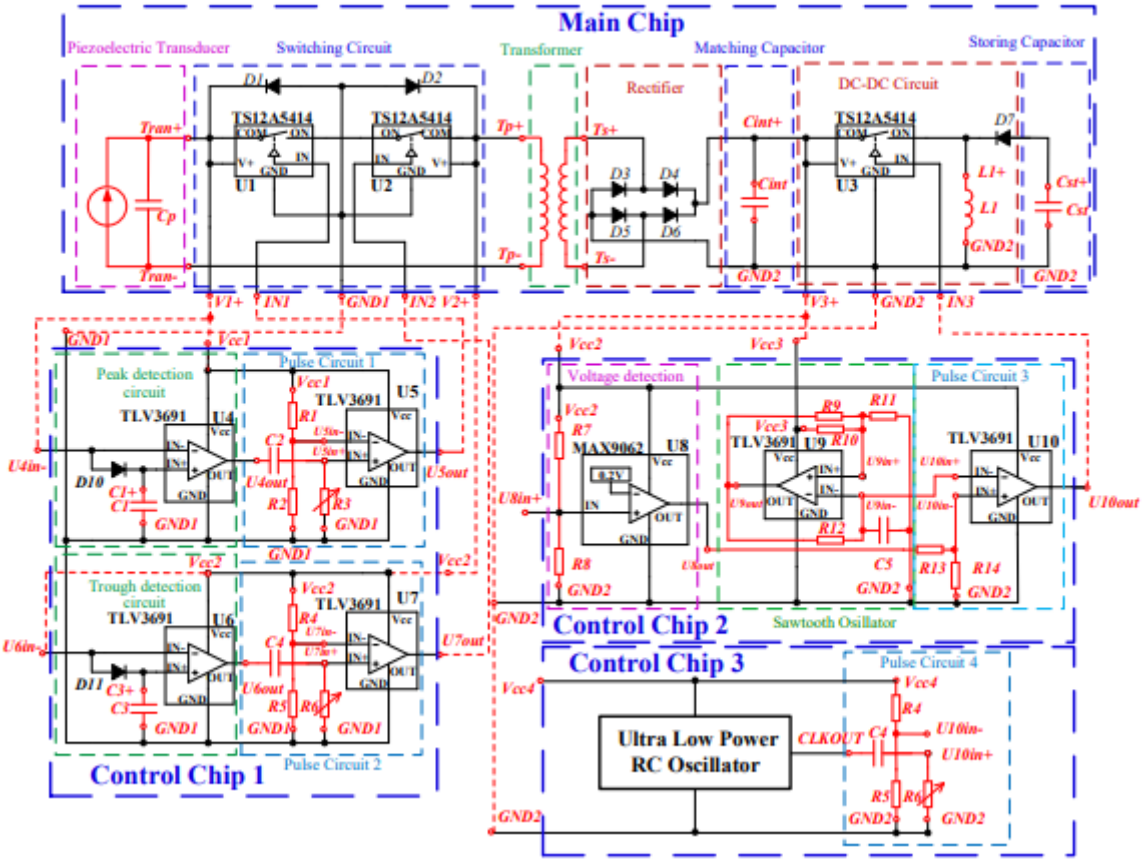


*Figure 1: Schematic overview of the proposed Power Management Circuit for a piezoelectric energy harvester.*

The main goal of this research work, proposed by Sensovann AS, is to design an Analog Switch and a Rectifier to be placed in the main chip of the PMC shown in Figure 1. To surpass all the harvesting limitations, designing these two circuits in CMOS technology is highly desirable to decrease the device's form factor, easily integrate with the energy harvester, achieve low power consumption, and mitigate the

unwanted leakage current (Colomer-Farrarons et al. 2008). Since the low frequency of the environmental sources does not match with the resonant frequency of the deployed energy harvester, the Analog Switch is designed to fulfil this gap by performing the up-conversion technique (P. Li et al., 2014). This method allows the energy harvester to reach the resonant frequency, ensuring that the maximum output power is transferred to the PMC. With the Analog Switch, it can be produced a higher frequency signal and a wide bandwidth to generate a higher output power under a weak vibration environment. In addition, due to the AC signal properties of the vibrational energy harvester, the Rectifier is designed to perform the AC/DC conversion in order to charge the supply unit properly. For the desired application, the key features of this work are high VCE and PCE.

## 2 State of the Art

The electrical characteristics of the environmental sources are not ideal for being transferred directly to electronic devices. Its signal variability leads to innovative approaches to performing a dynamic electrical matching between the energy harvesting system and the natural sources (Ruan, Chew, and Zhu 2017). Nevertheless, the vibrational energy harvesters have a working operation that does not match the environmental sources (Chew, Ruan, and Zhu 2019). To ensure maximum transferred power to the energy harvesting system, a technique needs to be employed to increase the low frequency of the environmental sources to match the resonant frequency of the deployed energy harvester, see Figure 2. Thus, section 2.1 describes the up-conversion technique and state of the art on analog switches and their respective switch-induced errors.

Since the vibrational energy sources produce AC signals, scavenging such vibrational energy requires a full-wave rectifier as a key circuit inside the PMC, which allows the AC/DC conversion to power the WSNs properly. In this way, section 2.2 presents the state of the art on the previous CMOS full-wave rectifiers for energy harvesting applications. Furthermore, since the leakage current is one of the main problems concerning the technology downscaling, it is important to be aware of it while designing a CMOS circuit. Thus, section 2.3 presents the leakage current in CMOS and some techniques to reduce it.

### 2.1 Analog Switch

The up-conversion technique aims to fulfil this gap in energy harvesters by reaching, in this application, the resonant frequency of the piezoelectric device (P. Li et al., 2014). Since the environmental frequencies and amplitude of the signals are very low, the operational frequency of the PMC needs to be increased in order to reach the harvester's resonant frequency. This frequency achievement produces a higher output power on the transducer. The analog switch is a possible solution to attend to this demand because it can receive low-frequency signals from the harvester in the Hz range and convert them into higher

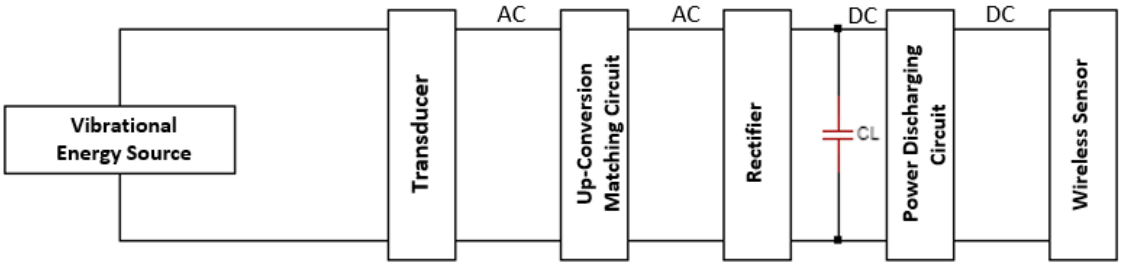


*Figure 2: Simplified block diagram of the PMC.*

frequencies in the kHz range (P. Li et al. 2014). Figure 3 shows an example of the frequency spectrum of the up-conversion output signal. According to P. Li *et al.* (2014), the resonant frequency of this vibrational energy harvester is at 3.2 kHz, as shown in the mentioned figure.

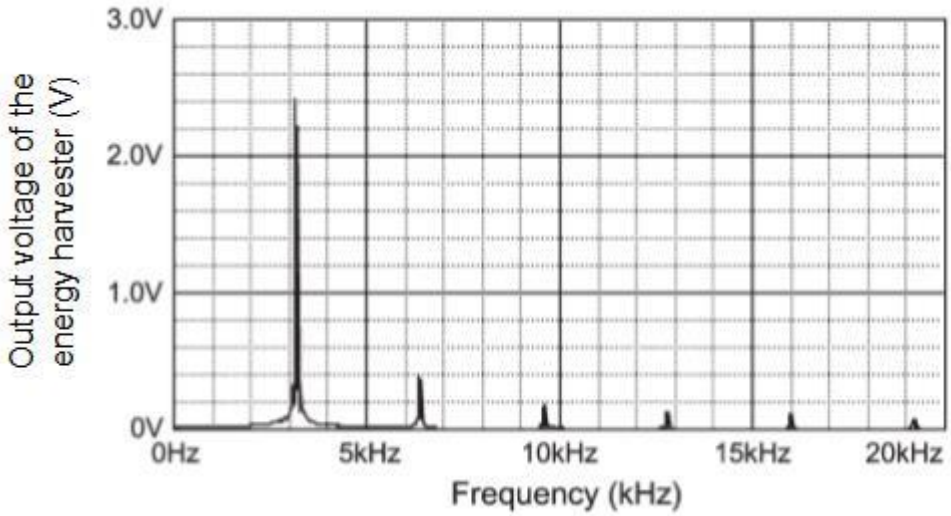


*Figure 3: Frequency spectrum example of the up-conversion output signal proposed by P. Li et al. ( 2014)*

Analog switches are a common building block in analog signal processing. When turned ON, they can conduct both analog and digital signals from the input to the output, regardless of the signal traveling direction. The structure of the conventional analog switch, known as TG, is presented in Figure 4. This circuit consists of an NMOS in parallel with a PMOS. While turned ON, it allows the signal to pass in either direction. When the circuit is OFF, it isolates the output from the input. The switch mechanism is controlled by an inverter or NOT gate, in which the input and output bias the gate of NMOS and PMOS, respectively. The working principle is simple: when CLK is high, and CLKN is low, NMOS and PMOS will be ON, and the current can flow through them. When the opposite happens, the circuit blocks the current

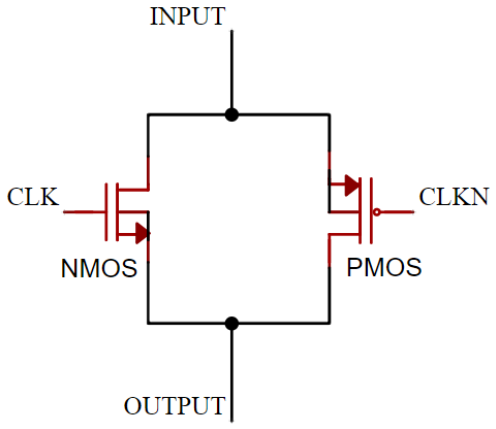


*Figure 4:Schematic of the TG.*

and isolates the output from the input (Baker 2019). Nevertheless, when the switch is ON, since the two transistors are in the deep-triode region, which means that $V_{DS} < 0.2 \cdot (V_{GS} - V_{th})$ (Sharroush and Abdalla 2021), the output voltage is highly dependent on the ON-resistance. As it is shown in Equation 1, the ON-resistance is dependent on the electron mobility μ, the unit capacitance of the oxide of the gate $\mathrm{C_{ox}}$, the ratio of the width to length$\left(\frac{W}{L}\right)$, the voltage between the gate and the source $\mathrm{V_{GS}}$, and the threshold voltage $\mathrm{V_{th}}$ (Chiranu et al. 2019). Therefore, it is important to manage these parameters in order to increase the efficiency of the analog switch. Figure 5 shows the power consumption of the TG with the W variation. As mentioned before, this analog circuit works as a frequency converter or frequency changer, which converts as AC signal of a specific frequency to an AC signal with another frequency. However, this structure presents some switch-induced errors that affect the performance of the Analog Switch. These errors will be presented in the next subsection.

$$R_{ON} = \frac{1}{\mu\, C_{ox}\, \frac{W}{L}\, (V_{GS} - V_{th})} \qquad 1$$

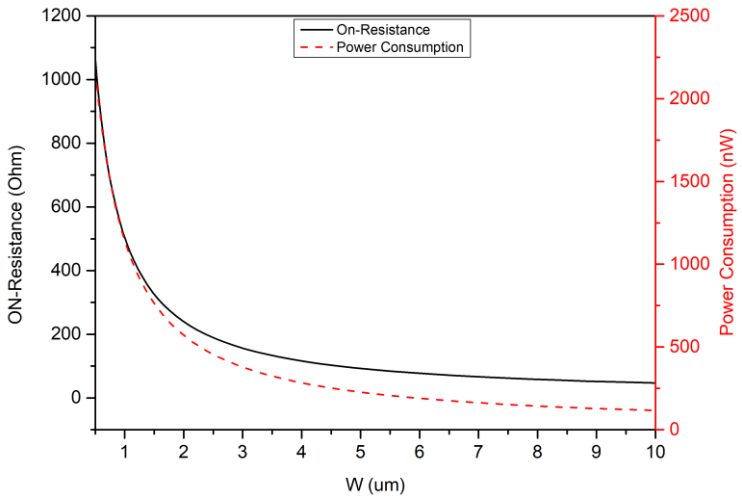


*Figure 5: TG's ON-resistance and Power Consumption behaviour with W variation.*

### 2.1.1 Switch-Induced Errors

The main problem of this type of circuit is the switch-induced errors. Thus, this subsection illustrates the main errors that affect the performance of analog switches, such as charge injection and clock feedthrough.

#### 2.1.1.1 Charge Injection

The structure of the sample and hold set by a simple NMOS switch is presented in Figure 6 (a). If a clock signal (CK) is applied to the gate of the NMOS transistor (M1), the gate-to-source voltage will be greater than the threshold voltage. Therefore, the transistor is switched on and starts operating in the triode region with approximately zero voltage across its drain and source terminals (George Wegmann, Yittoz, and Rahali 1987). During the time when the transistor is at ON state, it holds mobile charges in its channel. Equation 2 illustrates the amount of the charge ($Q_{ch}$) that the transistor can hold during its operation, where $W_1$ and $L_1$ are the effective channel width and length of the transistor, respectively, $C_{ox}$ is the gate capacitance per unit area, and $V_{th}$ is the threshold voltage.

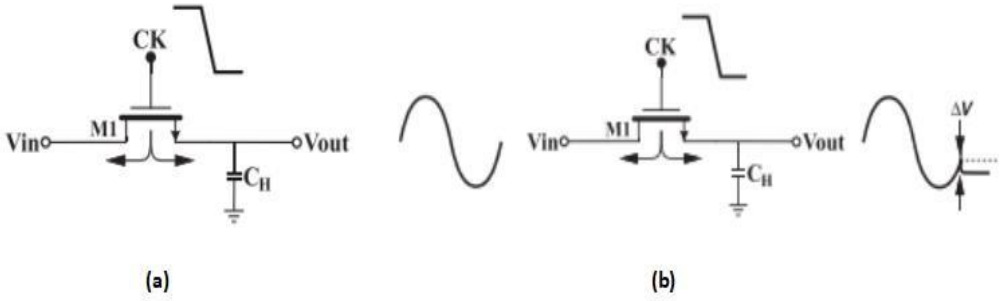


*Figure 6: (a) Structure of a simple analog switch and the charge injection when it is at OFF state. (b) Charge injection effect* (Naghavi, Sharifi, and Abrishamifar 2018).

$$Q_{ch} = W_1 L_1 C_{ox}(V_{DD} - V_{in} - V_{th}) \quad (2)$$

Subsequently, once the switch is turned off, the mobile charges flow out through the source and drain terminals since there is no longer an electrical force to attract the channel charge.

The charge injected to the drain terminal presented in Figure 6 (b) is absorbed by the input voltage source since the impedance is lower than the output; therefore, any error value is produced on the holding capacitor. On the other hand, there are always a few charges injected into the source terminal, which affects the stored value on the holding capacitor and produces an error voltage (G Wegmann, Vittoz, and Rahali 1987). Equation 3 presents the resulting error voltage due to charge injection if it is assumed that the fraction α of $Q_{ch}$ is eventually stored in the holding capacitor ($C_H$).

$$\Delta V_{CI} = \frac{\alpha Q_{ch}}{C_H} = \frac{\alpha W_1 L_1 C_{OX}(V_{DD} - V_{in} - V_{th})}{C_H} \quad (3)$$

As presented in the previous equation, the charge injection error voltage is signal-dependent and causes nonlinear distortions (Patel and Sadiwala 2021). For instance, Figure 6 (b) shows that the error for an NMOS switch appears as a negative spike at the output.

#### 2.1.1.2 Clock feedthrough

Besides charge injection, clock feedthrough is also an error to be aware of while the analog switch is being designed. A MOS switch couples the clock transitions to the holding capacitor ($C_H$) through its gate-source or gate-drain overlap capacitance.

As shown in Figure 7, this phenomenon introduces an error in the output voltage as a result of this overlap capacitance. Assuming that this capacitance is constant, the error voltage due to the clock feedthrough can be stated by Equation 4, where $C_{OV}$ is the overlap capacitance per unit width. The equation shows that the output error is independent of the input voltage. Therefore, it can be concluded that the offset value is directly proportional to the clock signal amplitude (Xu and Friedman 2002).

$$\Delta V_{CFT} = V_{CLK} \frac{W_1 C_{OV}}{W_1 C_{OV} + C_H} \quad 4$$

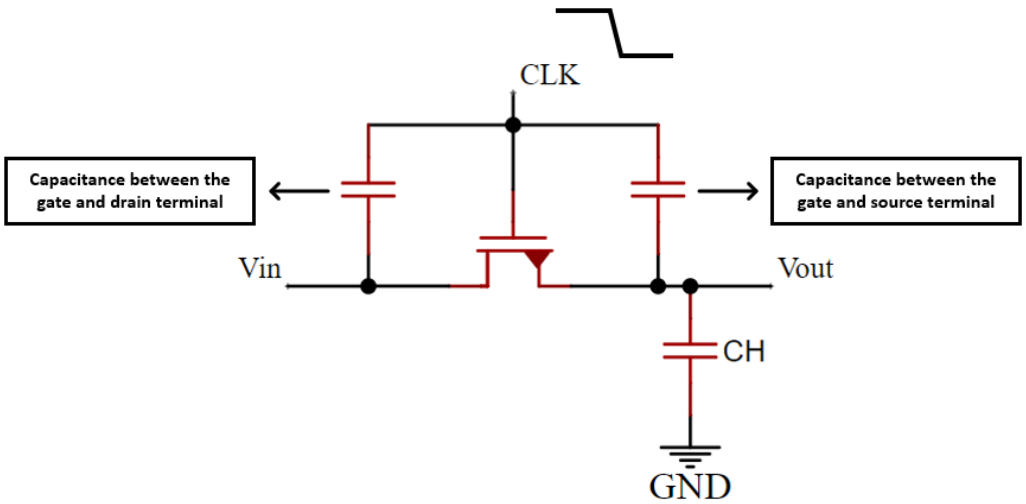


*Figure 7: Clock feedthrough in a simple analog switch.*

### 2.1.2 Previous Works

For low input voltage and low input frequency applications, analog switches must have a good performance, low power consumption, high linearity, and a low-frequency operation. Several works have been proposed to improve the performance characteristics of analog switches. Yang (2005) proposed a

low-voltage and low distortion switch due to a low THD. Then, the bootstrap technique was proposed to alleviate the problem with poor conduction and varying ON-resistance (H. Chen et al. 2014). This technique aims to control the switching operation with two non-overlapping clock signals (CLK and NCLK). The concept of this type of analog switch is illustrated in Figure 8 (a). During the standby operation (CLK is high, NCLK is low, SW1, SW2, and SW4 are on), the capacitor $C_1$ is charged to $V_{dd}$ and likely acts as a floating battery in order to bootstrap the gate voltage. Then, in the active mode (CLK is low, NCLK is high, SW3 and SW5 are on), the input signal charges the gate voltage of the switch equal to $V_{dd} + V_{in}$, resulting in an overdrive voltage nearly constant over the input signal voltage range.

Figure 8 (b) shows the traditional bootstrap switch implemented at the transistor level. During the OFF state, when clkb is high, MN2 is ON due to the action of the voltage doubler and charges the capacitor $C_3$, together with MN3. Then, transistor MP5 forces MP4 to turn off, and MN10 also forces MS, MN8 and MN7 to turn off. Nevertheless, parasitic capacitances of transistors MP4, MN7, MN9, and MN10 share the charge from $C_3$, which makes $V_{gs}$ less than $V_{dd}$. During the active state, when clkb is low, MN6 will turn on, pulling down the gate of transistor MP4, supplying the MN8 and MS gates. Since MN8 is ON, it tracks the input signal $V_{in}$ and then MS gate and its gate will have a voltage closer to $V_{in} + V_{dd}$. Thus, MS will have enough gate voltage to turn on during the active state.

To improve the characteristics mentioned above of the traditional bootstrap switch, Chen (2014) proposed another bootstrap switch with high speed, low nonlinear, and lower ON-resistance. Also, in order to reduce the number of transistors on-chip, Nazzal (2016) projected a bootstrap analog switch without a clock multiplier circuit and with low power consumption and low distortion caused by a low THD.

To eliminate the switch imperfections on the last subsection, Naghavi *et al.* (2018) proposed the structure of an analog switch presented in Figure 9. The elimination of the switch-induced errors in the proposed design is provided through an auxiliary path in parallel with the main signal path similar to the complementary switch. The novelty of this research work is using NMOS devices to avoid mismatches of different types of transistors. As shown in Figure 9, the main signal path of the proposed switch is formed by the transistors M1 and M1S. During the ON phase, when the clock signal CK is high, these transistors are in on-state. In this phase, a low-resistance path is provided, and the output follows the input voltage. The OFF-resistance is extremely high during the OFF phase due to a pseudo-resistor (MR1, MR2, and MR3), which is also a novelty of this work. Equation 5 proves that this circuit can eliminate the charge injection and clock feedthrough by connecting MS1 and MS2 in parallel.

$$+V_{CK}\frac{WC_{ov1S}}{WC_{ov1S}+C_H}-V_{CK}\frac{WC_{ov2S}}{WC_{ov2S}+C_H}=0 \qquad 5$$

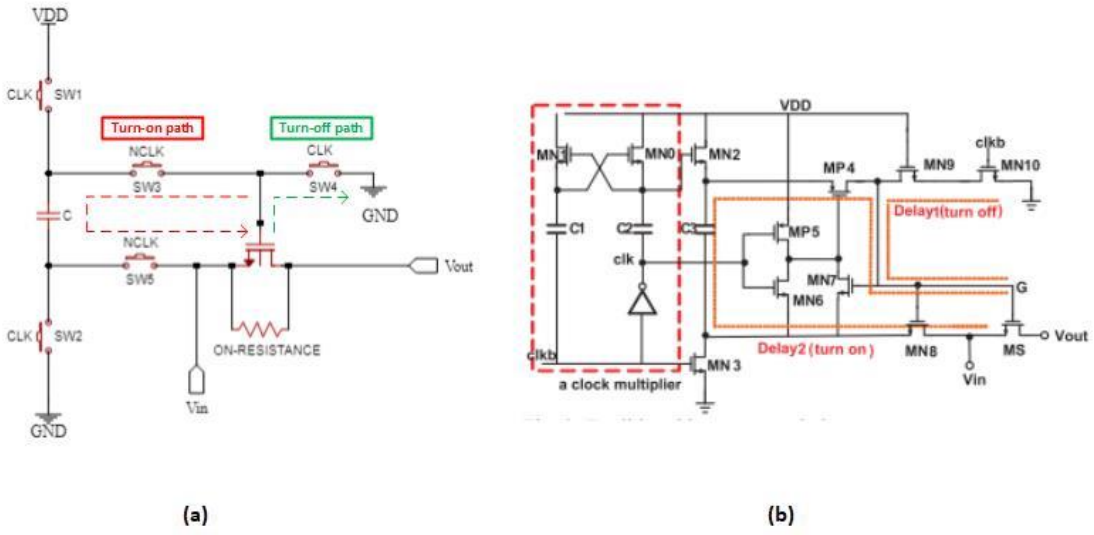


*Figure 8: Bootstrap analog switch (a) high level representation (b) traditional bootstrap switch represented in transistor level by Chen (2014).*

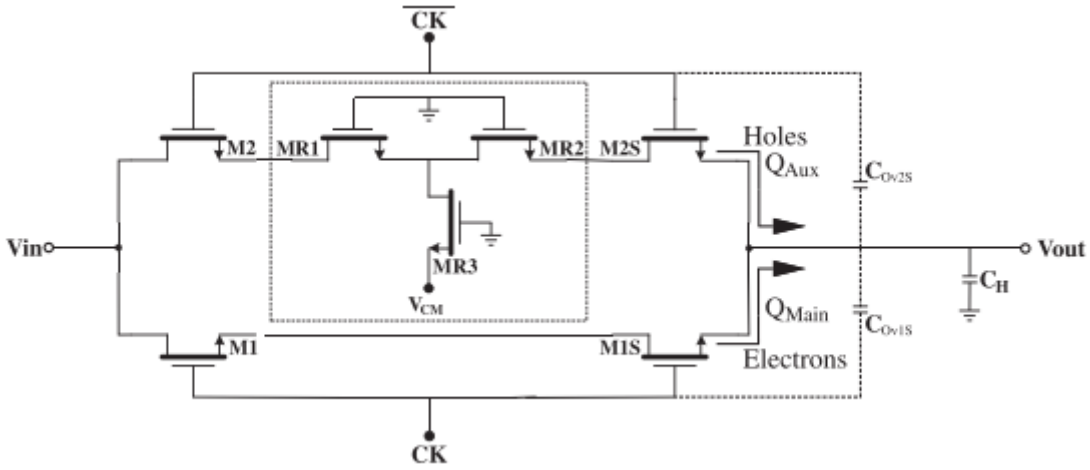


*Figure 9: Structure of the circuit proposed by* Naghav *et. al* (2018).

However, besides the aforementioned characteristics, those circuits are mostly designed for analog-to-digital converters, with high operational frequencies, in MHz or GHz range, and low signal distortion are highly demanded. Therefore, those circuits cannot be used for this type of application due to different demands of working principles such as low input frequency, the ability to increase the operating frequency and receive nonlinear signals.

## 2.2 Full-wave Rectifiers

Rectifiers essentially convert AC to unregulated DC in electrical power processing systems. The purpose of a rectifier in a micropower energy harvesting system is to efficiently process and transfer the small amount of ambient energy extracted by the vibrational energy harvesters in AC form to predominantly DC microelectronic load. This efficient conversion should involve a device that only allows one way of current flow. Otherwise, the capacitor load cannot be charged properly. Also, it must block or mitigate any reverse leakage current from the capacitor load to avoid undesired power losses.

The rectifier requires a low input voltage operation as practical micropower energy harvesters typically produce voltage levels around hundreds of millivolts (Toshiyoshi et al. 2019). Furthermore, the DC loads are generally in the form of a handheld, wearable, implantable, or wireless sensing devices that will require a battery-free small form factor to operate unobtrusively. Therefore, this energy autonomy requires ultra-low power rectifier operation and hence a high PCE to maximize the transfer to the load capacitor. These considerations resulted in various rectifier designs focusing on circuit topology and switch parameters for specific energy harvesting applications.

Conventional rectifiers are designed by using diodes and capacitors. The full-wave rectifier with a diode bridge is suitable for high voltage applications since the diode forward voltage drop from 0.7 V to 1 V (Q. Li, Wang, Niu, et al. 2014). However, this cannot be accepted in a low voltage energy harvesting system.

Firstly, it is important to see how the full-wave rectifier works. The full-wave rectifier presented in Figure 10 (a) must be employed when it is necessary to rectify both half-cycles of the input voltage. This circuit consists of four diodes and stands out for giving small output ripple voltage, commonly used in high voltage applications, where the diode forward voltage is between 0.7 V and 1 V. For low-voltage applications, these values result in large voltage losses, reducing the PCE significantly.

Current flows in the same direction through the load resistor for both polarities of the input voltage by using two forward-biased diodes in series with $R_L$ at any time, as presented in Figures 10 (b) and (c). In Figure 10 (b), the input voltage has a polarity that makes the top input terminal positive; hence, only the two diodes shown are forward biased and are conducting. As the input voltage reverses, the bottom terminal becomes positive. Then, the remaining two diodes conduct, while the previous two are open-circuited, as shown in Figure 10 (c). The result is that current flows through $R_L$ at all times, as shown in Figure 10 (d). However, these conventional full-wave rectifier structures present a forward voltage drop

around 0.7 V. Therefore, since the output power of the energy harvester is low, the high forward voltage drop required by the full-wave diode bridge and Schottky diodes rectifiers limits their use on these low power applications (Hashemi, Sawan, and Savaria 2012).

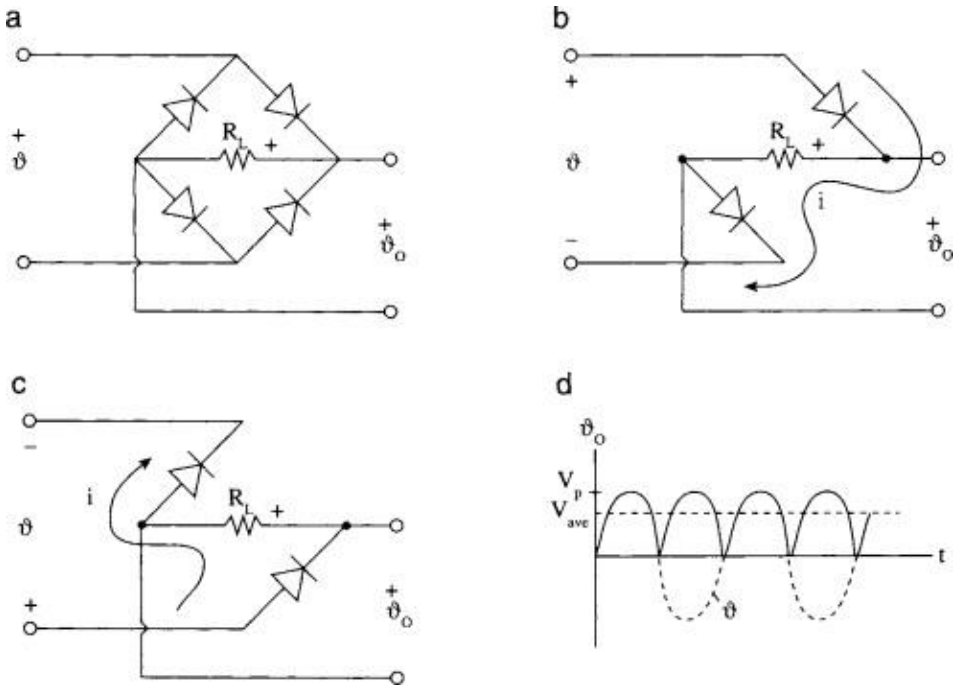


*Figure 10: (a) A full-wave bridge rectifier (b,c) Conduction path when the input polarity is as shown, (d) Output voltage Vo of the full-wave rectifier*(M. Plonus 2020).

Several CMOS rectifiers have been proposed throughout the last years to overcome the high forward voltage drop issue mentioned before. Diode-connected MOS transistors came up to replace diodes in standard CMOS processes, which is revealed to be a solution to make fully integrated low input voltage rectifiers (Gomez-Casseres et al. 2016). CMOS rectifiers can be classified into either passive or active configurations. On the one hand, passive rectifiers perform the full-wave rectification without controlling the reverse leakage current that comes from the load. On the other hand, active rectifiers use passive configurations to achieve the rectification while attaching them with an extra circuit to control the reverse leakage current depending on the input and output voltage conditions. Thus, the following sections present the state of the art of these two configurations.

### 2.2.1 Passive Rectifiers

As it was previously mentioned, classical full-wave rectifier circuit topologies use diodes for switching. Since their forward voltage drops are high (typically 0.7 V), this topology cannot be applied for energy harvesting applications. Therefore, different standard CMOS passive rectifier techniques were proposed

to reduce the diode forward voltage drop, which the goal was to improve the power and voltage conversion efficiency. This subsection presents the description of different types of rectifier topologies and the comparison between them.

#### 2.2.1.1 Gate Cross-Coupled Full-Wave Rectifier

Conventional full-wave bridge rectifiers introduced by Rakers *et al.* (2001) use four switches to create two conduction paths that an AC input produces a DC output, $V_{out}$ (Figure 11). These are two diode drops in each conduction path thereby reducing the useful input voltage range. This can be achieved by reducing the threshold voltage drop of the diode-tied connection in the conduction path from the threshold voltage to the voltage drop across the diode during the forward conduction (Hashemi, Sawan, and Savaria 2012). Colomer-Farrarons *et al.* (2008) proved that PCE improves to around 70% compared to the conventional topology bridge PCE of about 50% with a piezoelectric micro-generator with 2.5V open-circuit voltage. This is caused by the cross-connection of gates, which generates the gate voltage swing to be larger than the diode-tied connections, leading to an increase in the overall forward current. However, this topology still lacks efficiency due to the threshold voltage drop across the diode-connected in each conduction path (Gomez-Casseres et al. 2016).

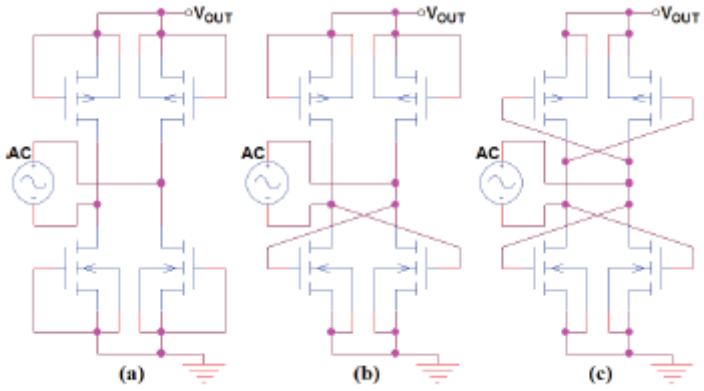


*Figure 11: CMOS Full-wave bridge rectifiers: (a) conventional topology, (b) gate cross-coupled topology, and (c) fully cross-coupled* (Yeo et al. 2015).

#### 2.2.1.2 Fully Cross-Couple Full-Wave Rectifier

Since the one threshold voltage drop still occurs in the previous topology, the fully cross-coupled full-wave rectifier was proposed in order to reduce this voltage drop of all the diodes in the conduction path (Colomer-Farrarons et al. 2008; Wahab et al. 2017), see Figure 11 (c). Therefore, the voltage and power efficiency also increase with this improvement.

Furthermore, to improve the linearity of the ON-resistance in PMOS, the body bias technique was added to the NVC in Yoon *et al.* (2017) with wide operation voltage where the bulk terminal of PMOS was connected to a beta-multiplier voltage reference. This technique proved to improve the NVC efficiency in the low input voltage region.

#### 2.2.1.3 Voltage Multiplier

This topology can rectify a low-voltage AC to a higher voltage DC using self-commutating switched-capacitors for charge storage and transfer. As shown in Figure 12, this half-wave voltage doubler doubles the input voltage by clamping a capacitor voltage to the input voltage. During the negative half cycle of the input, the capacitor is charged to the input peak voltage minus the threshold voltage of the diode in the charging path. In the positive half-cycle, the capacitor acts as a DC source in series with the input. Assuming that the capacitor is large enough to keep the output voltage almost constant throughout the discharging in the positive half-cycle, the output voltage of this topology is twice the input voltage minus two diode threshold voltage drops, one each in charge storing and charge transfer phase. Increasing the capacitor value leads to an increase in the charge transfer, producing a larger voltage across an output load due to the reduction of the capacitive reactance. Even though this topology can get a higher output voltage, the current will be lower due to this voltage amplification. Also, large capacitors are not suitable for fully integrated designs and will need to be off-chip. Therefore, this topology is not suitable for energy harvesting applications.

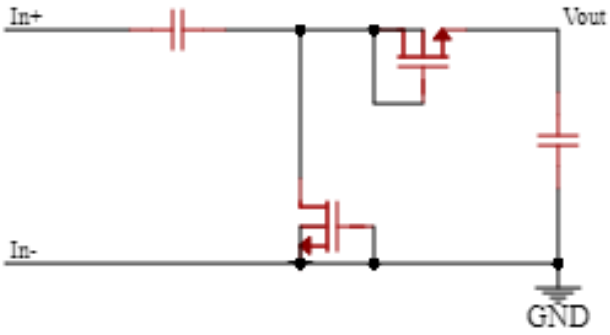


*Figure 12: Voltage doubler.*

Table 2 presents the performance comparison between all the previous topologies that Yeo et al. (2015) presented. The features of VCE and PCE were calculated according to Equations 6 and 7. It can be concluded that the topology that showed the best features for harvesting applications was the fully gate cross-coupled since the voltage operation is lowest compared to the other topologies. Besides that, this rectifier presented a higher PCE, which means that the efficiency of the circuit is the highest.

$$VCE = \frac{V_{OUT}}{V_{IN}} \cdot 100\% \qquad 6$$

$$PCE = \frac{\int_t^{t+T} V_{OUT}(t) \cdot I_{OUT}(t)dt}{\int_t^{t+T} V_{IN}(t) \cdot I_{IN}(t)dt} \cdot 100\% \qquad 7$$

*Table 2: Comparison of different full-wave rectifier topologies* (Yeo et al. 2015).

| CMOS Passive Rectifier Topology | Performance Metrics | | |
|---|---|---|---|
| | PCE (%) | VCE (%) | Minimum input voltage (mV) |
| Conventional full-bridge | 27.74 | 7.21 | 500 |
| Gate cross-coupled | 57.43 | 23.76 | ~50 |
| Fully cross-coupled | 82.12 | 40.75 | ~20 |

Moreover, these passive rectifiers present a critical disadvantage. It is impossible to control the reverse leakage current when a capacitor is used as a load, damaging the overall device. Thus, it is required to use an active stage to control this unwanted reverse leakage current.

### 2.2.2 Active Rectifiers

Active rectifiers increase efficiency throughout active signal control mechanisms that interfere with the rectification process. Those use controlled switches (working as an ideal diode) and high-gain comparators, providing reduced forward voltage compared to other mechanisms described above. Nevertheless, these control circuits constitute an additional power consumption for the system, in some situations, can require a limited power supply. Therefore, low power consumption and low voltage operations are basic needs for active rectifiers (Niu, Huang, and Jiang 2012). Furthermore, these circuits aim to behave as an ideal diode, implying no forward voltage drop and no reverse current.

An active rectifier is proposed in (Niu, Huang, and Jiang 2012) with a body input comparator and a body bias technique used to allow low voltage operation and high voltage and power conversion efficiency, see Figure 13. This circuit is composed of a passive stage (NVC) to convert the AC signal into a DC and an active diode, with a body comparator that controls its switching action. This comparator receives as an input the output signal from the NVC and the capacitor, then if $V_{out} < V_{NVC}$, the comparator keeps the diode at ON state. However, if $V_{out} > V_{NVC}$, the comparator turns off the diode, which blocks the reverse current from the load. This rectifier can achieve a peak voltage efficiency of over 96% and the maximum power efficiency of over 94%.

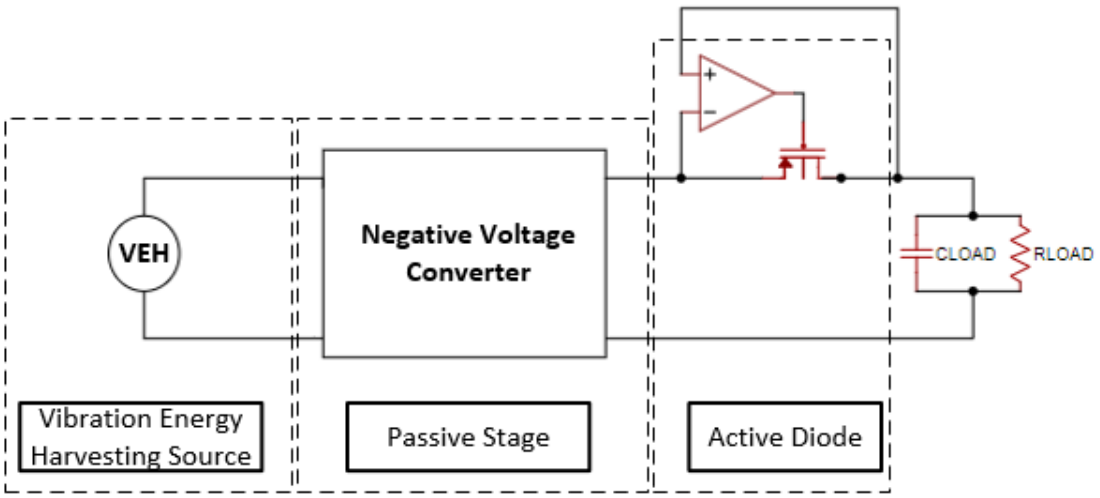


*Figure 13: Schematic of an active CMOS rectifier.*

Figure 14 presents the schematic of the active stage of the rectifier proposed by Niu *et al.* (2012). This comparator consists of three parts: the bias circuit part (M11 and M12), body-input circuit part (M1-M4), and inverter output circuit (M5-M10). Moreover, it was added to the PMOS switch (active diode) a body bias technique (M21 and M22) to restrain latch-up and a MOSFET bypass diode to ensure a safe start-up of M1.

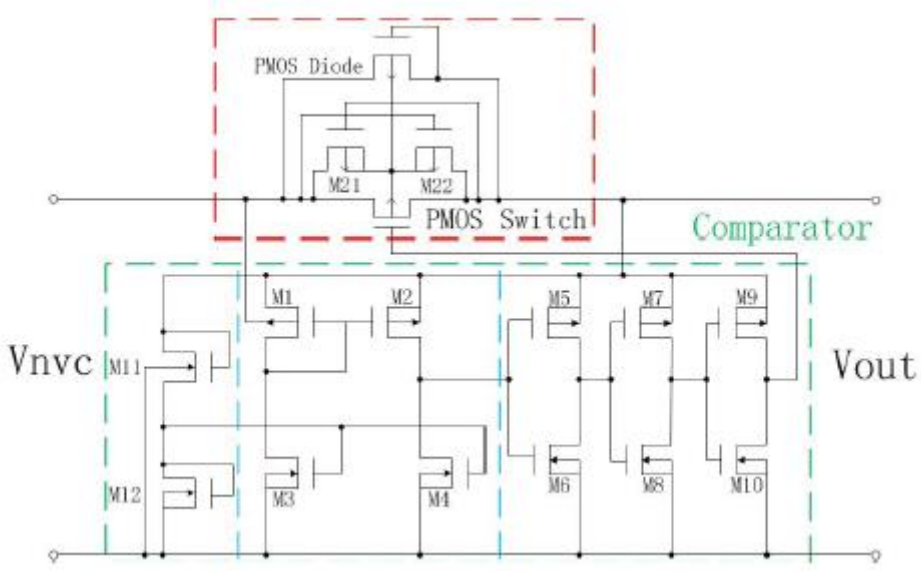


*Figure 14: Schematic of the active stage (Niu, Huang, and Jiang 2012).*

Peters *et al.* (2011) proposed an active rectifier with a bulk-input comparator technique for ultra-low-voltage energy harvesting systems. This rectifier was designed to work with input source amplitudes around 0.5 V. This structure is composed of two stages: the NVC and the active diode. In addition, the authors added a body bias block in the negative voltage converter stage (Figure 15 (a)) to reduce the threshold voltage of PMOS, which reduces the minimum operation voltage to 0.3 V since the transistors will only turn on when the input voltage is higher than the threshold voltage. Figure 15 (b) shows the structure of the bulk-input comparator. This comparator uses only two stacked transistors, and no tail source is used in this circuit (Peters et al. 2011). However, when the input voltage is higher than the output voltage, the PN junctions between the bulk and source terminal of the input transistor will be turned on. Consequently, the bulk leakage current will increase, which compromises the efficiency of the circuit (Q. Li, Wang, Ding, et al. 2014). In addition, the proposed rectifier in Peters et al. (2011) has a frequency band not suitable for the application of this work.

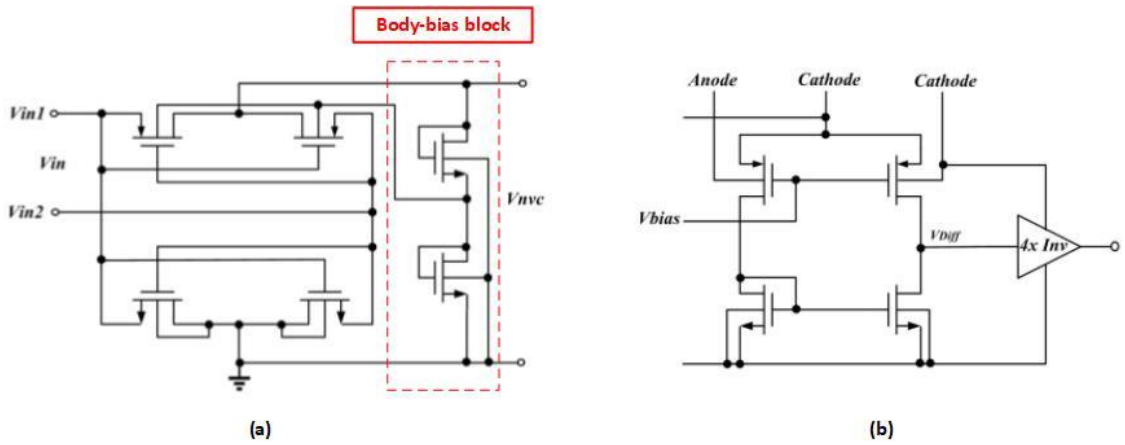


*Figure 15: Schematic of the ultra-low voltage rectifier (Peters et al., 2011) (a) negative voltage converter with a body-bias block; (b) input-bulk comparator.*

In contrast, the frequency bandwidth in the following research papers (Q. Li, Wang, Ding, et al. 2014; Guo and Lee 2009; R. C.-H. Chang et al. 2020; Oh et al. 2017) corresponds to the desired application. The authors use two active diodes to control the reverse current that flows through the two NMOS in each input cycle and two PMOS in cross-coupled to provide the conduction path. However, the dynamic range does not meet the requirements to achieve a low-power consumption. Furthermore, the proposed rectifiers cannot work for input voltages lower than 1 V, which is critical for energy harvesting applications(Q. Li, Wang, Ding, et al. 2014). In R. C. H. Chang *et al.* (2017), the authors designed a fully active configuration using NMOS and PMOS to ensure that the reverse leakage current through the PMOS input source is zero. The main disadvantage of this configuration is when the NMOS devices turn on simultaneously, which leads to power losses. Therefore, Chang *et al.* (2020) proposed a rectifier with a third comparator to eliminate the oscillations of NMOS, which avoids the two active diodes turning on/off simultaneously. Nevertheless, the PCE is only high for an input voltage around 4.88 V.

However, the main limitation of these configurations is that they cannot decrease the $V_{SG}$ of the main transistor, and thus enhancing the output voltage stored on the load capacitor. Therefore, an extra circuit is demanded to smooth the threshold voltage effect of this transistor to overcome these drawbacks.

### 2.2.3 Threshold Cancellation Topologies

Several threshold cancellation topologies were proposed to enhance the output voltage by reducing the threshold voltage effect of the main transistor of the rectifier (Koji Kotani and Ito 2007; K Kotani and Ito 2009; Khan and Choi 2017). The threshold voltage is a process parameter dependent on the type and thickness of oxide (Hashemi, Sawan, and Savaria 2012). Low threshold voltage MOSFETs present a high leakage current caused by the low substrate doping, which leads to an increase in power consumption

and reliability problems. Thus, these threshold cancellation techniques are used to avoid those types of MOSFETs since it is only needed to smooth the threshold voltage effect when the main pass transistor is ON.

Hashemi *et al.* (2012) proposed a low-voltage CMOS rectifier to perform this technique using the bootstrap technique, see Figure 16 (a). This bootstrap circuit can achieve high voltage conversion efficiency by reducing the voltage drop. In this structure, M5 works as a diode and provides the current through M7 to charge the bootstrapping capacitor ($C_{B1}$) at the start up state. Then, the power stored at $C_{B1}$ will be applied to the gate of M3, which works as a switch. When the input voltage is larger than the output voltage by one threshold voltage, M5 will be turned on and the current flows through M5 and M7 to charge the boostrapping capacitor. By increasing the voltage helded on the gate of M3, the threhsold voltrage effect will be reduced, which leads to a voltage drop reduction. However, even if the minimum operation voltage can be as smal as 0.8 V, VCE and PCE are not high enough, especially the power efficiency, which is only around 30% when the input voltage is lower than 0.8 V. This low PCE is caused by the high reverese leakage current, which degrades the overall performance of the system.

An active bootstrapping rectifier is presented in (Lee, Liao, and Lee 2019) to overcome the issues of the previous work, see Figure 16 (b). This topology uses two active diodes to control the conduction path for each input cycle and a bootstrap technique to reduce the threshold voltage of both main pass PMOS. Also, an AVC is set in this work to adjust the gate voltage of the main pass PMOS, which reduces the voltage drop by reducing the ON-resistance. Besides reducing the reverse leakage current, the PCE of this configuration can still be improved for input voltages smaller than 1 V. To overcome the drawbacks mentioned above, in Vithya Lakshmi *et al.* (2021), a dual switching technique replaced the two active

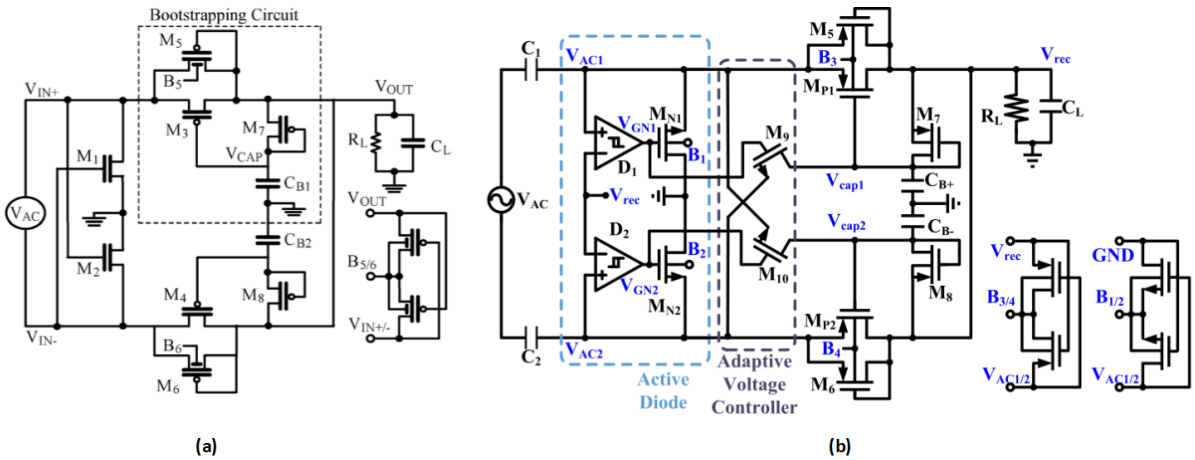


*Figure 16: (a) Full-wave bootstrap rectifier* (Hashemi, Sawan, and Savaria 2012)*; (b) Active bootstrapping rectifier* (Lee, Liao, and Lee 2019).

diodes. This approach can maintain a constant gate bias on the two main NMOS transistors, avoid the reverse leakage current, reduce the area on-chip, and enhance the PCE for low voltage applications. However, high values for PCE can only be obtained for input frequencies around 20 kHz.

## 2.3 Leakage current in CMOS

Initially, in the CMOS process, the high voltage supply value caused the electric field to rise, reducing the device's reliability. By decreasing the channel length, the MOSFET can operate with lower voltages due to lowering the threshold voltage, and thus the low power demands can be reached. However, the downscaling of the channel length has led to new challenges such as short-channel effects, high leakage current, and static power dissipation, which deteriorates the circuit frequency and performance. Therefore, it is necessary to raise the performance to an acceptable level. To reach low power consumption, further minimization of power supply and channel dimensions must occur, approaching the voltage supply value towards the threshold voltage. Since a significant portion of the total power consumption is related to leakage current, it must be managed and used as the primary operational current to satisfy low power requirements.

As the transistor length decreases in size, at the same time, some challenges emerge, such as short-channel effects, high leakage current, and static power dissipation. Therefore, designing a CMOS circuit with reduced technology involves a trade-off between chip area, the performance of the circuit, and dynamic power dissipation. However, special attention must also be given to static power consumption since it is ideally expected that the CMOS circuit does not consume power while it is at OFF state. Figure 17 shows the leakage power consumption trend with the technology downscaling. Thus, it is important to manage these metrics to maximize these deep submicron levels (Bohr and Young 2017).

$$P_{Dynamic} = \alpha \cdot C_L \cdot {V_{DD}}^2 \cdot f_0 \quad (8)$$

$$P_{Static} = I_{leakage} \cdot V_{DD} \quad (9)$$

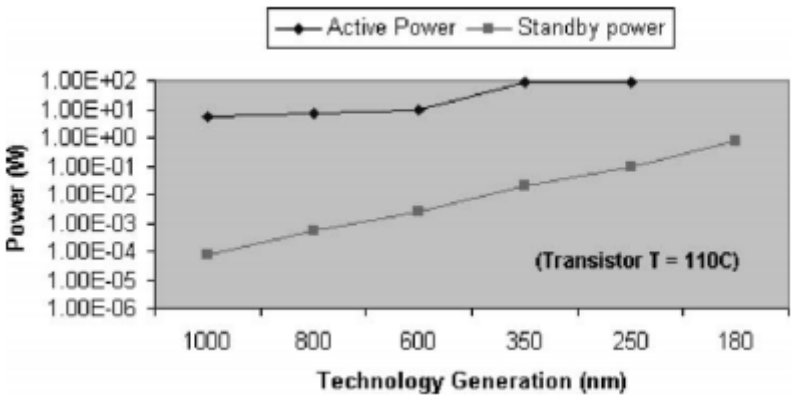


*Figure 17: Leakage power consumption behaviour with technology downscaling* (Hanchate and Ranganathan 2004).

According to Equation 8, $P_{Dynamic}$ is defined as the power dissipation when the circuit is working (active mode), where α is the switching activity, $C_L$ is the gate capacitance, $V_{DD}$ is the voltage supply, and $f_0$ is the operating frequency. $P_{Dynamic}$ results from charging and discharging the capacitances as a result of the switching activity of the transistor. On the other hand, the continuous scaling of the MOSFET to deep sub-micron channel length has delivered lesser area and low capacitance effects leading to negligible dynamic power dissipation(Gupta and Kahng 2003).

$P_{Static}$ is the power consumption when the circuit is at OFF state, where $I_{leakage}$ is the off-state leakage current and $V_{DD}$ is the voltage supply, see Equation 9. $P_{Static}$ is mainly the off-state leakage current that leaks through the transistor even in the inactive mode (Kim et al. 2003). This power consumption is an important feature to consider when CMOS technology is scaling down since its dominance increases with the shrinking of the processor technology. Unfortunately, smaller geometries increase the leakage current, and therefore, static power begins to dominate the power consumption equation in chip design (Kim et al. 2003).

This off-state current is influenced by many parameters, such as the threshold voltage, channel length, channel/surface doping profile, drain/source junction depth, gate oxide thickness, and $V_{DD}$ (Roy, Mukhopadhyay, and Mahmoodi-Meimand 2003). When CMOS circuits are being designed using short-channel transistors, low power supply levels are required to reduce the static power consumption, influencing the weak inversion state (or subthreshold region). Since the threshold voltage is also downscaled, it consequently increases the portion of off-state leakage current (De and Borkar 2000). Moreover, as the drain voltage increases, the channel depletion region widens, which results in a significant increase in the drain current. Thus, from this point of view, the off-state leakage current is caused by the DIBL, which is an undesirable field penetration among the source and drain that generates the unwanted current through the channel (Qu et al. 2011). This unwanted current destroys the classical infinite input impedance assumption of the MOSFET and affects the efficiency of the circuit by increasing the overall power consumption (Roy, Mukhopadhyay, and Mahmoodi-Meimand 2003). Therefore, leakage current reduction techniques must be addressed to improve the performance of the CMOS circuits.

### 2.3.1 Leakage Current Reduction Techniques

As technology scales down to deep submicron levels, leakage power consumption has proved to be a major concern in designing CMOS VLSI circuits due to the reduced threshold voltage and device form

factor. The voltage supply needed to be scaled to overcome the dynamic power and reliability issues. To keep an acceptable level of circuit performance, the threshold voltage also needs to be scaled. This reduction leads to an exponential rise of the leakage power consumption to a level that might overwhelm the dynamic power consumption (Chun and Chen 2010; Lahbib et al. 2015). Therefore, it is demanded to be aware of some existent approaches to minimize and estimate this unwanted current in both ON and OFF state in MOS transistors (Agarwal et al. 2004). The reduction in leakage current can be achieved in two ways: process and circuit-level techniques. The first one is achieved by regulating the transistor dimensions (length, oxide thickness, junction depth, etc.) and the doping profile. Threshold voltage and leakage current can be managed at the circuit level by applying different techniques to control the transistor voltage terminals (source, drain, gate, and bulk) (Roy, Mukhopadhyay, and Mahmoodi-Meimand 2003).

This subsection presents some circuit-level approaches proposed to minimize the leakage current, such as multi-threshold voltage designs, voltage supply scaling, and transistor stacking.

#### 2.3.1.1 Multi-threshold voltage designs

This process-level approach minimizes the subthreshold leakage current, which provides both high and low threshold voltage transistors in a single chip (see Equation 10). Thus, the high-threshold transistor mitigates the subthreshold leakage, while the low threshold transistors are used to achieve high performance depending on the circuit's behaviour (Roy, Mukhopadhyay, and Mahmoodi-Meimand 2003).

$$I_D = I_{D0} \cdot \frac{W}{L} \cdot \exp\left(\frac{V_{GS} - V_{th}}{n \cdot V_T}\right) \qquad 10$$

Multiple-threshold voltages values can be achieved by varying different parameters regarding the fabrication processes, see Figure 18. Thus, threshold voltage depends on the channel doping profile, gate oxide thickness, and channel length.

This technique is mainly used to keep higher performance levels while decreasing the leakage power consumption during standby and active operation modes. The advantage of this technique is that it avoids additional circuits, delays, and extra area on-chip(Kim et al. 2003). One practical example is on CMOS rectifiers since the high threshold transistors can be used on non-critical paths to reduce the leakage current. At the same time, the performance is reached with low threshold transistors to decrease the overall voltage drop of the circuit. Further disadvantages of applying this technique in the proposed circuits will be given in section 3.2.

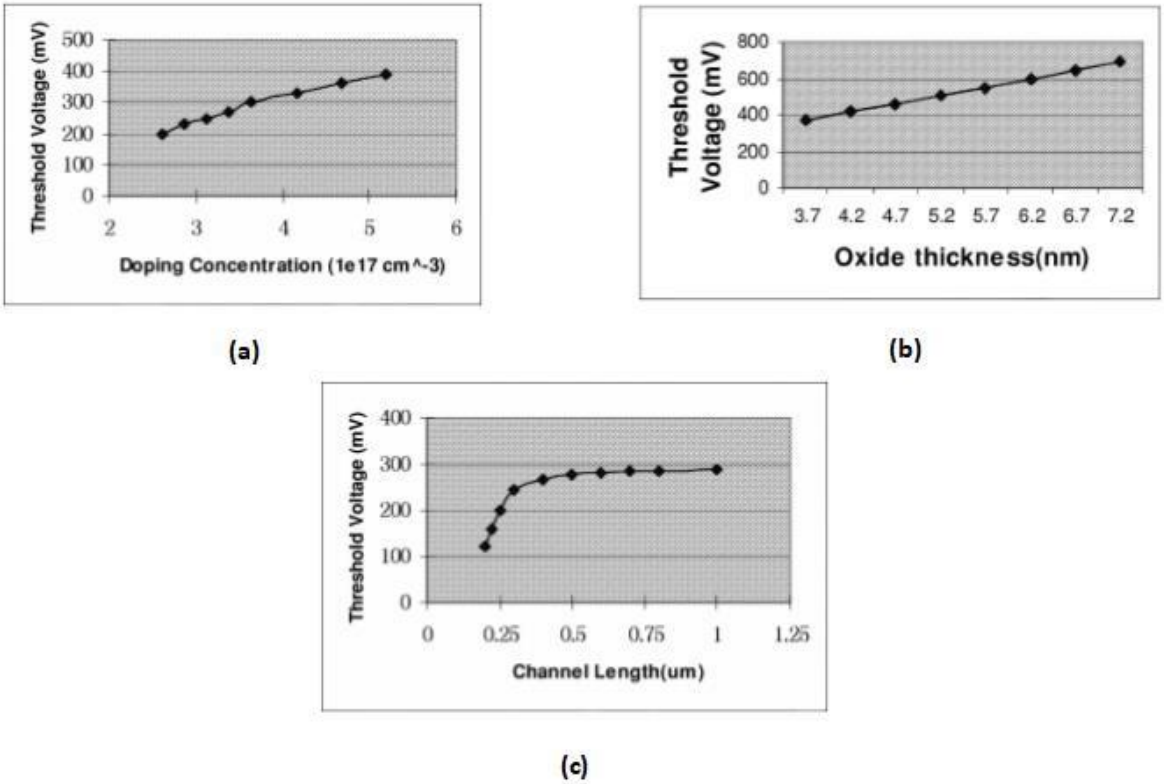


*Figure 18: Fabrication process parameters that influence the threshold voltage (a) channel doping concertation (b) oxide thickness (c) channel length.*

### 2.3.1.2 Supply Voltage Scaling

This technique is used to reduce the dynamic power consumption and the leakage current, which consequently reduces the leakage power consumption (Butzen and Ribas 2007) (Gonzalez, Gordon, and Horowitz 1997). This method is considered effective in reducing the power consumption of the CMOS circuits due to the quadratic dependence of the switching power concerning the supply voltage, see the previous Equation 1. Besides the supply voltage scaling providing leakage power saving, it exponentially

reduces the leakage current that results from the DIBL effect due to the technology down-scaling (Roy, Mukhopadhyay, and Mahmoodi-Meimand 2003).

#### 2.3.1.3 Transistor Stacking

The leakage current flowing through a stack of series-connected transistors is reduced when more than one transistor in the stack is turned off (Butzen and Ribas 2007). This effect is known as the "stacking effect" or "self-reverse bias". As shown in Figure 19 (b), the leakage of a two-transistor stack in order of magnitude is less than the leakage in a single transistor. However, when more than two stacking transistors are used, the leakage current tends to be constant, as seen in the illustrated plot. Figure 19 (a) presents a NAND topology with transistor stacking. If the NMOS M1 and M2 are OFF, the voltage at the intermediate node ($V_M$) will be slightly positive due to the small drain current (Nagar and Parmar 2014). This positive source potential created by the transistor stacking will turn the potential between the gate and source negative. The positive potential at $V_M$ has three effects such as (Butzen and Ribas 2007; Nagar and Parmar 2014):

1. The leakage current is substantially reduced due to the intermediate point's negative gate-to-source positive source potential, which is caused by the positive source potential.
2. Since $V_M$ is positive, the body-to-source potential of transistor M1 becomes negative, resulting in a body effect increase of M1, thus reducing the leakage current that flows through this transistor.
3. The DIBL effect is mitigated due to the decrease of the drain to source potential of M1 caused by the positive $V_M$. Consequently, the leakage current is also reduced.

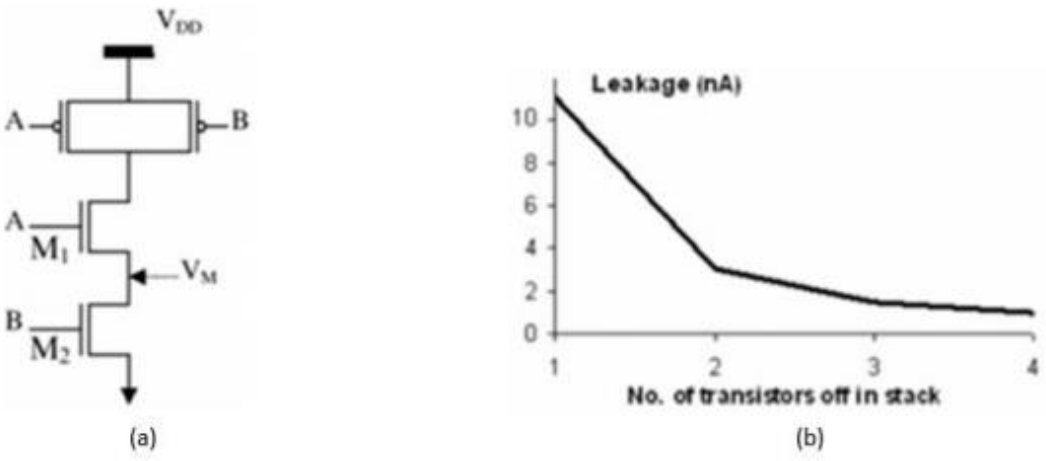


*Figure 19: Transistor Stacking, (a) Stacking effect in two-input NAND gate, (b) Subthreshold leakage current using different number of stacks in OFF state* (Butzen and Ribas 2007).

# 3 Development and Results

## 3.1 Analog Switch

One of the main bottlenecks of the vibrational energy harvesters is the piezoelectric's operational resonant frequency that contrasts with the low frequency of the vibrational environmental sources. An efficient matching circuit is required to increase the transferred energy to the storage unit to maximize the scavenged power. A frequency up-conversion technique is needed to increase the operating frequency to overcome these disadvantages. By increasing the working frequency, a matching circuit can be more efficient, the size of the passive components decreases compared to traditional matching circuits. Also, as the dimension decreases, producing these passive matching components in CMOS technology, its reliability increases and decreases related intrinsic noise.

Even though the single TG improves the switch's characteristics, managing the MOSFETs' threshold voltage inside it is still important. This bulk voltage management is essential because low ON-resistance is needed to avoid power losses when the switch is ON. On the other side, when the switch is OFF, a high OFF resistance is required to isolate the piezoelectric device's output.

Another problem related to the TG is the unwanted reverse current when a capacitor or an inductor is added as a load. When an input sinusoidal signal is applied, the output voltage would be slightly higher than the input voltage in several time intervals, leading to a change of the current direction. Therefore, it is essential to create a technique to block the reverse current. This unwanted reverse current decreases the performance of the circuit and is a potential hazard to the device.

Hence, a new topology was designed to fix these issues, and it is presented in Figure 20. This design also has a TG as the primary switch device. Compared with the single TG, this circuit presents a constant and low ON-resistance and a high OFF-resistance, which leads to an increase in its performance. Besides that, it prevents reverse current from the RC load. Therefore, this circuit is composed of an inverter with a transistor stacking technique to bias the switch, a TG with the switching-bulk technique applied to the

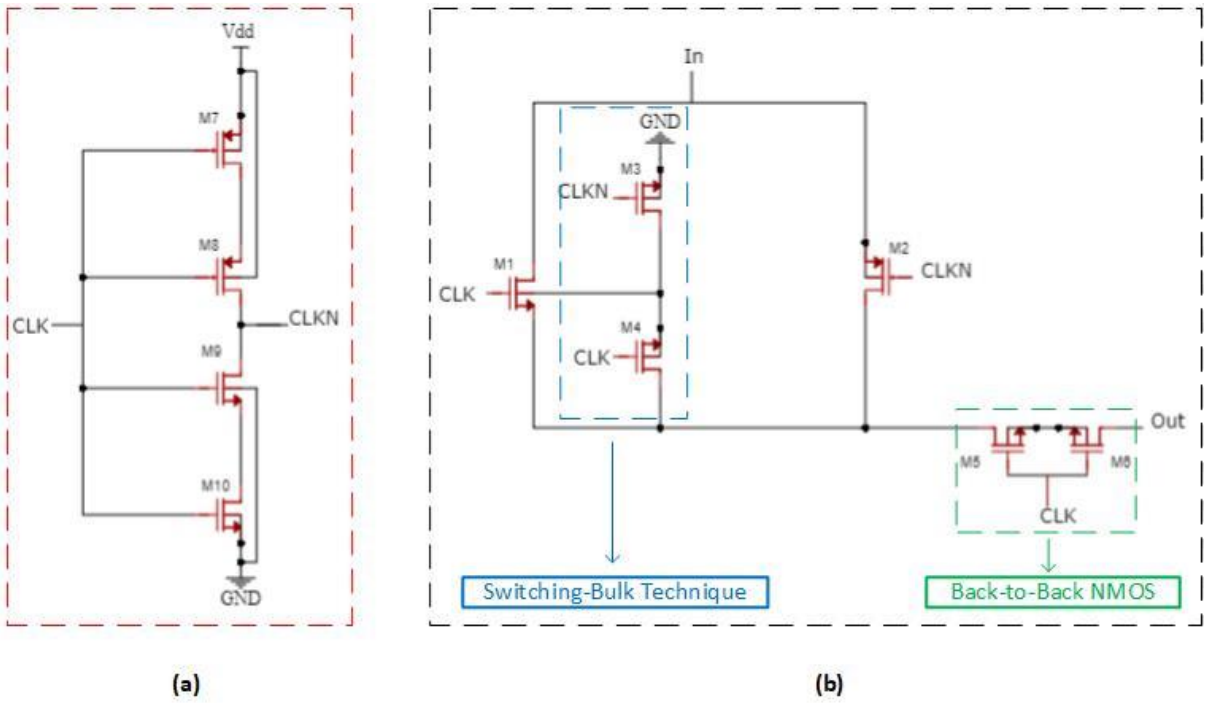


*Figure 20: (a) Inverter stage with Transistor Stacking used to bias the analog switch; (b) Proposed analog switch with the addressed techniques.*

NMOS transistor, and a Back-to-Back NMOS configuration that connects the TG to the RC load. The size of the transistors used in the Analog Switch design is displayed in Table 3. Furthermore, the physical layout of the proposed analog switch is presented in Figure 21.

During the ON phase, the inverter biases the TG NMOS with CLK at high state and PMOS with CLKN at a low state, making the output signal tracking the input signal with high voltage efficiency low switch's ON-resistance. During the OFF phase, CLK is low, and CLKN is high, making the TG turn off, and the output voltage drops to almost 0 V.

The following subsections present the techniques added to the analog switch to improve the linearity, threshold voltage, ON-resistance, OFF-resistance, and avoid the unwanted reverse current.

*Table 3: Transistor size of the Analog Switch.*

| MOSFET | Unit Size (µm/µm) |
|---|---|
| M1/2 | 10/0.13 |
| M3/4/7/8/9/10 | 0.15/0.13 |
| M5/6 | 5/0.13 |

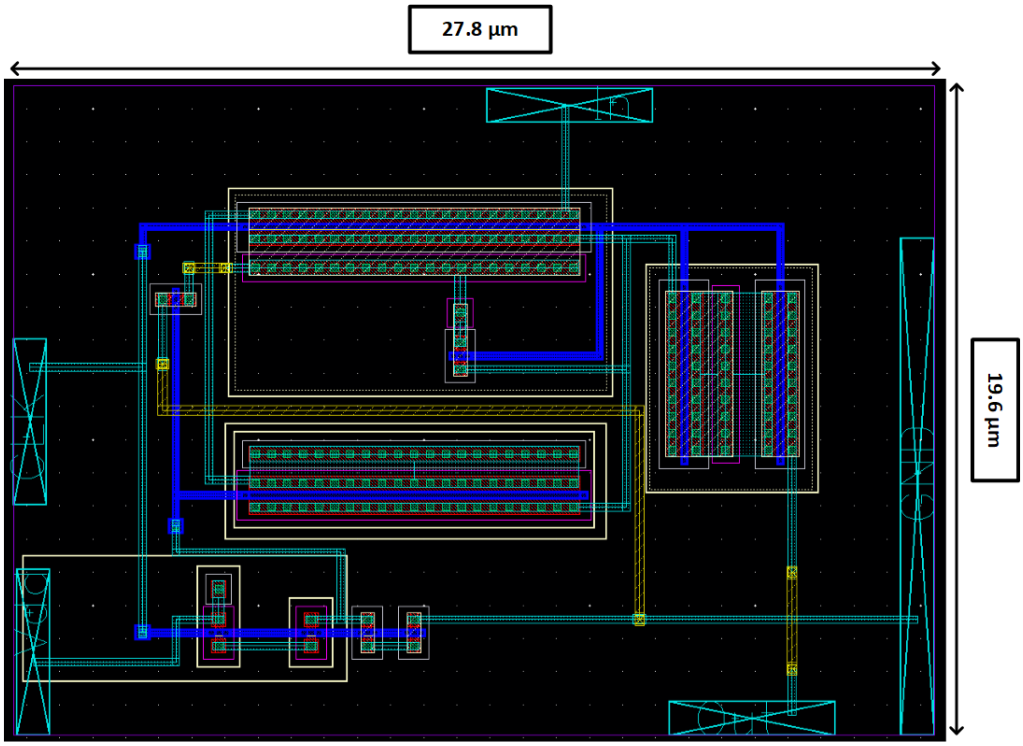


*Figure 21: Physical layout of the proposed analog switch.*

### 3.1.1 The Switching-Bulk Technique

Due to high threshold variations on the TG when the bulk terminal is connected to the power supply for PMOS, and to the ground for NMOS, a switching-bulk NMOS technique was added in order to fix this issue. It consists of two auxiliaries NMOS, M3 and M4, that switch the main NMOS bulk between GND, during the OFF phase, and the source voltage, during the ON phase. For this application, this technique is revealed to be useful because, on the one hand, the TG's resistance becomes lower and constant

during the ON phase due to the threshold voltage reduction. On the other hand, during the OFF phase, the resistance increases due to the threshold voltage's increase, leading to a better switch's conductance and performance.

However, for this application, this technique cannot be added to the PMOS transistor because, due to its bulk voltage being varied between the input voltage and the voltage supply, the bulk voltage would be higher than the input voltage when the switch is at OFF state. Therefore, it would generate a reverse current flowing from the bulk to the input voltage. The bulk terminal was connected to the source for this transistor to keep the threshold voltage almost constant due to body effect cancellation. With this technique, the difference between PMOS and NMOS threshold voltage was reduced, which improves the unavoidable charge injection error.

To prove the efficiency of the switching bulk technique, Figure 22 shows the ON-resistance and OFF-resistance behavior with the input voltage variation with and without this technique. As shown in the presented figure, the ON-resistance is low and constant for the two cases since the bulk terminal of M1 is connected to the drain by M4. At an input voltage amplitude of 500 mV, the ON-resistance is 216 Ω, which is revealed to be low. However, when the analog switch is not working, the OFF-resistance is higher when this technique is used because M3 connects the bulk terminal of M1 to 0 V. Since the bulk voltage is different from the drain one, the OFF-resistance is increased due to the body effect in M1, which is good for isolating the load from the input. Therefore, it can be concluded that the mentioned overall features of the analog switch are improved by using the switching bulk-technique.

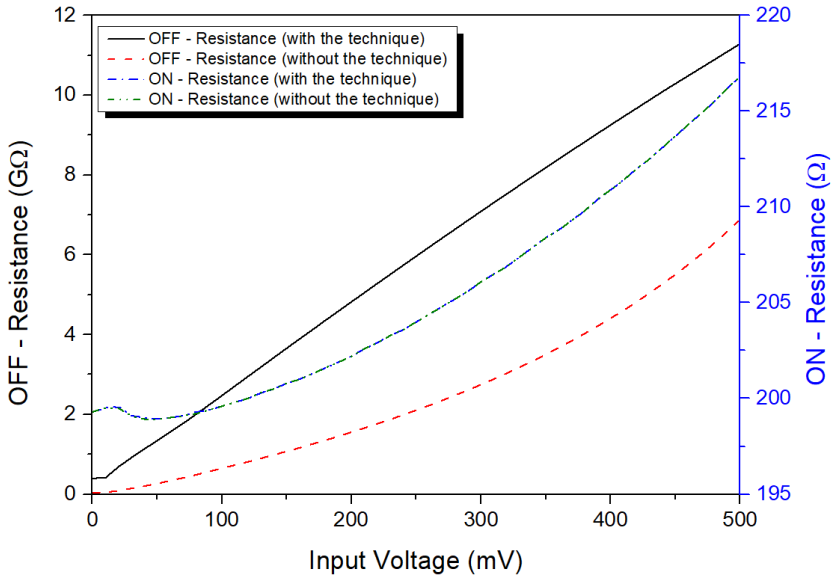


*Figure 22: ON-resistance and OFF-resistance behaviour with and without the switching bulk technique for different input voltage.*

### 3.1.2 Back-to-Back NMOS

As explained before, one of the problems of the analog switch is the reverse leakage current associated with the load when the output voltage is slightly higher than the input voltage. Thus, since the NMOS impedance between drain and source is lower than in PMOS, a back-to-back NMOS configuration was added after the TG, consisting of two NMOS transistors, M5 and M6, with both source terminals connected. This configuration is useful because it eliminates all the blocking diodes and replaces them with a pair of NMOS with their internal body diodes pointing away from each other to block the unwanted reverse current flow. Besides that, this technique decreases the circuit's current consumption due to leakage current reduction, which enhances this circuit's power efficiency. Even though this technique reduces voltage efficiency, the voltage drop across the two NMOS is low, so it is not significant.

Since the OFF-state leakage current is an important parameter that influences static power consumption (Jayakumar et al. 2010), this current was measured with the input voltage variation with the back-to-back technique and without it. In Figure 23, it is proved that the back-to-back NMOS avoids reverse current and mitigates the OFF-state leakage current due to the high impedance path generated by the two NMOS transistors. Also, this OFF-state leakage current is lower than the prior state of the art on analog switches, as shown in section 3.1.4.

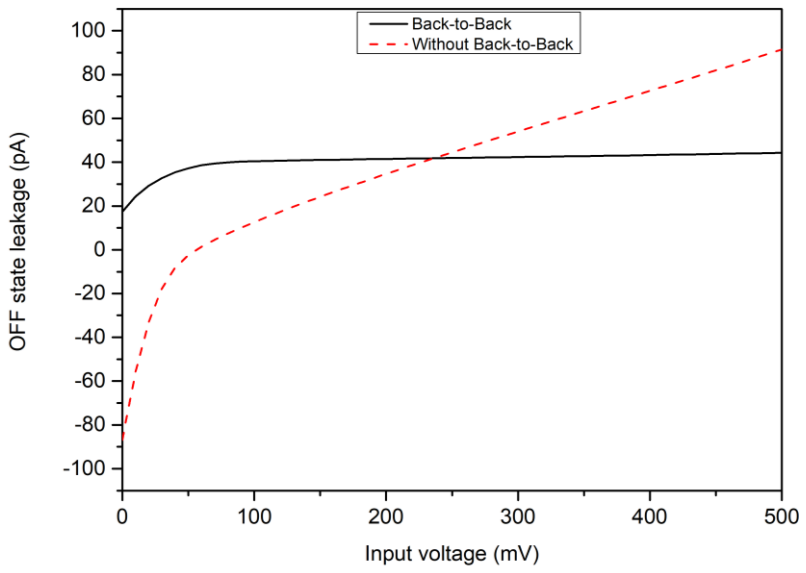


*Figure 23: OFF-state leakage current with and without the back-to-back NMOS technique.*

### 3.1.3 Transistor Stacking on the Inverter stage

Finally, Figure 20 (a) presents the inverter stage with transistor stacking. It is essential to add this stage to bias the MOSFETs inside the TG. Therefore, it is imperative to manage the leakage current and the power dissipation at this stage. A transistor stacking was added to this stage by connecting M7 and M10 to decrease these features. These two transistors present a high threshold voltage caused by the body effect. Consequently, the overall static power consumption is reduced due to the decrease of both static current and OFF-state leakage current.

Table 4 shows the current that the power source needs to bias to the inverter during the ON and OFF state with and without the transistor stacking. As expected, this technique mitigates the current consumption of the inverter, which consequently reduces its static power consumption.

*Table 4: Current and static power consumption comparison.*

| Features | With Transistor Stacking | Without Transistor Stacking |
|---|---|---|
| $I_{ON}$ (µA) | 17.40 | 36.10 |
| $I_{OFF}$ (nA) | 71.41 | 133.33 |
| $P_{Static}$ (nW) for $V_{DD} = 2\ V$ | 142.80 | 266.66 |

### 3.1.4 Results

The proposed analog switch was simulated in the Cadence Virtuoso Analog Design Environment using 130 nm CMOS technology. The input voltage is a sine wave with 500 mVp-p amplitude, and the power supply voltage is a DC source with 2 V. The input frequency was set in 32 Hz, which simulates the harvester output frequency. Since an external oscillator circuit generates the clock signal, a square wave source was used to simulate its behavior. The amplitude signal was varied from 0 V to 2 V with a frequency of 3.2 kHz and a duty cycle of 20 %. A load resistor and capacitor were added with 10 kΩ and 1 pF, respectively, in the output to study the circuit's performance.

Figure 24 shows the sampled output voltage and the input voltage signal for the proposed analog switch. As observed, when the CLK signal reaches the high value, the analog switch is ON, which allows the current to flow, and the output voltage almost reaches the input one. In the opposite state, the analog switch isolates the input terminal from the output, which drops the output signal to 0 V. As expected, the output frequency increases from 32 Hz to 3.2 kHz. Furthermore, it is possible to notice that, when the input is at 500 mV of amplitude, the voltage drop of the analog switch is higher due to the increase of the ON-resistance and current, as presented in Figure 25. According to Equation 4, the rise of the ON-resistance is caused by the increase of the source terminal, which reduces $V_{GS}$.

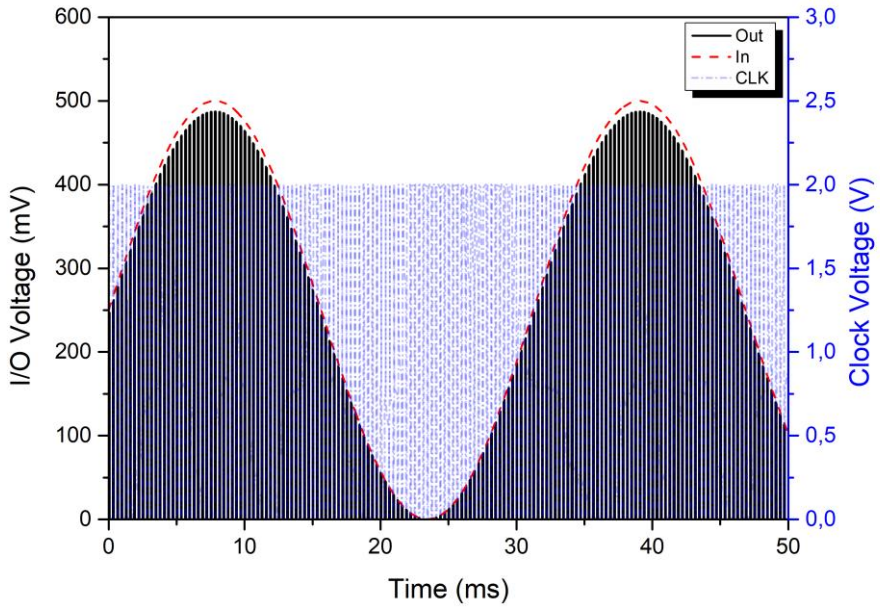


*Figure 24: Simulation of the proposed analog switch working principle, including the input voltage (In), clock signal (CLK), and the output voltage (Out).*

In addition, Figure 25 shows the ON-resistance behaviour for different temperature values. It can be observed that the ON-resistance increases for higher temperatures since the threshold voltage is directly proportional to the temperature. Nonetheless, the ON-resistance is still low for higher temperatures, which proves the analog switch's robustness to temperature variations.

The switching speed was measured using the Cadence calculator tool to complete the previous tests, see Figure 26. In this figure, it is possible to observe the clock voltage used to bias the inverter stage (CLK) and the output voltage ($V_{out}$) and the respective measured switching speed. The switch's turn-on time ($t_{ON}$) is the time required to activate the circuit from the OFF to the ON state, and vice-versa for the switch's turn off time ($t_{OFF}$). As observed in the following figure, the analog switch takes 385.7 ns to

make the output reach the input waveform. Moreover, the circuit takes 332.4 ns to make the output reach 0 V.

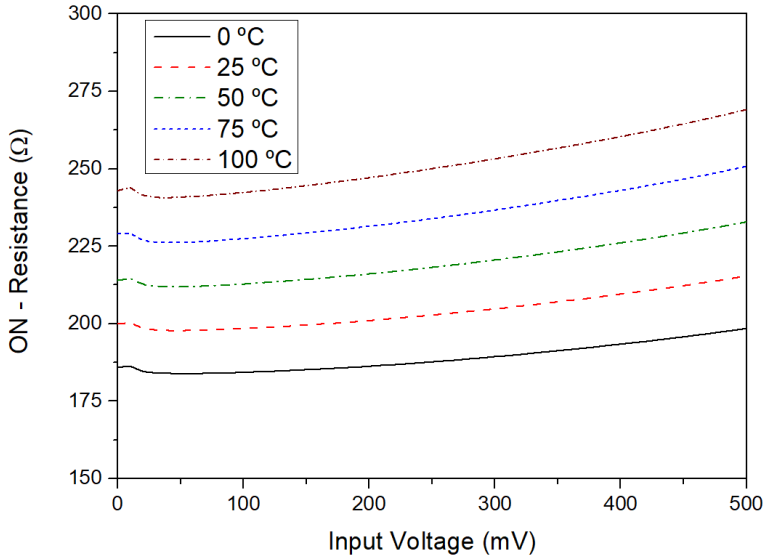


*Figure 26: ON-resistance behaviour with input voltage variation for different temperatures.*

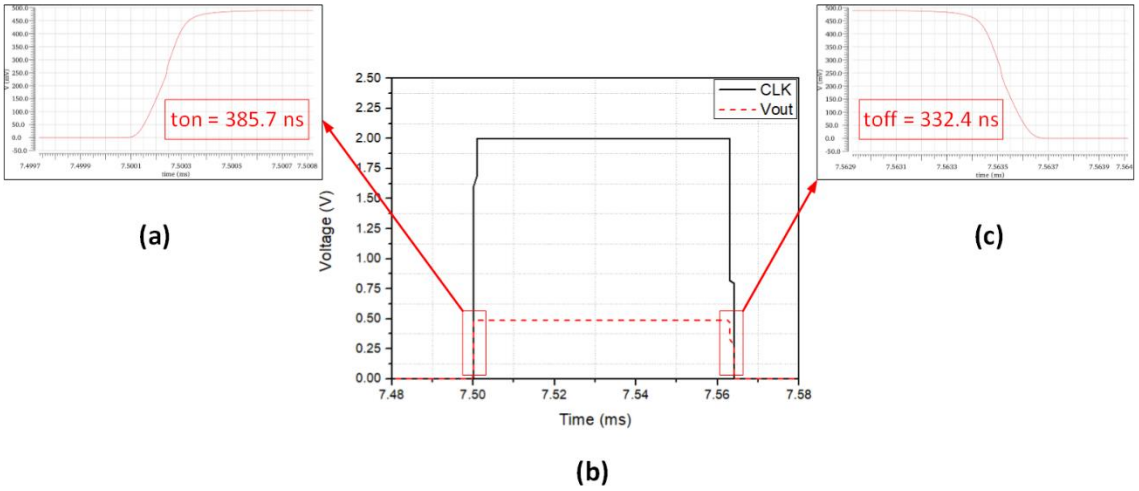


*Figure 25: Switching speed test: (a) Rise time of $V_{out}$ ; (b) $V_{out}$ and CLK behaviour; (c) Fall time of $V_{out}$.*

Moreover, to provide a more accurate evolution of the proposed switch behaviour during the ON and OFF state, the switch's ON-loss and OFF-isolation were measured with the input voltage variation using Equation 11 and 12, respectively. As presented in Figure 27, the ON loss is approximately -0.21 dB, which means a voltage efficiency of 97.4 %. The OFF-isolation ratio of the switch is around -120 dB, which provides excellent isolation between the input and output signals.

$$ON_{LOSS} = 20 \cdot \log\left(\frac{V_{out}}{V_{in}}\right) \qquad 11$$

$$OFF_{Isolation} = 20 \cdot \log\left(\frac{V_{out}}{V_{in}}\right) \quad 12$$

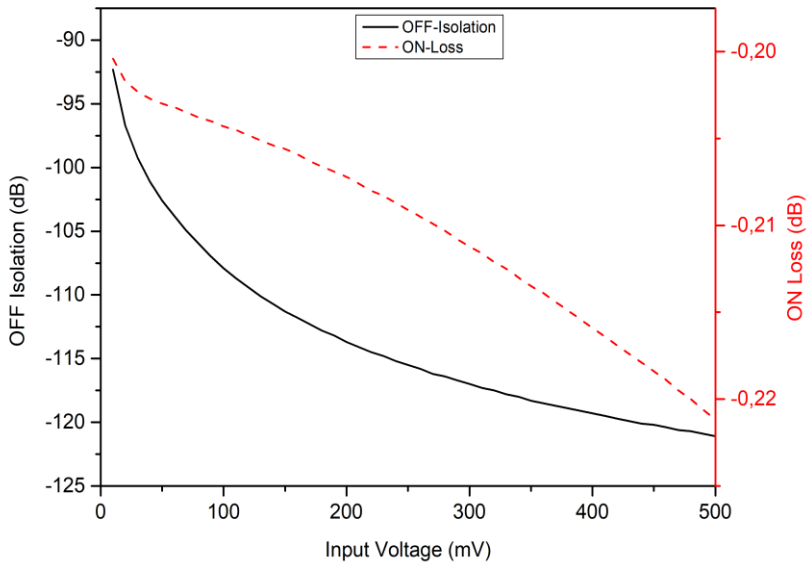


*Figure 27: ON-loss and OFF-isolation behaviour with input variation.*

Table 5 summarizes the performance of the proposed switch and compares it to the previous works. It can be observed that this configuration presents a very low OFF-state leakage current and low power consumption when compared to the others.

*Table 5: Analog Switches performance summary and comparison.*

| | This Work | (Chiranu et al. 2019) | (Naghavi, Sharifi, and Abrishamifar 2018) | (Zhou and Li 2012) |
|---|---|---|---|---|
| Tech. (nm) | 130 | 180 | 180 | 130 |
| $V_{dd}$ (V) | 2 | 2.05 | 0.8 | 0.16 |
| $V_{in}$ (V) | 0.5 | 5 | 0.8 | 0.16 |
| $R_{ON}$ (Ω) | 244.6 | 100 | 270 | - |
| $R_{OFF}$(GΩ) | 5.9 | - | 23.5 | - |
| OFF-Isolation (dB) | -120 | -95 | -160 | -140 |
| ON-Loss (dB) | -0.21 | - | - | - |
| $I_{OFF}$ (nA) | 0.044 | 11 | - | - |
| Power Consumption (nW) | 200.8 | - | - | 670 |

## 3.2 CMOS Rectifier

Regarding the inherent output characteristics of the piezoelectric transducer, the proposed CMOS rectifier was mainly designed to achieve a high PCE for wide low input voltage and frequency conditions. Therefore, the operational voltage ranges from 0.4 V to 1 V, and the operational frequencies from hundreds of Hz to a few kHz. In addition, the output impedance of the energy harvester is not considered in this design because the matching impedance process is performed before this rectification stage in the PMC. Since it is required to avoid the use of external power sources, the rectifier must be capable of using efficiently the input voltage to bias all transistors. Thus, the main goal of this work is to reduce the voltage drop across the structure by applying a threshold cancellation technique that will further enhance the power converted to the ohmic load. These improvements will overcome the drawbacks of the previous works by mitigating the reverse leakage current, and thus enhancing the PCE for a low input voltage range.

Figure 28 and Figure 29 show the simplified schematic of the proposed configuration and the physical layout, respectively. It consists of an NVC and an active diode biased by a threshold cancellation circuit to make it work as an ideal diode. The first stage is set to perform the signal full-wave rectification, by converting the negative input signals into positive. However, because this passive stage cannot control the reverse current that comes from the load capacitor when the output voltage is higher than the input,

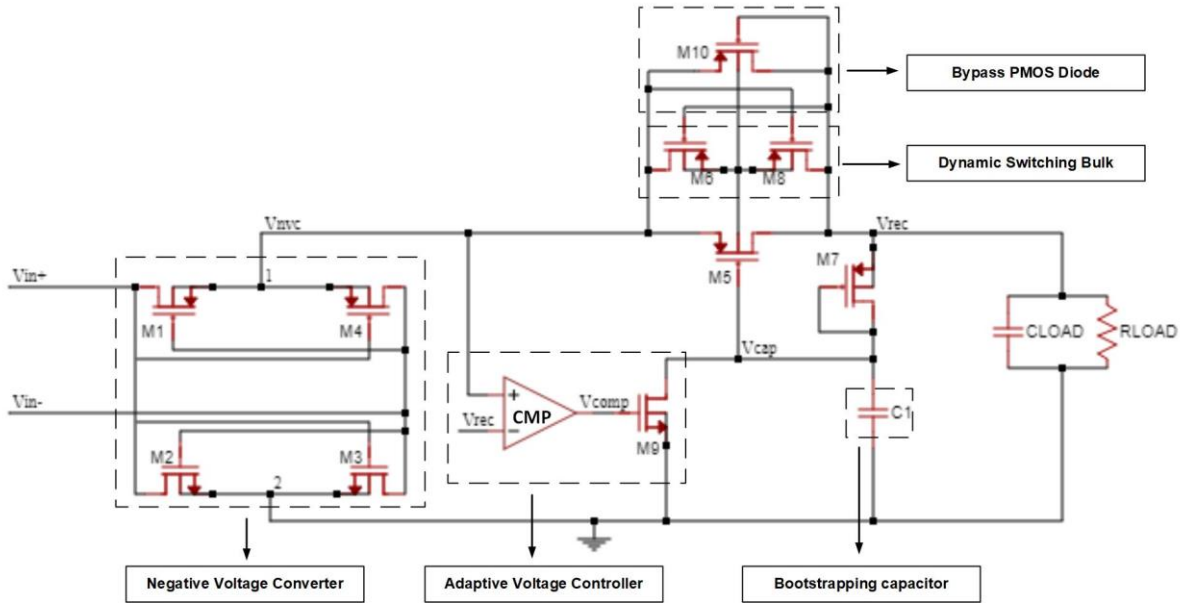


*Figure 28: Schematic of the proposed active rectifier composed by an NVC and an Active diode controlled by a Threshold Cancellation Circuit.*

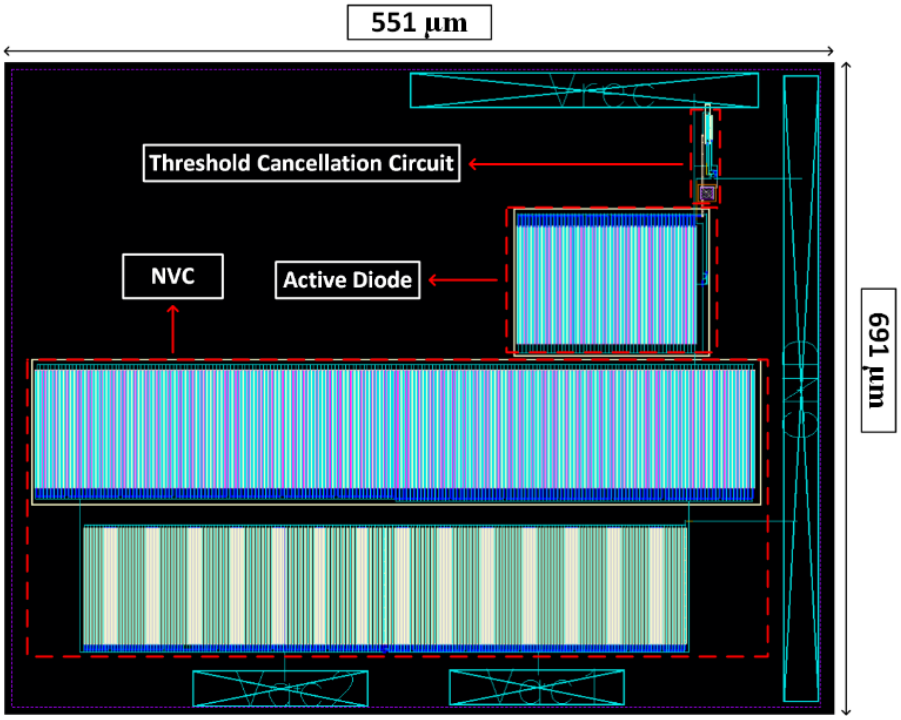


*Figure 29: Physical layout of the proposed CMOS rectifier.*

a second stage active diode (M5) is needed. This active stage is composed of a PMOS controlled by a threshold cancellation circuit with a bootstrapping capacitor to reduce the effective threshold of the active diode, and an AVC to adjust the gate voltage of M5 by controlling the charging/discharging cycle of the bootstrapping capacitor. To perform it, a two- input common gate comparator and an NMOS are used. Besides these stages, a DSB technique and a bypass transistor (M10) were used to control the bulk voltage of the active diode PMOS and ensure a safe start-up of these transistors, respectively.

### 3.2.1 Negative Voltage Converter

The first stage is entirely passive, and it is used to perform the signal full-wave rectification by applying a fully cross-coupled configuration. During the positive half period of the input signal ($V_{in+} > V_{in-}$), M1 and M3 will be conductive as soon as the input voltage gets larger than $V_{thn}$ and $|V_{thp}|$. In this cycle, node 1 is connected to $V_{in+}$ and node 2 to $V_{in-}$. For the negative period of the sine wave, M2 and M4 are conducting while the previous two transistors are now turned off (cut-off region). Therefore, the higher voltage potential is always at node 1, whereas the lowest potential is at node 2. The voltage drop of the NVC is given by $V_{dsn} + V_{sdp}$ in each conduction path, where $V_{dsn}$ and $V_{sdp}$ are the voltage drop of NMOS transistors M2 and M3 and PMOS transistors M1 and M4, respectively.

To meet all the power restrictions related to the piezoelectric energy harvesting systems, the rectifier circuit must minimize the voltage drop across the rectification process. As less voltage drop occurs, higher it will be the figure of merit metrics related to this circuit (PCE and VCE). For this stage, NVC, the main requirement is to decrease the voltage drop associated to each MOSFET by reducing their ON-resistance.

### 3.2.2 Active Diode

One of the main challenges on the rectifier circuit is to control the direction of the current and avoid the reverse leakage current. Therefore, an active diode controlled with a threshold cancellation circuit, can regulate the work behaviour of this device depending on the voltage potential between the input and output. The deployed threshold cancellation circuit controls the gate potential of the MOSFET M5 by comparing the input/output voltage conditions. Additionally, the width of M5 has a large influence on the performance of this rectifier because the voltage drop is mainly affected by the internal ON-resistance. Thus, the influence of the width of the NVC stage (M1-M4) and of M5 in both PCE and VCE can be observed in Figure 30. For this test, the width of both stages was individually varied, while the other was kept constant. This figure shows that the VCE and PCE features of both stages are at their maximum point for a width of 100 µm since the ON-resistance of this transistor is directly influenced by the size of the transistor.

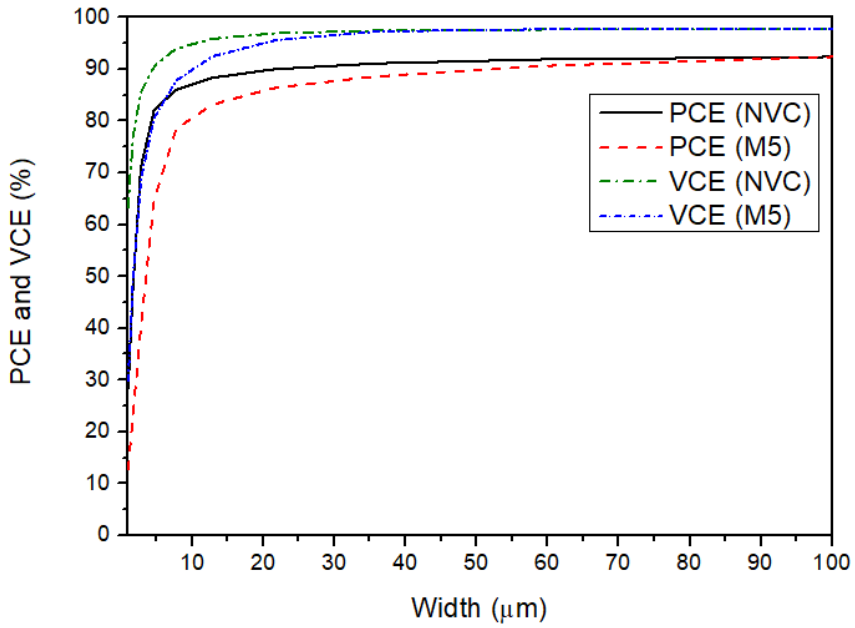


*Figure 30: PCE and VCE plot with the variation of the width of the NVC transistors and M5 (L = 130 nm).*

Besides, it was implemented a DSB technique, composed of M6 and M8, to reduce the leakage current through the bulk terminal of M5 by connecting it to the higher potential ($V_{nvc}$ or $V_{rec}$). Another advantage of this technique is eliminating the body effect of M5, which reduces the rectifier voltage drop. Both M6 and M8 can have a small size since only a very low current flows through them during the start-up phase.

To assure a safe start-up of M5, a bypass PMOS diode (M10) was connected in parallel. Even if the area increases, it makes the active diode more robust by preventing it from leakage current in the subtract that induces latch-up. After the start-up phase, the bypass diode always operates in the cut-off region.

### 3.2.3 Threshold Cancellation Circuit

In order to reduce the threshold voltage effect on M5, it is used a bootstrap technique using the capacitor $C_1$. When the $V_{NVC}$ is higher that the output voltage $V_{rec}$, M5 is turned ON, since $V_{SG5}$ is no longer lower than $V_{TH5}$, and thus it can be defined by Equation 13. Nevertheless, since M5 is operating in deep-triode region due to $V_{SD5}$ being much lower than $V_{SG5} - |V_{TH5}|$, $V_{SG5}$ can also be defined according to the ON-resistance equation, see Equation 14.

$$V_{SG5} = V_{NVC} - V_{CAP} \tag{13}$$

$$V_{SG5} = \frac{1}{\mu_p \cdot C_{ox} \cdot \frac{W_5}{L_5} \cdot R_{SD5}} + |V_{TH5}| \tag{14}$$

Here, $\mu_p$ is the carrier mobility, $C_{ox}$ is the oxide capacitance, $\frac{W_5}{L_5}$ is the aspect ratio of transistor M5, and $V_{TH5}$ is its respective threshold voltage.

The bootstrapping capacitor ($C_1$) is charged up through an auxiliary diode-connected PMOS transistor M7, and it maintains a value when the rectifier is under the steady-state regime. At this time, since $C_1$ is discharging, $V_{CAP}$ is one diode forward-bias voltage ($V_{TH7}$) bellow $V_{rec}$ due to M7 is being in the saturation region. Thus, the voltage held on the bootstrapping capacitor can be defined as:

$$V_{CAP} = V_{rec} - |V_{TH7}| \tag{15}$$

$V_{SG5}$ and $V_{CAP}$ from (13) and (15), respectively, can be replaced in (14), which means that $V_{rec}$ can now be defined according to the following two equations:

$$\frac{1}{\mu_p \cdot C_{ox} \cdot \frac{W_5}{L_5} \cdot R_{SD5}} + |V_{TH5}| = V_{NVC} - (V_{rec} - |V_{TH7}|) \quad 16$$

$$V_{rec} = V_{NVC} - (|V_{TH5}| - |V_{TH7}|) - \frac{1}{\mu_p \cdot C_{ox} \cdot \frac{W_5}{L_5} \cdot R_{SD5}} \quad 17$$

According to Equation 17, the rectified signal is highly influenced by the size of M5 and the threshold voltage of both M5 and M7, and thus it is vital to manage these parameters to enhance the output signal voltage. The implemented threshold cancellation circuit reduces the voltage drop of the main pass transistor M5 by reducing the threshold voltage effect. Also, the size of the bootstrap capacitor is an important design concern for the implementation of the proposed rectifier. Integrated capacitors consume a considerable area on the chip when standard CMOS processes are used (Khan and Choi 2017). Therefore, $C_1$ was set at 200 fF not only to reduce the correspondent area on die, but also to have a faster charging/discharging time. Consequently, this low bootstrap capacitance allows a lower gate voltage of M5 at the ON state. Due to the reduction of its internal source to drain resistance, the voltage drop is decreased. The reverse leakage current during the OFF will be avoided since $V_{SG5}$ is reduced. Moreover, it is highly demanded an auxiliar circuit to hold $V_{CAP}$ node when M5 is OFF, and to discharge it at the opposite state.

The bootstrapping capacitor is used to reduce the threshold voltage effect of M5. However, an increase of its ON-resistance can be noticed due to the reduction of $V_{SG5}$. Thus, a conduction path needs to be generated to discharge the gate of M5 during the ON state, which will lead to a further increase of $V_{SG5}$. The proposed AVC is composed of NMOS M9 and a comparator CMP that drives its gate. When $V_{NVC}$ is higher than the output voltage $V_{rec}$, comparator CMP should immediately turn on M9 in order to provide a discharge path of the $V_{CAP}$ node. Consequently, it will turn on the main pass transistor M5 with a low ON-resistance. Since the large size of M5 increases the gate capacitance, the AVC must have a faster bias signal control to switch the discharge path of the gate node ($V_{CAP}$). Thus, the comparator must be designed to attend these demands.

Figure 31 shows the proposed two-input common gate comparator. This comparator is composed of a current mirror stage to make the comparison, plus an inverter block to bias the gate of M9. Even if the transistor of the current mirror should be as small as possible to reduce the current consumption of the comparator, the size of M12 and M15 must be carefully chosen to manage the delay, and consequently the reverse leakage current in M5. These two transistors cannot have the same W/L ratio as M11 and M14. Otherwise, it would generate a delay caused by the inverter's gate capacitance's low charging/discharging time. Additionally, they cannot be much larger than the other transistors because of the reduced time that M5 would be ON, which would lead to a PCE reduction. Therefore, M12 and M15 only need to be slightly higher to provide the required charging/discharging time to reduce the delay of the overall comparator. Table 6 summarizes the dimension values of the proposed rectifier circuit.

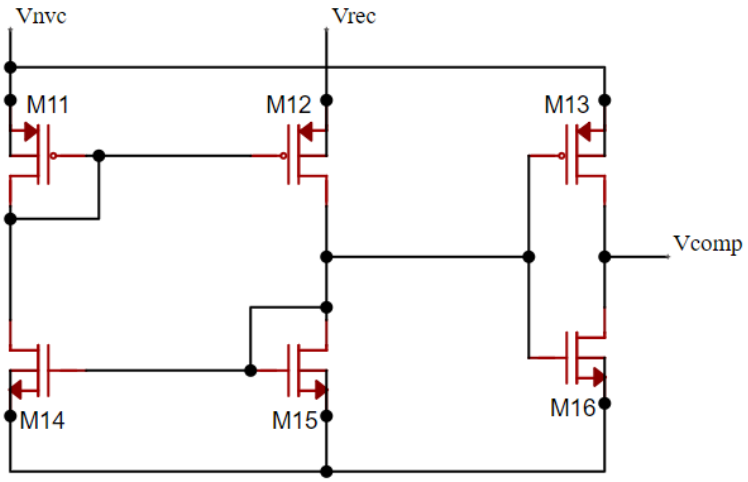


*Figure 31: Schematic of the two-input common gate comparator CMP.*

*Table 6: Circuit transistor sizes.*

| MOSFET | Unit Size (µm/µm) | Multiply Factor |
|---|---|---|
| M1/2/3/4 | 100/0.13 | 100 |
| M5 | 100/0.13 | 50 |
| M6/8/10/11/13/14/16 | 0.28/0.13 | 1 |
| M7/9 | 20/0.13 | 1 |
| M12/15 | 0.34/0.13 | 1 |

### 3.2.4 Results

In this section it will be presented and discussed the simulation results of the proposed CMOS rectifier. The simulations were carried out using Cadence Virtuoso Analog Design Environment with 130 nm CMOS process. To replicate the output behaviour of the energy harvester, the default input sinusoidal voltage amplitude and frequency used in the simulations were 600 mV and 3.2 kHz, respectively. Throughout most of the simulations, $C_{LOAD}$ and $R_{LOAD}$ were set by default with 2 µF and 5.5 kΩ to simulate the capacitance of the storing capacitor and the impedance of the electronics to be powered.

#### 3.2.4.1 Transient Behaviour

The transient performance of the output voltage, in both stages, is displayed in Figure 32. The first stage does the full-wave rectification by converting the negative input voltage ($V_{IN}$) into positive ones ($V_{NVC}$). The voltage drop on this stage is around 1 mV, while the total voltage drop on the rectifier is around 12 mV, which it was possible to accomplish due to the reduction of the internal resistance of the main pass transistor M5. The achieved voltage drop was crucial to enhance the output voltage across the load.

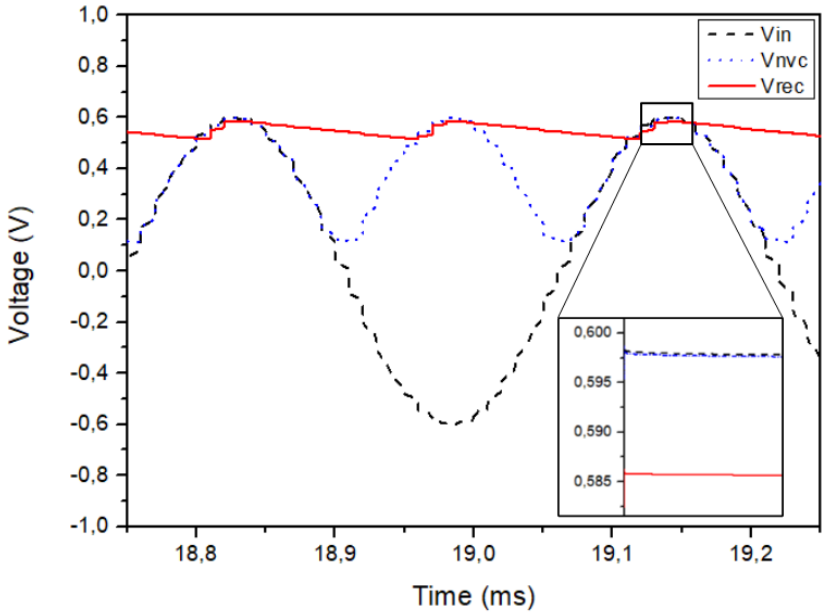


*Figure 33: Simulated waveforms of the rectifier for $R_{LOAD} = 5.5\ k\Omega$ and $C_{LOAD} = 2\ \mu F$.*

Figure 33 shows the VCE behaviour versus the input voltage amplitude, for different $R_{LOAD}$ values. VCE is defined by the comparison between the input voltage and the output rectified voltage. It is possible to observe that the proposed rectifier can work for an input voltage range from 0.45 V to 1 V for different ohmic loads, with a VCE varying between 96% and 99%. For an input voltage lower than 0.4 V, the VCE sharply decreases because the NVC transistors will enter in subthreshold region or even cut-off. Moreover, it can be noticed that the rectifier VCE is higher for larger load resistors, as it would be expected.

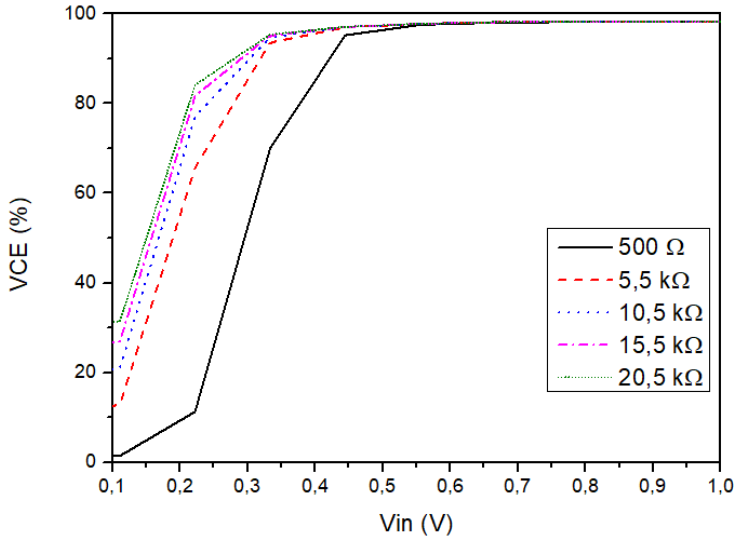


*Figure 32: VCE versus input voltage amplitude simulated for different ohmic loads.*

### 3.2.4.2 Reverse Leakage Current Analysis

The reverse leakage current analysis is one of the most important analyses to make in CMOS rectifiers, since it affects the power efficiency of the overall system. Thus, the reverse leakage current was first

analysed in the NVC stage in two cases: the first was consisted in attaching this stage directly to the RC load; and the second one involved connecting the NVC to the active stage. As shown in Figure 34, the reverse leakage current spikes are clear to be noticed when the active diode is attached to this subcircuit. Therefore, it is possible to conclude that the active stage is essential to block this unwanted current when the output voltage is higher than the input.

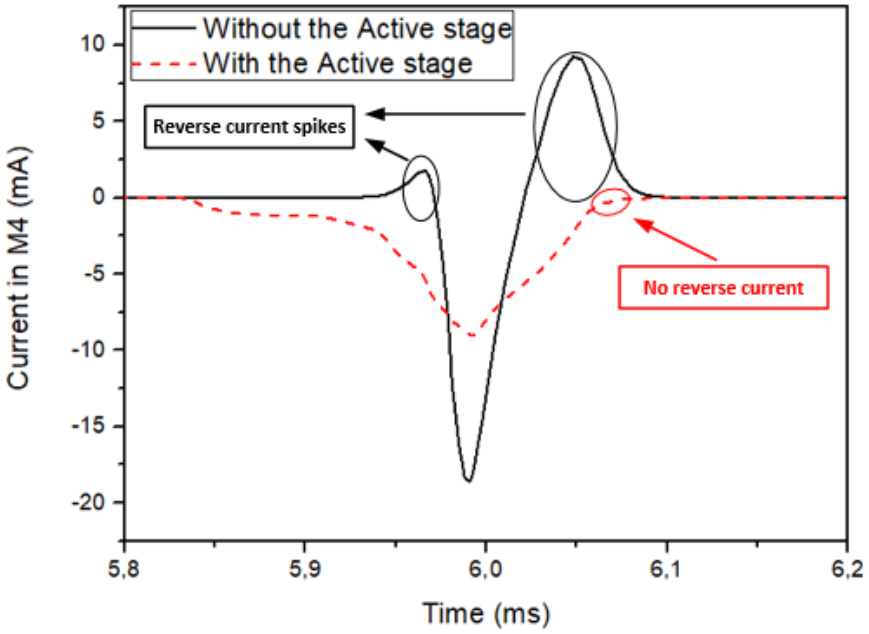


*Figure 34:. Reverse leakage current analysis in the NVC stage*

This unwanted current is also dependent on the delay of the comparator and, consequently, of the discharging path of the active diode provided by the AVC. Thus, the analysis of the transient performance of the comparator is shown in Figure 35. It presents the output voltage of the comparator ($V_{CMP}$), the input and output voltage of the active diode used to perform the comparison, the gate voltage of M5 ($V_{CAP}$), and the current that flows through the active diode ($I_{M5}$). As can be seen, the comparator immediately turns on the gate of the AVC transistor to create the discharge path when $V_{NVC}$ exceeds $V_{rec}$. At this stage, the current is flowing through M5, and $V_{CAP}$ is low, which leads to a low voltage drop since $V_{SG}$ is high. When $V_{NVC}$ drops below $V_{rec}$, the comparator then quickly turns off the AVC, and consequently, the active diode. Thus, the proposed structure does not exhibit reverse leakage current that would degrade the PCE of the proposed rectifier.

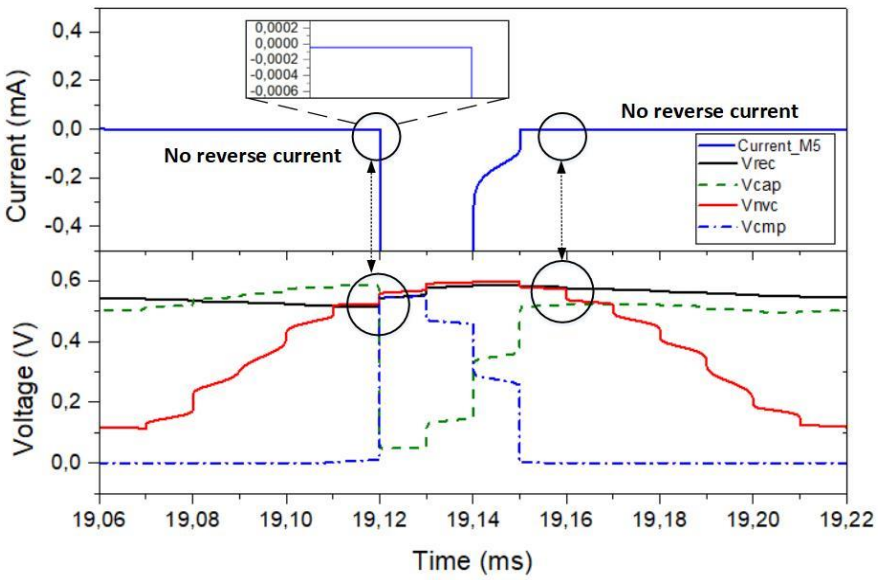


*Figure 35: Simulated comparator behaviour in steady state for $R_{LOAD} = 5.5\ k\Omega$ and $C_{LOAD} = 2\ \mu F$.*

### 3.2.4.3 Power Efficiency

The simulated power efficiency versus input voltage amplitude for different load resistors is presented in Figure 36. The maximum PCE value can be found at 0.6 V with 94% for an $\mathrm{R_{LOAD}}$ of 500 Ω. On the one hand, when $V_{in}$ is lower than this range, the PCE sharply decreases due to the low voltage efficiency as it was previously mentioned in subsection 3.2.4.1. Thus, the efficiency of the rectifier is poor in the ultra-low voltage range. Additionally, the PCE tends to decrease for higher input voltages because the power losses are mainly concentrated in the comparator. With these input voltage conditions, the inverter stage comparator tends to consume more power in the transitory state, which affects the PCE of the

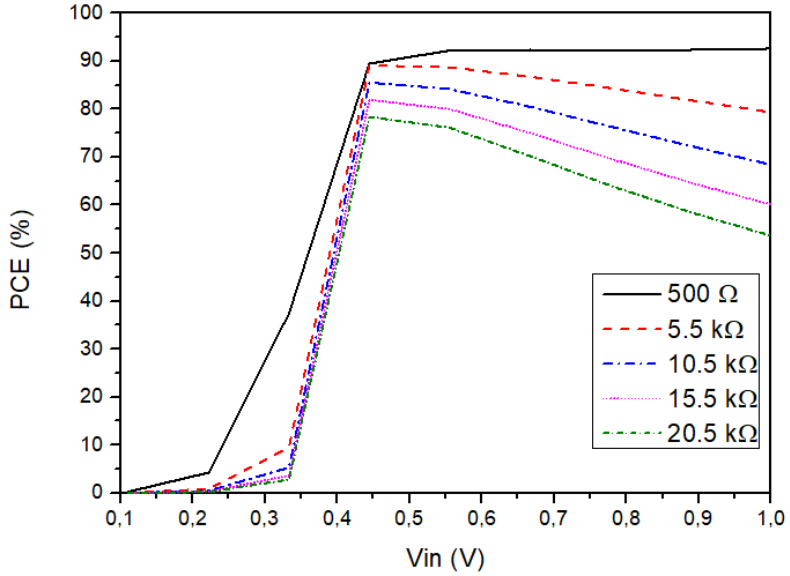


*Figure 36: PCE versus input voltage amplitude simulated for different $\mathrm{R_{LOAD}}$ values.*

rectifier. However, this case is not significant for ohmic loads lower than 15.5 kΩ. Moreover, for higher load resistors, the PCE tends to decrease due to the reduction of the output current, whereas the bias current that comes from the voltage source keeps almost constant. Even if the gate capacitance of M5 increases with the size, Figure 35 shows that the threshold cancellation circuit is capable of driving this large transistor.

Since most energy harvesters reveal to have a low output frequency caused by environmental sources, the proposed rectifier must achieve a high-power efficiency for a low-frequency range. Thus, Figure 37 shows the power efficiency versus input voltage amplitude for different input frequencies. The load capacitor was adapted to keep the output ripple voltage small depending on the input frequency. It is possible to observe that the proposed rectifier can achieve a high-power efficiency for low input frequencies in the operating voltage range. However, when the input voltage and frequency are high, the power efficiency tends to slightly decrease due to the power losses in the NVC and in the active diode, which in this case is caused by the output signal of the comparator being too fast. Consequently, the working time of transistor M5 will be too short, which reduces the amount of power converted to the load. Nonetheless, at typical energy harvesting frequencies, the performance of the CMOS rectifier for the presented frequency range is suitable for this application.

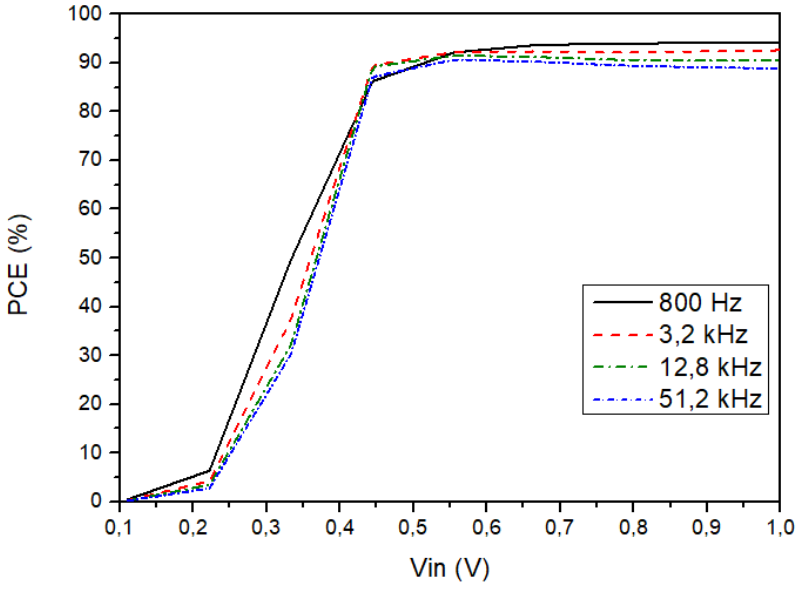


*Figure 37: PCE versus input voltage amplitude for different input frequencies.*

To prove the robustness of the proposed CMOS rectifier, it has been tested through the four known process corners, such as the typical ones, fast, slow, slow NMOS and fast PMOS, and fast NMOS and slow PMOS. Figure 38 presents the PCE plots with temperature variation depending on the process

corner. According to the simulation results, it can be observed that PCE tends to decrease when a fast PMOS is used due to the high speed of the active diode, which decreases the ON time of the rectifier and consequently affects the power transferred to the load.

Regardless, the worst case for PCE is found at 79% for 100 °C, which proves that it achieves an acceptable performance not only for this energy harvesting application but also compared to the prior works on CMOS rectifiers.

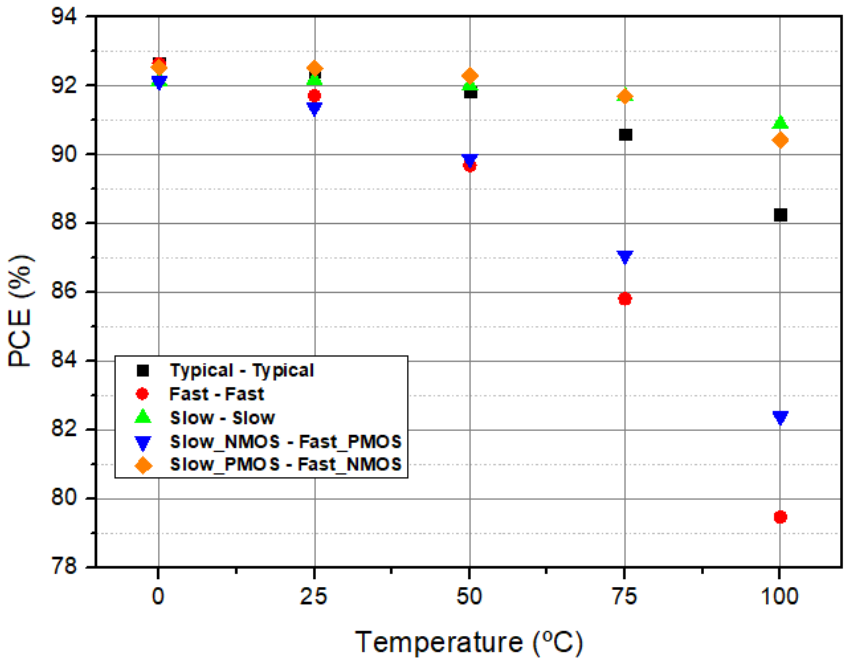


*Figure 38: PCE variation with temperature depending on the process corner variation for $R_{LOAD} = 500\ \Omega$.*

The performance comparison between this work and the previous rectifiers is presented in Table 7. It shows that the proposed configuration can achieve higher VCE and PCE for a low voltage range. Even if the PCE in Ud Din et al. (2019) is higher for a higher ohmic load, for this application, it is only expected a low impedance of the electronics to be powered. Thus, the achieved VCE and PCE in this work are higher than those in the reported literature, highlighting its added value (Peters et al. 2011; Vithya Lakshmi et al. 2021; Yuen, Chong, and Ramiah 2019). Therefore, it can be concluded that this rectifier can overcome the drawbacks of the previous works, mentioned in section 2.2, which means that this rectifier is very suitable for energy harvesting applications.

*Table 7: Research Comparison on CMOS Rectifiers.*

| Ref. | Tech (nm) | $f_{in}$ (kHz) | $V_{in}$ (V) | $R_{LOAD}$ (kΩ) | $C_{LOAD}$ (µF) | VCE (%) | PCE (%) |
|---|---|---|---|---|---|---|---|
| (Peters et al. 2011) | 180 | 0.1 | 0.5 | 50 | 10 | 99 | 84 |
| (Vithya Lakshmi et al. 2021) | 180 | 20 | 0.8 | 2 | 2 | 75 | 85 |
| (Ud Din et al. 2019) | 180 | 0.2 | 3 | 200 | 1 | - | 91.5 |
| (Yuen, Chong, and Ramiah 2019) | 65 | 0.12 | 1.23 | 12 | 10 | 98 | 84 |
| **Proposed** | 130 | 3.2 | 0.45 - 1 | 5.5 | 2 | 99 | 80-90 |

# 4 Conclusion

Power management circuits are considered a very promising and reliable technology that allows to power WSNs. However, sometimes they lack efficiency in vibrational energy harvesting since they cannot properly scavenge and convert the output power. This research dissertation aims to solve the problem of the energy harvesting systems by proposing two circuits, an analog switch and a rectifier, designed in the standard 130 nm CMOS technology.

Firstly, a new analog switch configuration was designed. The main purpose of this circuit was to increase the efficiency of the output power extraction from the energy harvester by performing the Up-conversion technique. By attaching a switching-bulk technique and a back-to-back NMOS configuration, the presented analog switch could manage to achieve a low and constant ON-resistance of 216 Ω while blocking the reverse current from the output load. Furthermore, simulations results revealed that this circuit is robust to high temperatures and can reach an OFF-isolation of around -120 dB, which means that it can isolate the load from the input signal in the OFF state. These features were crucial to accomplish the low power consumption.

Secondly, a highly efficient active CMOS rectifier suitable to be applied to vibrational energy harvesters was also presented in this work. The results showed a voltage conversion efficiency of 99 % and a power conversion efficiency of 80-90 % for a low operation voltage from 0.45 V to 1 V and an operating frequency of 3.2 kHz. These features were achieved by combining an NVC with an active diode biased by a threshold cancellation circuit, which dynamically reduces the threshold voltage effect. Also, this structure avoids the reverse leakage current due to the use of a no-delay comparator, which was vital to reduce the power losses.

To conclude, it is believed that the two structures will efficiently solve the battery limitation problem of the WSNs. Thereby, further work passes for integrating the Analog Switch and the Rectifier in the PMC, fabrication of the IC, and respective testing in real environmental conditions.

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## Attachments

## Publications

**Godinho, António**, Zhaochu Yang, Tao Dong*, Luís Gonçalves, Paulo Mendes, Yumei Wen, Ping Li, and Zhuangde Jiang. 2021. "A Dynamic Threshold Cancellation Technique for a High-Power Conversion Efficiency CMOS Rectifier" *Sensors* 21, no. 20: 6883. https://doi.org/10.3390/s21206883

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# A Dynamic Threshold Cancellation Technique for a High-Power Conversion Efficiency CMOS Rectifier

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**Abstract:** Power conversion efficiency (PCE) has been one of the key concerns for power management circuits (PMC) due to the low output power of the vibrational energy harvesters. This work reports a dynamic threshold cancellation technique for a high-power conversion efficiency CMOS rectifier. The proposed rectifier consists of two stages, one passive stage with a negative voltage converter, and another stage with an active diode controlled by a threshold cancellation circuit. The former stage conducts the signal full-wave rectification with a voltage drop of 1 mV, whereas the latter reduces the reverse leakage current, consequently enhancing the output power delivered to the ohmic load. As a result, the rectifier can achieve a voltage and power conversion efficiency of over 99% and 90%, respectively, for an input voltage of 0.45 V and for low ohmic loads. The proposed circuit is designed in a standard 130 nm CMOS process and works for an operating frequency range from 800 Hz to 51.2 kHz, which is promising for practical applications.

**Keywords:** vibration energy harvester; power management circuit; CMOS rectifier; dynamic threshold cancellation technique; high power conversion efficiency



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## 1. Introduction

Presently, energy harvesting appears as a promising reliable technology that can prolong the lifetime of batteries and power wireless sensor networks (WSNs) for environmental monitoring [1]. However, in these WSN applications, ambient vibrations are unpredictable, time-varying, and low amplitude, which restricts the available power of the energy harvesting system [2]. To overcome these drawbacks, research groups have been focusing on using piezoelectric harvesters due to their high power density and capability to integrate MEMS and CMOS technology, making it possible to develop all the systems (energy harvester and electronic system) in a single chip [3–5]. Thus, to maximize the amount of energy transferred under different ambient conditions, a power management circuit (PMC) is crucial in order to extract, convert, store, regulate, and manage the scavenged energy from the piezoelectric device [6,7].

Because the vibrational energy sources produce AC signals, scavenging such energy requires a full-wave rectifier as a key circuit inside the PMC, which allows the AC/DC

conversion to properly power the WSNs. However, because the output power of the vibrational energy harvester is low [4], the high forward voltage required by standard full-wave diode bridges and Schottky diode rectifiers limits their use on these low power restrict applications [8]. To surpass these limitations, diode-connected MOS transistors have been widely used because they present similar I-V characteristics to the standard diodes. Thus, designing the rectifier in CMOS technology is highly desirable to decrease the device's form factor and easily integrate with the energy harvester while exploring new dynamic techniques to reduce the power consumption, achieve high PCE, and minimize leakage current [9,10].

Recent work has been developing dynamic threshold techniques to reduce the threshold voltage effect [11]. Addressing these techniques allows for the reduction of total voltage drop and mitigation of the reverse leakage current in the active stage. By attending to these concerns during the design of the circuit, it is possible to minimize the circuit's overall power and leakage current consumption. Thus, all these conditions were carefully considered during the design of the proposed high-power efficiency CMOS rectifier to attend to the demands of this application.

In this work, a new CMOS rectifier structure for piezoelectric energy harvesters is presented. It combines a passive stage negative voltage converter (NVC) with an active diode controlled by a dynamic threshold cancellation circuit to build a new architecture that can reduce its total voltage drop. With this configuration, a voltage drop lower than 2 mV can be achieved in the second stage, which consequently enhances features such as VCE and PCE, as well as reduces the reverse leakage current that flows from the load.

## 2. CMOS Rectifiers

### *2.1. Passive Rectifiers*

The CMOS gate cross coupled can replace the conventional full-wave bridge rectifier to overcome the high forward voltage drop because it allows a minimum input voltage to operate [10,12,13]. However, this topology still lacks efficiency due to the threshold voltage ($V_{TH}$) drop across the diode connected in each conduction path [13].

The fully cross-coupled rectifier intends to fulfill the gap of the previous configuration by eliminating all $V_{TH}$ drops, which reduces the voltage drop across this stage [13]. Consequently, this topology improves both PCE and VCE of the circuit [13]. However, the reverse leakage current appears to be the main disadvantage of using this single configuration, which affects the power transferred from the circuit to the load [10]. Thus, an extra circuit must be added to overcome this issue.

### *2.2. Active Rectifiers*

To prevent the circuit from reverse leakage current, the CMOS passive rectifiers combined with an active configuration can mitigate the reverse leakage current to enhance the DC power of the load [14–19]. In these active configurations, comparators are designed to control the gate voltage of the active diode (or so-called the main transistor) depending on its input and output voltage conditions. In work done by Peters et al. [15], an active rectifier with a bulk-input comparator technique is proposed for ultra-low-voltage energy harvesting systems. However, when the input voltage is higher than the output voltage, the PN junctions between the bulk and source terminal of the input transistor will be turned on. Consequently, the reverse leakage current will flow from the cathode terminal to the anode terminal through the body PN junctions, which compromises the efficiency of the circuit [8]. In addition, the proposed rectifier in [19] has a frequency range not suitable for the application of this research work. In contrast, in the following research papers [8,9,20,21], the frequency bandwidth corresponds to the desired application. The authors use two active diodes to control the reverse current that flows through the two NMOS in each input cycle, and two PMOS in cross-coupled to provide the conduction path. However, the dynamic range does not meet the requirements to achieve a high PCE for input voltages lower than 1 V, which is critical for energy harvesting applications [8].

In [20], the authors designed a fully active configuration using PMOS and NMOS to ensure that the reverse current through the PMOS input source is zero. The main disadvantage of this configuration occurs when the two NMOS devices turn on simultaneously, which leads to power losses. Chang et al. [21] proposed a rectifier with a third comparator to eliminate the oscillations of NMOS, which avoids the two active diodes turning on/off simultaneously. Nevertheless, the PCE is only high for an input voltage around 4.88 V.

However, the main limitations of these configurations are that they cannot control the $V_G$ of the main transistor to increase $V_{SG}$ during the conduction phase. Thus, it is not possible to reduce the internal resistance of this transistor, which limits the output power of the rectifier. Therefore, an extra circuit is needed to reduce the threshold voltage effect of this transistor to overcome these drawbacks.

### *2.3. Threshold Cancellation Topologies*

Several threshold cancellation topologies were proposed to enhance the output stored voltage by dynamically reducing the threshold voltage effect of the main transistor of the rectifier [22–25]. The threshold voltage is a process parameter dependent on the oxide type and thickness [24]. Low threshold voltage MOSFETs present a high leakage current caused by the low substrate doping, which leads to an increase in power consumption and reliability problems [24,26]. Thus, these threshold cancellation techniques are used to avoid those types of MOSFETs since it is only needed to reduce the threshold voltage effect when the main pass transistor is ON. In [25], a low-voltage CMOS rectifier is proposed to perform this technique by using the bootstrap technique, which has enhanced the output voltage stored in the load capacitor. However, for the minimum operating voltage of this configuration (0.8 V), the PCE of this circuit is around 30%, which is not enough for the requirements of this application.

An active bootstrapping rectifier is presented in [27] to overcome the issues of the previous work. This topology uses two active diodes to control the conduction path for each input cycle and a bootstrap technique to reduce the threshold voltage of both main pass PMOS. Additionally, an adaptive voltage converter is set in this work to adjust the gate voltage of the main pass PMOS, which reduces the voltage drop by reducing the on-resistance. Besides lowering the reverse leakage current, the PCE of this configuration can still be improved for input voltages smaller than 1 V. To overcome the low PCE values for a narrow input voltage range, in [28], a dual switching technique replaced the two active diodes. This approach can maintain a constant gate bias on the two main NMOS transistors, avoid the reverse leakage current, reduce the area on-chip, and enhance the PCE for low voltage applications. However, high values for PCE can only be obtained for input frequencies around 20 kHz, which makes the frequency bandwidth narrow.

## 3. Design Implementation

Regarding the inherent output characteristics of the piezoelectric transducer, the proposed CMOS rectifier was mainly designed to achieve a high PCE for wide low input voltage and frequency conditions. Therefore, the operational voltage ranges from 0.4 V to 1 V, and the working frequency varies from hundreds of Hz to a few kHz. In addition, the output impedance of the energy harvester is not considered in this design because the matching impedance process is performed before this rectification stage in the PMC. Thus, the main goal of this work is to reduce the voltage drop across the structure by applying a threshold cancellation technique that will further enhance the power converted to the ohmic load. These improvements will overcome the drawbacks of previous work by mitigating the reverse leakage current, and thus enhancing the PCE for a low input voltage range.

Figure 1 shows the simplified schematic of the proposed active rectifier. It consists of an NVC and an active diode biased by a threshold cancellation circuit. The first stage is set to perform the signal full-wave rectification. However, because this passive stage cannot control the reverse current from the load capacitor when the output voltage is higher

than the input, a second stage active diode (M5) is needed. This active stage is composed of a PMOS controlled by a threshold cancellation circuit with a bootstrapping capacitor to reduce the effective threshold of the active diode, and an adaptive voltage controller (AVC) to adjust the gate voltage of M5 by controlling the charging/discharging cycle of the bootstrapping capacitor. To perform it, a two-input common gate comparator and an NMOS transistor are used. Besides these stages, a dynamic switching bulk (DSB) technique was used to control the bulk voltage of the active diode PMOS.

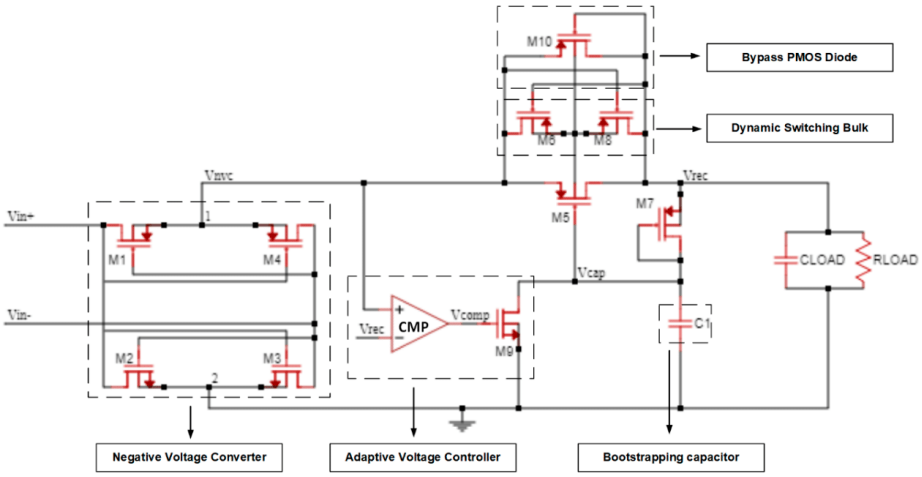


**Figure 1.** Schematic of the proposed active rectifier composed by a NVC and an active diode controlled by a threshold cancellation circuit.

### *3.1. Negative Voltage Converter*

The first stage is fully passive, and it is used to perform the signal full-wave rectification by applying a fully-cross coupled configuration. During the positive half period of the input signal ($V_{in+} > V_{in-}$), M1 and M3 will be conductive as soon as the input voltage gets larger than $V_{THn}$ and $|V_{THp}|$. In this cycle, node 1 is connected to $V_{in+}$ and node 2 to $V_{in-}$. For the negative period of the sine wave, M2 and M4 are conducting while the previous two transistors are now turned off (cut-off region). Therefore, the higher voltage potential is always at $V_{nvc}$, whereas the lowest potential is at 0 V. The voltage drop of the NVC is given by $V_{DSn} + V_{SDp}$ in each conduction path, where $V_{DSn}$ and $V_{SDp}$ are the voltage drop of NMOS transistors M2 or M3 and PMOS transistors M1 or M4, respectively.

To meet all the power restrictions related to the piezoelectric energy harvesting systems, the rectifier circuit must minimize the voltage drop across the rectification process. As less voltage drop occurs, both the VCE and the PCE of the circuit will be higher. For this stage, NVC, the main requirement is to decrease the voltage drop associated with each MOSFET by reducing their on-resistance.

### *3.2. Active Diode*

One of the main challenges on the rectifier circuit is to avoid the reverse leakage current by controlling the operation of transistor M5. Therefore, an active diode controlled with a threshold cancellation circuit can regulate the work behavior of this device depending on the voltage potential between the input and output. The deployed threshold cancellation circuit controls the gate potential of the MOSFET M5 by comparing the input/output voltage conditions. Additionally, the width of M5 has a large influence on the performance of this rectifier because the voltage drop is mainly affected by this parameter due to the

internal on-resistance. Consequently, since the gate capacitance of M5 depends on the width, the turn on/off time of the transistor will also be affected by this parameter. In addition, the DSB technique, composed of M6 and M8, is deployed to reduce the leakage current through the bulk terminal of M5 by connecting it to the higher potential ($V_{nvc}$ or $V_{rec}$). Another advantage of this technique is eliminating the body effect of M5, which reduces the rectifier voltage drop. Both M6 and M8 can be small in size since only a very low current flows through them during the start-up phase.

To assure a safe start-up of M5, a bypass PMOS diode (M10) was connected in parallel. This transistor makes the active diode more robust by preventing it from leakage current in the subtraction that induces latch-up. After the start-up phase, the bypass diode always operates in the cut-off region.

### *3.3. Threshold Cancellation Circuit*

In order to reduce the threshold voltage effect on M5, a bootstrap technique is used by attaching the capacitor $C_1$ to the output terminal. When the $V_{NVC}$ is higher than the output voltage $V_{rec}$, M5 is turned ON, since $V_{SG5}$ is no longer lower than $V_{TH5}$, and thus it can be defined in (1). Nevertheless, because M5 is operating in the deep-triode region due to $V_{SD5} \ll 2{\cdot}(V_{SG5} - |V_{TH5}|)$, $V_{SG5}$ can also be defined according to the on-resistance equation, see (2).

$$V_{SG5} = V_{NVC} - V_{CAP} \tag{1}$$

$$V_{SG5} = \frac{1}{\mu_p{\cdot}C_{ox}{\cdot}W_5/L_5{\cdot}R_{SD5}} + |V_{TH5}| \tag{2}$$

Here, $\mu_p$ is the carrier mobility, $C_{ox}$ is the oxide capacitance, $W_5/L_5$ is the aspect ratio of transistor M5, and $V_{TH5}$ is its respective threshold voltage.

The bootstrapping capacitor ($C_1$) is charged up through an auxiliary diode-connected PMOS transistor M7, and it maintains a value when the rectifier is under the steady-state regime. At this time, because $C_1$ is discharging, $V_{CAP}$ is one diode forward-bias voltage ($V_{TH7}$) bellow $V_{rec}$ due to M7 is being in the saturation region. Thus, the voltage held on the bootstrapping capacitor can be defined as:

$$V_{CAP} = V_{rec} - |V_{TH7}| \tag{3}$$

$V_{SG5}$ and $V_{CAP}$ from (2) and (3), respectively, can be replaced in (1), which means that $V_{rec}$ can now be defined according to the following equation:

$$V_{rec} = V_{NVC} - (|V_{TH5}| - |V_{TH7}|) - \frac{1}{\mu_p{\cdot}C_{ox}{\cdot}W_5/L_5{\cdot}R_{SD5}} \tag{4}$$

According to (4), the rectified signal is highly influenced by the size of M5 and the threshold voltage of both M5 and M7, and thus it is vital to manage these parameters to enhance the output signal voltage. The implemented threshold cancellation circuit reduces the voltage drop of the main pass transistor M5 by lowering the threshold voltage effect. Additionally, the size of the bootstrap capacitor is an important design concern for the implementation of the proposed rectifier. Integrated capacitors consume a large area on the chip when standard CMOS processes are used [24]. Therefore, $C_1$ was set at 200 fF not only to reduce the correspondent area on the die but also to have a faster charging/discharging time. Consequently, this low bootstrap capacitance allows a lower gate voltage of M5 at the ON state. Due to the reduction of its internal source to drain resistance, the voltage drop is decreased. The reverse leakage current during the OFF state will be avoided because $V_{SG5}$ is reduced. Moreover, it is necessary to have an auxiliary circuit to hold the $V_{CAP}$ node when M5 is OFF, and to discharge it at the opposite state.

The bootstrapping capacitor is used to reduce the threshold voltage effect of M5. However, an increase in its on-resistance can be noticed due to the reduction of $V_{SG5}$. Thus, a conduction path needs to be generated to discharge the gate of M5 during the ON state,

which will lead to a further increase of $V_{SG5}$. The proposed AVC is composed of NMOS M9 and a comparator CMP that drives its gate. When $V_{NVC}$ is higher than the output voltage $V_{rec}$, the comparator CMP should immediately turn on M9 to provide a discharge path of the $V_{CAP}$ node. Consequently, it will turn on the main pass transistor M5 with a low on-resistance. Because the large size of M5 increases the gate capacitance, the AVC must have a faster bias signal control to switch the discharge path of the gate node ($V_{CAP}$). Thus, the comparator must be designed to attend to these demands.

Figure 2 shows the proposed two-input common gate comparator. This comparator is composed of a current mirror stage to make the comparison, plus an inverter block to bias the gate of M9. Even if the transistor of the current mirror should be as small as possible to reduce the current consumption of the comparator, the size of M12 and M15 must be carefully chosen to manage the delay, and consequently, the reverse leakage current in M5. These two transistors cannot have the same W/L ratio as M11 and M14. Otherwise, this would generate a delay caused by the inverter's gate capacitance's low charging/discharging time. Additionally, they cannot be much larger than the other transistors because of the reduced time that M5 would be ON, which would lead to a PCE reduction. Therefore, M12 and M15 only need to be slightly higher to provide the required charging/discharging time to reduce the delay of the overall comparator. Table 1 summarizes the dimension values of the proposed rectifier circuit.

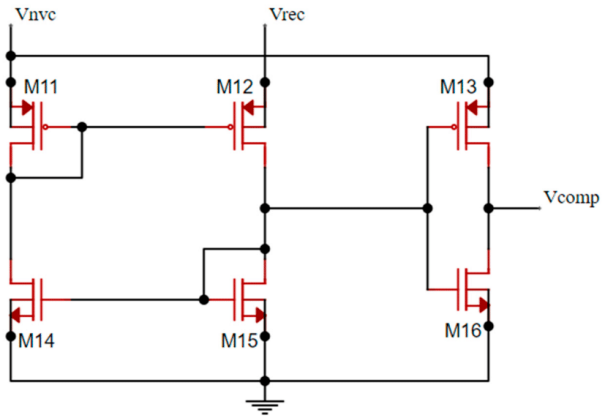


**Figure 2.** Schematic of the two-input common gate comparator CMP.

**Table 1.** Circuit transistor sizes.

| | Unit Size (µm/µm) | Multiply Factor |
|---|---|---|
| M1/2/3/4 | 100/0.13 | 100 |
| M5 | 100/0.13 | 50 |
| M6/7/10/11/13/14/16 | 0.28/0.13 | 1 |
| M7/9 | 20/0.13 | 1 |
| M11/12 | 0.34/0.13 | 1 |

## 4. Results and Discussion

The simulation experiments were carried out using Cadence Virtuoso Analog Design Environment with a 130 nm CMOS process. The respective physical layout of the CMOS rectifier is presented in Figure 3. To replicate the output behavior of the energy harvester, the default input sinusoidal voltage amplitude and frequency used in the simulations were 600 mV and 3.2 kHz, respectively. Throughout most of the tests, $C_{LOAD}$ and $R_{LOAD}$

were set at 2 µF and 5.5 kΩ to simulate the capacitance of the storing capacitor and the impedance of the electronics to be powered, respectively.

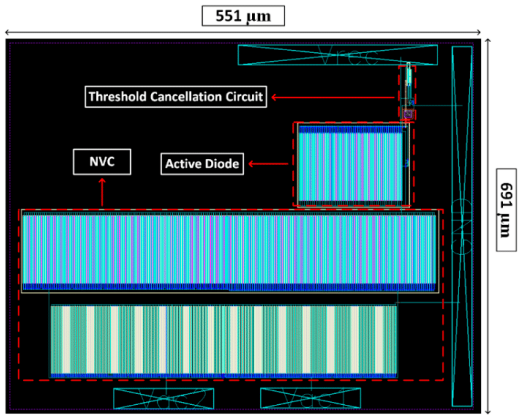


**Figure 3.** Physical layout of the proposed CMOS rectifier.

*4.1. Transient Behavior*

The transient performance of the output voltage, in both stages, is displayed in Figure 4. The first stage performs the full-wave rectification by converting the negative input voltages ($V_{IN}$) into positive ones ($V_{NVC}$). The voltage drop on this stage is around 1 mV, whereas the total voltage drop on the circuit is around 12 mV, which is possible due to the reduction of the internal resistance of the main pass transistor M5. The achieved voltage drop is crucial to enhance the output voltage across the load.

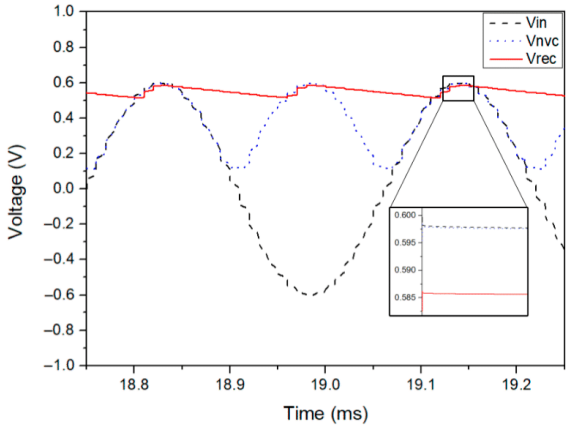


**Figure 4.** Simulated waveforms of the rectifier for $R_{LOAD} = 5.5$ kΩ and $C_{LOAD} = 2$ µF.

Figure 5 shows the VCE behavior versus the input voltage amplitude for different $R_{LOAD}$ values. It is possible to observe that the proposed rectifier can work efficiently for an input voltage range from 0.45 V to 1 V for different ohmic loads, with a VCE varying between 96% and 99%. For an input voltage lower than 0.4 V, the VCE sharply decreases because the NVC transistors will enter the subthreshold region or even cut-off. Moreover, it can be noticed that the rectifier VCE is higher for larger load resistors, as would be expected.

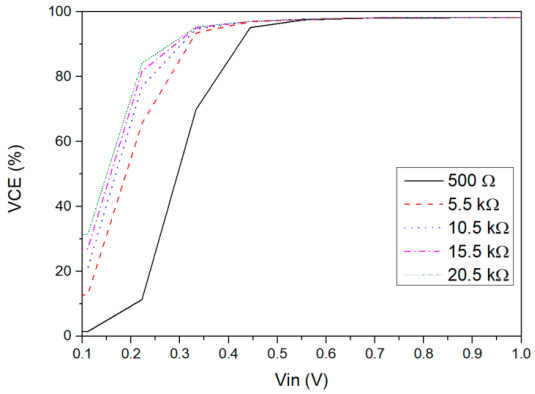


**Figure 5.** VCE versus input voltage amplitude simulated for different ohmic loads.

*4.2. Reverse Leakage Current Analysis*

The reverse leakage current analysis is one of the most important analyses to make in CMOS rectifiers because it affects the power efficiency of the overall system. This reverse leakage current is dependent on the delay of the comparator and, consequently, of the discharging path of the active diode provided by the AVC. Therefore, the analysis of the transient performance of the comparator is shown in Figure 6. It presents the output voltage of the comparator ($V_{CMP}$), the input and output voltage of the active diode used to perform the comparison, the gate voltage of M5 ($V_{CAP}$), and the current that flows through the active diode ($I_{M5}$). As can be observed, the comparator immediately turns on the gate of the AVC transistor to create the discharge path when $V_{NVC}$ exceeds $V_{rec}$. At this stage, the current is flowing through M5, and $V_{CAP}$ is low, which leads to a low voltage drop because $V_{SG}$ is high. When $V_{NVC}$ drops below $V_{rec}$, the comparator then quickly turns off the AVC, and consequently the active diode. Thus, the proposed structure does not exhibit reverse leakage current that would degrade the PCE of the proposed rectifier.

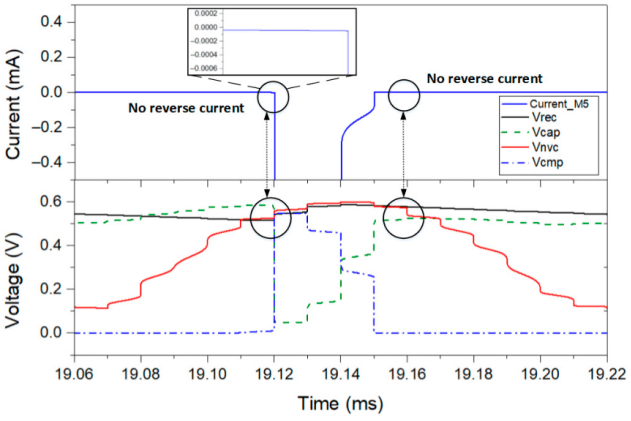


**Figure 6.** Simulated comparator behavior in steady state for $R_{LOAD} = 500\ \Omega$ and $C_{LOAD} = 2\ \mu F$.

*4.3. Power Efficiency*

The simulated power efficiency versus input voltage amplitude for different load resistors is presented in Figure 7. The definition of PCE is shown in (5):

$$PCE = \frac{\int_t^{t+T} V_{OUT}(t) \cdot I_{OUT}(t) dt}{\int_t^{t+T} V_{IN}(t) \cdot I_{IN}(t) dt} \cdot 100\%. \quad (5)$$

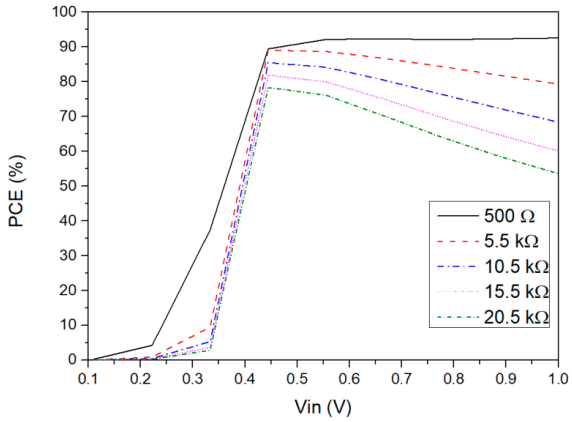


**Figure 7.** PCE versus input voltage amplitude simulated for different values of $R_{LOAD}$

The maximum PCE value of 94% can be found at 0.6 V for a $R_{LOAD}$ of 500 Ω. When $V_{in}$ is lower than this range, the PCE sharply decreases due to the low voltage efficiency, as noted in Section 4.1. Thus, the efficiency of the rectifier is poor in the ultra-low voltage range. Additionally, the PCE tends to decrease for higher input voltages because the power losses are mainly concentrated in the comparator. However, this case is not significant for ohmic loads lower than 15.5 kΩ. Moreover, for higher load resistors, the PCE tends to decrease due to the reduction of the output current, whereas the bias current that comes from the voltage source keeps almost constant. Regardless, from 0.45 V to 1 V, the power efficiency for low ohmic loads is considered as being good for this application. Additionally, the influence of the width of the NVC stage (M1–M4) and of M5 in both PCE and VCE can be observed in Figure 8. For this simulation test, the width of each stage was individually varied while the other was kept constant. This figure shows that the VCE and PCE features of both stages are at their maximum point for a width of 100 µm because the on-resistance of this transistor is directly influenced by the $W/L$ ratio of the MOSFET. Even if the gate capacitance of M5 increases with the size, Figure 6 shows that the threshold cancellation circuit can drive this large transistor.

Figure 9 shows the power efficiency versus input voltage amplitude for different input frequencies. The load capacitor value was adapted to keep the output ripple voltage small depending on the input frequency. It is possible to observe that the proposed rectifier can achieve a high-power efficiency for low input frequencies in the operating voltage range. However, when the input voltage and frequency are high, the power efficiency tends to slightly decrease due to the power losses in the NVC and in the active diode, which in this case it is caused by the output signal of the comparator being too fast. Consequently, the working time of transistor M5 will be too short, which reduces the amount of power converted to the load. Nonetheless, at typical energy harvesting frequencies, the performance of the CMOS rectifier for the presented frequency range is suitable for this application.

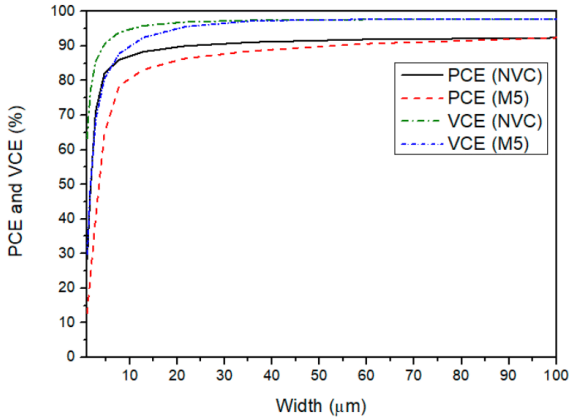


**Figure 8.** VCE and PCE features with the variation of the width of the NVC transistors and M5 (L = 0.13 µm).

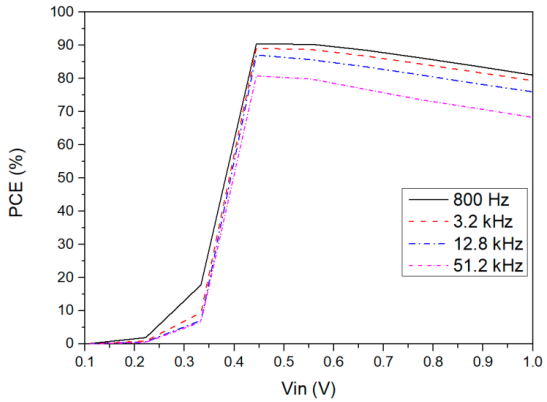


**Figure 9.** PCE versus input voltage amplitude simulated for different input frequencies for $R_{LOAD}$ = 5.5 kΩ.

To prove the robustness of the proposed CMOS rectifier, it was tested through the four known process corners, such as the typical ones, fast, slow, slow NMOS, and fast PMOS, and fast NMOS and slow PMOS. Figure 10 presents the PCE plots with the variation of the temperature depending on the process corner. According to the simulation results, it can be observed that PCE tends to decrease when a fast PMOS is used due to the high speed of the active diode, which reduces the ON time of the rectifier. Consequently, the power transferred to the load is affected. Nevertheless, as long as the temperature rises, the power consumption of the rectifier also increases because the MOS threshold voltage is an exponential function of the temperature.

The performance comparison between this work and previous rectifiers is presented in Table 2. It shows that the proposed configuration can achieve higher VCE and PCE for a low voltage range. Even if the PCE in [29] is higher for a high ohmic load, for this application, it is only expected a low impedance of the electronics to be powered. Thus, the achieved VCE and PCE in this work are higher than those in the reported literature, highlighting its added value [15,28,30]. In addition, this work presents a wider input voltage range compared to the previously noted article. Therefore, it can be concluded that

this rectifier can overcome the drawbacks of the structures discussed in Section 2, which means that this rectifier is very suitable for energy harvesting applications.

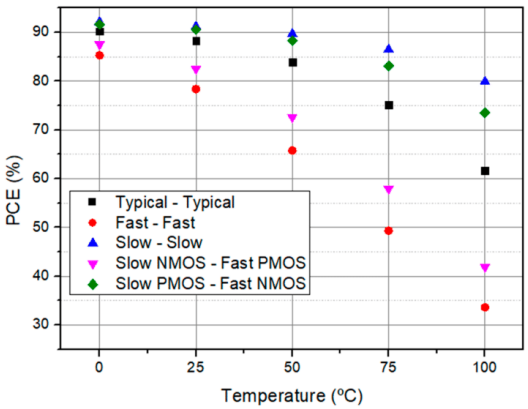


**Figure 10.** PCE variation with temperature depending on the process corner variation for a $R_{LOAD}$ = 5.5 kΩ.

**Table 2.** Research comparison.

| Ref. | Tech. (nm) | $f_{in}$ (kHz) | $V_{in}$ (V) | $R_{LOAD}$ (kΩ) | $C_{LOAD}$ (µF) | VCE (%) | PCE (%) |
|---|---|---|---|---|---|---|---|
| [15] | 350 | 0.1 | 0.5 | 50 | 10 | 99 | 84 |
| [28] | 180 | 20 | 0.8 | 2 | 2 | 75 | 85 |
| [29] | 180 | 0.2 | 3 | 200 | 1 | - | 91.5 |
| [30] | 65 | 0.12 | 1.23 | 12 | 10 | 98 | 84 |
| Proposed | 130 | 3.2 | 0.45–1 | 5.5 | 2 | 99 | 80–90 |

## 5. Conclusions

A highly efficient active CMOS rectifier suitable to be applied to vibrational energy harvesters was presented in this work. The proposed structure was designed in 130 nm CMOS technology, and the results showed a VCE of 99% and a PCE of 80–90% for a low operation voltage from 0.45 V to 1 V and for an operating frequency of 3.2 kHz, which proves the value of this work for a practical energy harvesting application. These features were achieved by combining an NVC with an active diode biased by a threshold cancellation circuit, which dynamically reduces the threshold voltage effect. Moreover, this structure avoids the reverse leakage current due to the use of a no-delay comparator, which was vital to reduce the power losses.

The research work focused on developing a highly efficient rectifier to be integrated into a PMC. It is believed that this structure will efficiently contribute to solving the battery limitation problems of the WSNs for an environmental monitoring application. Further work should focus on integrating the proposed structure in the PMC and respective testing in real environmental conditions.

**Author Contributions:** A.G. was responsible for the investigation, design of the proposed circuit, simulations, respective validation, and the writing of the original draft. Z.Y. was involved in the investigation, simulations, respective validation, and in the writing revision and editing. T.D. supervised the research, administrated the project, and acquired the project funding. L.G. and P.M. were involved in the research supervision and validation of the simulation. Y.W. and P.L. were responsible for the conceptualization of the research and the administration of the project. Z.J. was also involved in the conceptualization of the research. All authors have read and agreed to the published version of the manuscript.

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