Universidade do Minho
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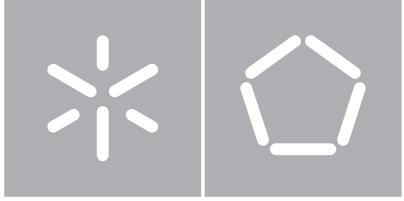
Piezoresistive thin film by metal-induced crystallization

Outubro de 2022



Universidade do Minho
Escola de Engenharia
Departamento de Eletrónica Industrial

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Piezoresistive thin film by metal-induced crystallization

Dissertação de Mestrado
Mestrado em Engenharia Física

Trabalho realizado sob orientação de

Professor Doutor Alexandre Ferreira da Silva
Doutor Filipe Serra Alves

Outubro de 2022

STATEMENT OF INTEGRITY

I hereby declare having conducted this academic work with integrity. I confirm that I have not used plagiarism or any form of undue use of information or falsification of results along the process leading to its elaboration.

I further declare that I have fully acknowledged the Code of Ethical Conduct of the University of Minho.

Agradecimentos

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Resumo

Dispositivos MEMS baseados no método de transdução piezoresistivo não só têm um processo de fabrico simples ou podem demonstrar boa sensibilidade associada ao material piezoresistivo usado como também providencia o uso de eletrónica de instrumentação simples. Uma vez que os dispositivos MEMS são fabricados a baixas temperaturas (<500 °C), existe um grande interesse em desenvolver materiais piezoresistivos que sejam compatíveis com técnicas de fabrico de dispositivos MEMS. De igual modo, a junção de materiais piezoresisitvos com dispositivos MEMS flexíveis abre portas para inúmeras aplicações, o que intensifica a motivação de desenvolver materiais piezoresistivos a baixas temperaturas.

O presente trabalho apresenta o fabrico de um material piezorresistivo, silício policristalino, pela cristalização induzida por metal mediada por AlSiCU. Esta é a primeira vez, do melhor conhecimento da autora que este material é utilizado como catalisador deste processo de cristalização.

O material foi desenvolvido sobre uma bolacha de silício e as condições de fabrico foram variadas de modo a obter um filme cristalino à temperatura mais baixa possível. A viabilidade de desenvolver dispositivos flexíveis com polissílicio foi investigada a partir do teste de cristalização deste material sobre uma camada polimérica. O material demonstrou uma estrutura semelhante à obtida sobre a bolacha de silício e foi ainda possível padronizar o material sem que este se desagregasse da camada polimérica.

Numa fase posterior, dispositivos de teste foram projetados e fabricados de modo a ser possível caracterizar eletrica e mecanicamente o material desenvolvido. O polissilício obtido apresenta um Coeficiente de Temperatura (TCR) de -0.000298 /°C e um Fator de Gauge (GF) of 12.31. Os dispositivos fabricados neste trabalho demonstram sensibilidade à radiação, o que significa que este material poderá ser utilizado para aplicações de foto deteção.

Palavras-chave: Piezoresistividade, Polissilício, AlSiCu, Baixas temperaturas, Substratos flexíveis, Fator de Gauge

Abstract

MEMS devices based on the piezoresistive transduction mechanisms, not only have simple fabrication processes, or can achieve good sensitivity associated with the piezoresistive material used, but also enables the use of simple instrumentation electronics. Due to the low-temperature procedure used to manufacture MEMS devices (<500 °C), there is interest in creating piezoresistive materials that are compatible with MEMS fabrication techniques. The development of low-temperature piezoresistive materials not only provides compatibility with standard Silicon-based MEMS fabrication processes, but also enables the exploration of such material in other types of substrates, like flexible, polymer-based ones, opening the door for many device applications.

This work presents the fabrication of a piezoresistive material, polycrystalline silicon, by a metal induced crystallization process mediated by AlSiCu at temperatures as low as 450 °C. It is the first time, to the best of the author's knowledge, that this alloy has been used as crystallization catalyst.

The material was obtained on top of a Si wafer, and the fabrication conditions were varied in order to obtain a crystalline film at the lowest temperature possible. The feasibility of developing flexible devices with poly-Si was then investigated by testing the crystallization technique on top of a polymeric layer. The material showed a similar structure to the one obtained on top of the Si wafer and could be patterned without flaking from the polymeric layer.

In a posterior phase, some test devices were designed and fabricated to allow the electrical and mechanical characterization of the material. The poly-Si developed shows a Temperature Coefficient of Resistance (TCR) of -0.000298 /°C and a Gauge Factor (GF) of 12.31. The devices fabricated in this work also show sensitivity to radiation, meaning that the developed material can be posteriorly used for photo-detection applications.

Key-words: Piezoresistance, Polysilicon, AlSiCu, Low-temperature, Flexible substrates, Gauge Factor

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Nomenclature

ΔG	Gibbs energy change
ϵ	Electric field vector
μ	Electron's charge mobility
μ_{Ni}	Chemical potential of Nickel
μ_{Si}	Chemical potential of Silicon
π	Piezoresistive coefficients
ρ	Resistivity of the material
σ	Stress
σ_s	Standard Deviation
υ	Poisson's Ratio
ε	Strain
ε_0	Vacuum permittivity
ε_r	Relative permittivity
A	Area
d	Distance
e	Electron charge
G	Gibbs energy of a system
H	Enthalpy

J	Current vector
L	Length of piezoresistive bar
n	Concentration of charge carriers
R	Electrical resistance
R_0	Electrical resistance at reference temperature
R_s	Sheet resistance
S	Entropy
T	Temperature
T_0	Reference temperature
T_c	Crystallization temperature
T_e	Eutectic temperature
Y	Young's Modulus

Acronyms

a-Si	Amorphous Silicon.
AIC	Aluminum Induced Crystallization.
BS	Backside.
BSED	Backscattered Electron Detector.
CVD	Chemical Vapor Deposition.
EDX	Energy-dispersive X-ray Spectroscopy.
ELA	Excimer Laser Annealing.
FEM	Finite Element Method.
GF	Gauge Factor.
INL	International Iberian Laboratory of Nanotechnology.
MEMS	Micro-electro-mechanical systems.
MIC	Metal Induced Crystallization.
MSM	Metal-Semiconductor-Metal.
PCB	Printed Circuit Board.
PECVD	Plasma Enhanced Chemical Vapor Deposition.
PI	Polyimide.
poly-Si	Polycrystalline Silicon.
RIE	Reactive Ion Etching.

SEM Scanning Electron Microscopy.

SPC Solid Phase Crystalization.

TCR Temperature Coefficient of Resistance.

XRD X-ray Dispersion.

Introduction

Since the beginning of our existence, we use our touch ability to interact with the world around us in order to survive. The skin is our largest sensor, and it allows the perception of temperature, textures, objects, and their manipulation. In today's world, we have electronic systems that, based on the capabilities of our skin, can convert external stimuli like pressure, force, and strain into an electrical signal for the most diverse applications.

For instance, Micro-electro-mechanical systems (MEMS) have been a focus of attention since this technology combines electrical and mechanical properties to create small transduction devices that can be applied to space-confined environments. Combining this technology with flexible electronics is very appealing since it broadens the possible applications to non-planar surfaces [Yang and Zhang, 2021].

One conceivable application is health monitoring devices [Liu et al., 2017], in which their flexible capability is critical since rigid sensors are not ergonomic and do not provide strong adhesion to the body. However, this is not the only application in which flexible sensors are convenient. Human-machine interaction profits from this characteristic as well, either for physiological measurement required in virtual reality equipment or for robots with incorporated electronic skin to perceive and interact with the external environment [Yin et al., 2021].

In earlier times, flexible devices consisted of a thin film that, due to its reduced thickness, could bend and be placed on curved surfaces [Crabb and Treble, 1967]. However, the latest devices take profit from surface micromachining techniques to assemble the sensors' layers on top of flexible substrates like polyimide, SU-8 or PDMS [Corzo et al., 2020].

Each sensor works according to a transduction mechanism, and the technology that best suits a specific application determines the selection of the sensing material.

Of all the existing sensing methods, the most common are capacitive, piezoelectric and piezoresistive. Each principle has its merits and demerits, summarized on Table 1.1, which require a thorough evaluation to choose which technology best satisfies the desired characteristics of the device.

Table 1.1: Advantages and disadvantages of different types of transduction mechanisms.

Mechanism	Advantages	Disadvantages
Capacitance	Simple structure Low power consumption Temperature insensitive	Non-linearity Parasitic capacitance Noise susceptible
Piezolectricity	No power supply Fast response High sensitivity	Unable to measure static signals
Piezoresistance	Simple manufacturing Design flexibility Wide detection range	Prone to hysteresis Temperature sensitive

Capacitance

Capacitive sensors are typically composed of two electrodes in a parallel-plate configuration, with a dielectric layer between them, and the capacitance value for this model is determined according to (1.1).

$$C = \varepsilon_0 \varepsilon_r \cdot \frac{A}{d} \tag{1.1}$$

In this equation, ε_0 is the dielectric constant of vacuum and ε_r of the dielectric layer between the plates. A is the overlapping area of the electrodes and d the distance between them, as illustrated on Figure 1.1.

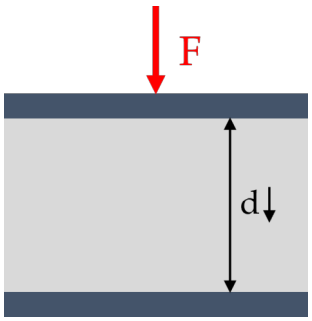


Figure 1.1: Illustration of the capacitance transduction mechanism.

Some advantages of using this method include its simple design structure and low power consumption [Li et al., 2020]. Also, sensors based on the capacitive mechanism are less sensitive to temperature drifts compared to other methods [Qin et al., 2021]. Nonetheless, for gap changing sensors, this sensing

mechanism has the problem of non-linearity, since the capacitance value C is inversely proportional to d. It is a mechanism very sensitive to parasitic capacitance, using demanding for more complex electronics.

Lastly, since C is directly proportional to A, the miniaturization of capacitive devices leads to signal reduction and consequent reduction of signal-to-noise ratio [Tiwana et al., 2012].

Piezoelectricity

Piezoelectricity can be described as the ability of some materials to generate an electrical signal when subjected to an external force, pressure, or strain since these external stimuli induce the distribution of charge on top of the material's surfaces as illustrated in Figure 1.2.

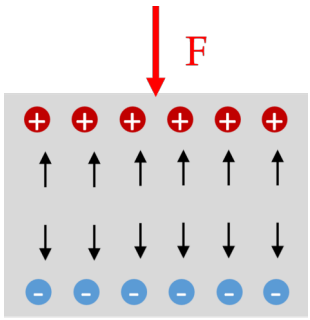


Figure 1.2: Illustration of the piezoelectric transduction mechanism.

Sensors based on the piezoelectric effect have a fast response time and high sensitivity [Li et al., 2018], but the greatest advantage is that they do not require an external supply voltage, which makes them convenient for implantable systems [Latif et al., 2021] and remotely controlled devices [Dong et al., 2017].

However, the frequency response of this type of sensor is not constant since it acts like a high-pass filter for low frequencies regime, which makes this transduction mechanism unsuitable for static force measurements [Huang et al., 2019].

Piezoresistance

The piezoresistive effect is associated with an electrical resistance change when an external force is applied to the sensor (Figure 1.3). This is the most used transduction mechanism in force and pressure sensors not only by virtue of their simple manufacturing process and integration with electronic circuits but also thanks to their good sensitivity, reliability, and wide detection range [Almassri et al., 2015].

However, this type of sensors can suffer from hysteresis and depending on the piezoresistive material, they can be highly sensitive to temperature variations [Chang et al., 2020]. Usually, sensors of this kind consist of a suspended diaphragm with embedded piezoresistive material on a Wheatstone bridge configuration to eliminate the temperature dependence.

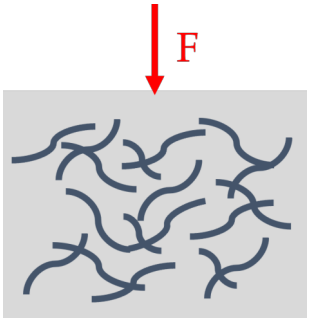


Figure 1.3: Illustration of the piezoresistive transduction mechanism.

1.1 Motivation and problem statement

MEMS devices based on the piezoresistive transduction mechanisms, not only have simple fabrication processes, or can achieve good sensitivity associated with the piezoresistive material used, but also enables the use of simple instrumentation electronics. The fabrication of MEMS devices is mainly based on low-temperature process (< 500 °C), so there is an interest in the development of low-temperature piezoresistive materials, to largely increase the compatibility with most MEMS fabrication processes. Besides the compatibility with standard Silicon-based MEMS fabrication processes, the development of low-temperature piezoresistive materials enables the exploration of such material in other types of substrates, like flexible, polymer-based ones, opening the door for many device applications.

Different approaches are used to increase the mechanical flexibility of MEMS. One of the strategies takes advantage of naturally flexible materials, such as conductive elastomers [Shi et al., 2018]. On the downside, these materials are incompatible with classic fabrication processes.

Another option is using transfer techniques to obtain bendable thin films on top of flexible substrates, but the high costs and low yield of the process are the principal weaknesses [Kervran et al., 2015].

As an alternative, the piezoresistive material can be deposited directly on a polymeric substrate. However, the fabrication temperature is constrained to the temperature that the polymers can handle before losing its integrity. For example, Polyimide (PI) is one of the most widely used polymers for flexible substrates and is thermally stable at temperatures up to 500 °C.

Another issue of using polymeric substrates such as PI is that it presents a smooth surface and is

chemically inert. This leads to poor adhesion of other materials and often requires specific treatments for its improvement [Cen-Puc et al., 2021].

This means that developing a piezoresistive material at low temperatures not only allows its integration with MEMS a fabrication process already well established, as it expands the application of the material to flexible MEMS.

1.2 Goals and research questions

With an eye on the possible applications that flexible sensors based on piezoresistive materials offer, the present work is done with the collaboration of the International Iberian Laboratory of Nanotechnology (INL) in Braga, Portugal and the main goal is to develop a microfabrication process of piezoresistive films at low temperatures to be used in future MEMS devices and to study the viability to use this material on top of flexible substrates.

The pursuing of these objectives were conducted by the research questions here enumerated:

- Which piezoresistive materials have been implemented in the literature, and what differentiates them?
- Which strategies have already been used to obtain piezoresistive material at low temperatures?
- Which parameters should be considered to evaluate the quality of the developed piezoresistive film?
- What is the feasibility of acquiring the piezoresistive material on a flexible layer?
- In which way can the piezoresistive material response be influenced by external factors?

1.3 Methodology

In order to accomplish the goal previously established, the dissertation project was divided in 4 main steps (Figure 1.4):

- **1st step:** The first phase consists in the study of piezoresistive material already implemented in the previous works and the evaluation of their characteristics.
- **2nd step:** Based on that study, the second step of the project involves the investigation of deposition technologies that allow the fabrication of piezoresistive films on flexible substrates.

- **3rd step**: The implementation of a low temperature deposition process is imposed based on the previous review and optimized by an iterative procedure.
- **4th step:** On a last phase, the behavior of the obtained piezoresistive film is characterized based on the piezoresistive response.

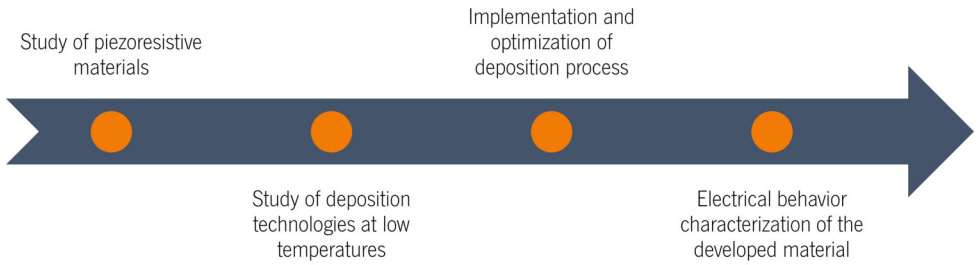


Figure 1.4: Timeline infographic of the project's main phases.

1.4 Thesis outline

The dissertation is composed of six chapters, including the current introduction chapter. Chapter 2 begins with an introduction on the theoretical fundamentals that act as a support for the notations used throughout the document, and the concepts behind piezoresistance. It follows with a literature review on the existing piezoresistive materials and their characteristics, with an emphasis on polycrystalline silicon, the material developed in this dissertation. The chapter proceeds with a discussion of existing polycrystalline silicon deposition technologies and approaches for lowering the temperature of the processes. Finally, an explanation is provided as to why the Aluminum Induced Crystallization (AIC) procedure was chosen to develop polysilicon, with a complementary study of the parameters that impact this process.

Chapter 3 describes of the experimental procedures implemented for developing a polycrystalline silicon thin film and closes with an analysis of the final results in light of the previous literature review.

Following the discussion of the process development in the preceding chapter, Chapter 4 provides an insight into manufacturing of the test structures intended for characterization.

Chapter 5 explores the characterization procedures to validate the piezoresistive effect of the obtained film and the results obtained.

The last chapter of this dissertation, namely Chapter 6, summarizes the accomplishments achieved by answering the research questions and establishes research lines to be addressed in future work.

State of the Art

Chapter 1 mentions that the aim of this work is the development of a piezoresistive material at low temperatures. The present chapter delves into the physics of piezoresistivity, providing a brief explanation of complementary concepts such as stress and strain and their relationship with a material's resistance.

This theoretical introduction is followed by a review and comparison of the characteristics of several piezoresistive materials. The chapter then follows with the description of the various fabrication methods before focusing on appropriate techniques at low temperatures. It concludes with a more in-depth overview of the fabrication process used in this dissertation.

2.1 Theoretical Principles

In order to better understand the concept of piezoresistivity, it is necessary to introduce the physics behind this transduction mechanism. This section provides the theoretical support needed before focusing on the analysis of different piezoresistive materials and their characteristics.

2.1.1 Stress and strain

When a force F is exerted on a certain body with a cross-section area A and length l, as illustrated in Figure 2.1, the element is subjected to stress σ, according to (2.1).

$$\sigma = \frac{F}{A} \tag{2.1}$$

This force can be a tensile or compressive type if it is outer or inner normal to the surface's plane, respectively. If the direction of the force is considered parallel to the object's surface, then it is called a shear force.

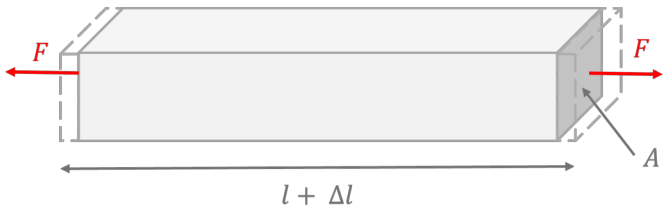


Figure 2.1: Illustration of a rigid body with a cross-section area A subjected to a tensile force, F.

The applied force induces a deformation Δl in the body described by the strain, ε, expressed in (2.2).

$$\varepsilon = \frac{\Delta l}{l} \tag{2.2}$$

In the elastic regime and for isotropic bodies[1], the stress relates to strain by Hooke's Law:

$$\sigma = Y \cdot \varepsilon \tag{2.3}$$

where Y is the Young's Modulus of the material subjected to the force.

However, for an anisotropic crystal like silicon (Si), the stress is dependent on the direction of the force applied and must be described by a tensor [Wortman and Evans, 1965]. Consider the unit element represented on Figure 2.2.

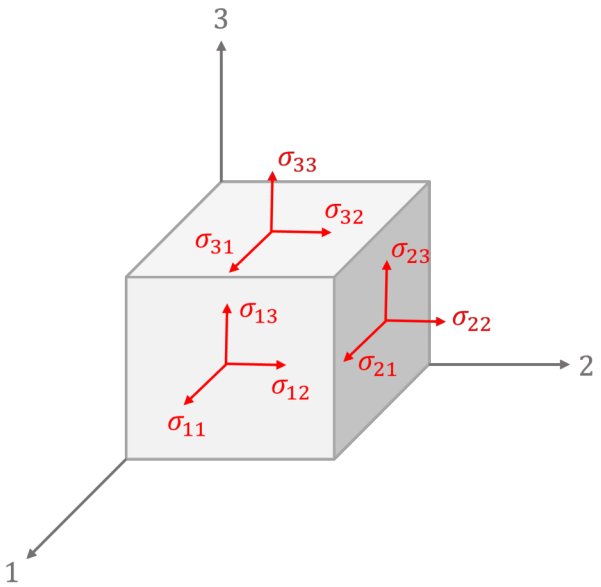


Figure 2.2: Illustration of the general stress tensor components applied to a unit cell.

[1] **Isotropic bodies**: bodies whose properties are independent of the orientation

The stress applied to this unit element is described by a stress tensor σ_{ij}, where i denotes the direction of the normal vector of the surface where the stress is applied and j denotes the direction of the applied stress. When $i = j$ it means that the applied stress is normal to the surface, whereas $i \neq j$ denotes a shear stress.

$$\sigma = \begin{pmatrix} \sigma_{11} & \sigma_{12} & \sigma_{13} \\ \sigma_{21} & \sigma_{22} & \sigma_{23} \\ \sigma_{31} & \sigma_{32} & \sigma_{33} \end{pmatrix} \tag{2.4}$$

Considering the equilibrium situation, the stress tensor σ is always symmetric, which means that $\sigma_{ij} = \sigma_{ji}$ making a stress tensor with only six independent components [Atanackovic and Guran, 2000].

The stress tensor of (2.4) relates to strain of the material through the compliance tensor, S:

$$\varepsilon_{ij} = S_{ijkl} \cdot \sigma_{kl} \tag{2.5}$$

2.1.2 Piezoresistance fundamentals

The piezoresistive effect was first discovered by Lord Kelvin in 1856, but it wasn't until 100 years later that Smith made a relevant research reporting the effect in germanium and silicon [Smith, 1954], boosting the development of piezoresistive devices. The term piezoresistance comes from the analogy with the word piezoelectricity and describes the variation of electrical resistance given by (2.6) of a metal or semiconductor when subjected to an external force. In this equation ρ is the resistivity of the material, l the length and A the cross-section area as previously stated.

$$R = \frac{\rho l}{A} \tag{2.6}$$

When the material is elastically deformed, its electrical resistance deviates according to (2.7).

$$\frac{\Delta R}{R} = \frac{\Delta \rho}{\rho} + \frac{\Delta l}{l} - \frac{\Delta A}{A} \tag{2.7}$$

This expression can be rewritten as (2.8) where υ is the Poisson ratio of the material.

$$\frac{\Delta R}{R} = (1 + 2\upsilon)\varepsilon + \frac{\Delta \rho}{\rho} \tag{2.8}$$

The first therm of the equation, $(1+2\upsilon)\varepsilon$, describes the geometrical change that the material suffers due to strain, whereas the second therm, $\Delta\rho/\rho$, relates to variations of the resistivity at the atomic level.

Depending on the material's nature, the dominant effect diverges. For metals, the prevailing effect is the dimensional modification while for semiconductors the opposite is true, since piezoresistance changes are 50 times more significant in this case [Kanda, 1991], which will be explored further.

Typically, the resistance change that a material undergoes with applied strain is quantified by the GF given by (2.9).

$$GF = \frac{\Delta R/R}{\Delta l/l} = \frac{\Delta R/R}{\varepsilon} \tag{2.9}$$

The higher the variation in resistance, the greater the value of this quantity. Higher gauge factors are beneficial since they imply that the piezoresistive sensor is more responsive to strain.

2.1.3 Piezoresistivity in semiconductors

When it comes to semiconductors, there is a change in the material's conductivity, in addition to the geometrical changes that contribute to the piezoresistive effect, as previously stated. From Drude's formula, the resistivity of a semiconductor is given by (2.10).

$$\rho = \frac{1}{en\mu} \tag{2.10}$$

Here e is the electron charge, n is the concentration of charge carriers and μ is their mobility.

By introducing the Drude's formula in (2.9) we obtain

$$GF = \frac{\Delta R/R}{\varepsilon} = 1 + 2\upsilon - \frac{1}{\varepsilon}\frac{\Delta(n\mu)}{n\mu} \tag{2.11}$$

This means that a change in the material's resistivity comes from the change in the number of charge carriers and their respective mobility, as the [Bardeen and Shockley, 1950] model proposes. The model states that when a piezoresistive semiconductor is under strain, there is a lattice deformation which leads to a reorganization of the charge carriers in the bands' structure. This effect leads to the modification of the effective mass of charge carriers and, consequently, their mobility.

From a phenomenological approach introduced by [Kanda, 1991], the relative change of the resistivity can be expressed as a function of the piezoresistive coefficients (π_{ij}).

From Ohm's law, the electric field vector, ϵ, is related to the current vector, J, by the 3x3 resistivity tensor ρ according to the expression $\epsilon = \rho J$.

The relative change of resistivity is then related to stress by the piezoresistive coefficients that form a 6×6 matrix:

$$\frac{\Delta\rho_i}{\rho} = \sum_{j=1}^{6} \pi_{ij} \cdot \sigma_j \tag{2.12}$$

For a crystal with a cubic structure, there are only 3 independent coefficients: π_{11}, π_{12} and π_{44}.

The change in the resistivity presented in (2.12) is usually written in order to the longitudinal (π_l) and transversal (π_t) piezoresistive coefficients, as shown in (2.13).

$$\frac{\Delta\rho}{\rho} = \pi_l\sigma_l + \pi_t\sigma_t \tag{2.13}$$

In this equation σ_l and σ_t are the stress parallel and perpendicular to the current flow, respectively.

The relationship between π_l, π_t and the coefficients π_{11}, π_{12} and π_{44} depends on the crystalline orientation of the piezoresistors. For example, for a piezoresistor of Si oriented along the (100) plane on top of a $<100>$ Si wafer, the piezoresistive coefficients are:

$$\begin{aligned} \pi_l &= \pi_{11} \\ \pi_t &= \pi_{12} \end{aligned} \tag{2.14}$$

In the case where the piezoresistors are aligned with the (110) plane, the relationship changes to:

$$\begin{aligned} \pi_l &= \frac{1}{2}(\pi_{11} + \pi_{12} + \pi_{44}) \\ \pi_t &= \frac{1}{2}(\pi_{11} + \pi_{12} - \pi_{44}) \end{aligned} \tag{2.15}$$

The piezoresistive material typically has a preferred direction where the sensitivity to strain is higher, meaning that these coefficients will have distinct values. Since the Gauge Factor is related to the piezoresistive coefficients, the positioning of the piezoresistor in the device must consider this factor.

2.2 Piezoresistive materials

The Gauge Factor, as presented in (2.9), is directly related to the variation of electrical resistance of the piezoresistor and consequently to the device's sensitivity. Several materials exhibit piezoresistivity and may be used to develop piezoresistive sensors, including metals, semiconductors, and alloys, as Table 2.1 shows. As a result, selecting the piezoresistor that best matches its future application is a critical undertaking.

Table 2.1: Gauge Factor (GF) of various piezoresistive materials.

Material	GF	Reference
Au	2.88	[Oerke et al., 2014]
Cu	3.88	[Jen et al., 2003]
ITO (7:3)	-2.10	[Oerke et al., 2014]
NiCr (8:2)	1.95 - 2.5	[Kazi et al., 2006]
<111> p-Si	175	[Fiorillo et al., 2018]
poly-Si	10 - 77	[Wu et al., 2016, Chuang et al., 2018]
3C-SiC	30.3	[Phan et al., 2014]
poly-SiGe	20.2	[Gonzalez et al., 2010]
DLC	16-68	[Tibrewala et al., 2007]

Due to silicon's widespread use in the semiconductor industry, the material is easily available, and the manufacturing processes are well-established. In particular, poly-Si has a relatively high Gauge Factor when compared to other materials, which makes this semiconductor attractive for pressure sensing applications. Even though single crystalline silicon has higher GF than the polycrystalline counterpart, the latter has the ability to be placed on different substrates since randomly oriented crystals do not require lattice matching [Grech et al., 2016].

However, this material has demerits already reported in literature, namely problems with reproducibility [Barlian et al., 2009, Fu et al., 2004] which must be acknowledged.

Another characteristic of poly-Si film is that its electrical behavior is highly reliant on the doping level and structural properties. [French and Evans, 1989] presents a theoretical model for the Gauge Factor of a polycrystalline silicon film, suggesting that larger grain sizes result in a higher Gauge Factor.

Besides the Gauge Factor, another factor that needs to be taken into consideration when evaluating piezoresistive materials is the TCR given by:

$$TCR = \frac{1}{R_0}\frac{dR(T)}{dT}\bigg|_{T=T_0} \tag{2.16}$$

In this equation, T_0 is the reference temperature and R_0 is the resistance evaluated at T_0. If this coefficient is high, it means that the electrical resistance of the material is strongly dependent of the surroundings' temperature.

2.3 Deposition methods

The manufacturing method of polycrystalline silicon must be carried out at low temperatures, as previously stated, to be compatible with MEMS fabrication technologies and to allow the fabrication of flexible devices. The following sections offer an overview of several deposition techniques used to produce polycrystalline silicon, focusing on the method employed in this project.

2.3.1 Direct growth

The most common technique for making a poly-Si film is called Chemical Vapor Deposition (CVD), in which a precursor gas like silane (SiH_4) combines with other substances within a chamber to produce a non-volatile compound that deposits on the wafer substrate. When treated at low temperatures, as seen on the graphic of Figure 2.3, this results in the creation of silicon in the amorphous phase. This outcome indicates that the procedure must be carried out at temperatures over 600 °C to produce a layer with a crystalline structure.

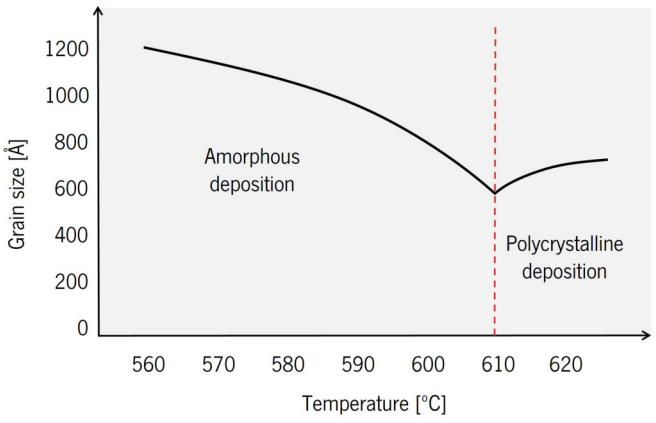


Figure 2.3: Silicon grain size as a function of the annealing temperature. Adapted from [French, 2002].

In addition, the obtained film is insufficiently doped, requiring an extra doping step reaching temperatures around 1100 °C [Wang et al., 2015, Liu et al., 2009]. Due to the thermal restriction of the polymeric substrates, this process is not a suitable solution.

Employing a DC bias to the substrate can overcome this drawback since this electrical signal affects the crystallinity and growth of the deposited film. [Liu et al., 2020] states that applying a negative voltage between 50 and 150 V during a plasma enhanced CVD process allows the formation of a crystalline film at temperatures as low as 100 °C. The fundamental disadvantage of this strategy is that it may harm the substrate-film interface by creating cracks in the crystalline film [Nozawa et al., 1997], especially when working with flexible substrates [Patra and Das, 2022].

Another approach to reducing the process temperature is by adding Hydrochloric acid (HCl) gas to the chamber [hoon Lee et al., 2016]. The presence of HCl is proven to inhibit the precipitation of amorphous silicon, allowing the formation of polycrystalline silicon at temperatures as low as 200 °C. However, this gas is highly corrosive, damaging structures made of metal.

2.3.2 Crystallization

The other way of obtaining poly-Si is by using alternative crystallization methods where an amorphous silicon layer is primarily deposited followed by a thermal treatment that allows the phase change from amorphous to crystalline.

Solid Phase Crystallization

Solid Phase Crystalization (SPC), illustrated in Figure 2.4, is a crystallization technique where a-Si deposited on a substrate is then annealed at temperatures around 500 °C to 700 °C for a 24 to 48 hours period to ensure the complete crystallization of silicon [Özmen et al., 2014]. This crystallization technique allows the formation of polycrystalline silicon grains with size of 1-3 micrometers [Becker et al., 2013]. Besides that, films obtained with this method show significant inter grain defects [Huang et al., 2015] hence the SPC process is impracticable owing to the high temperatures.

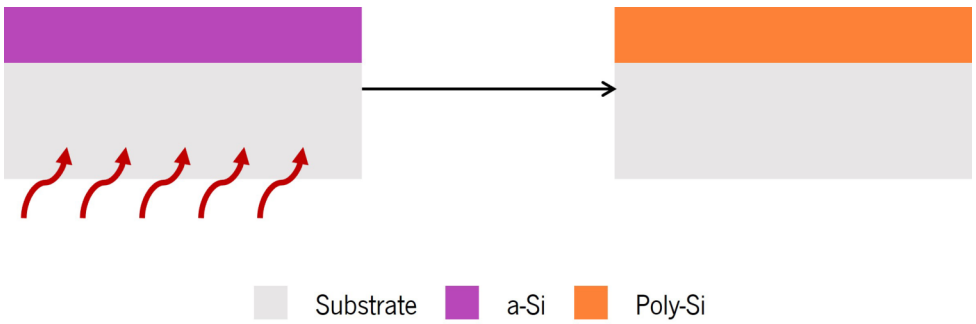


Figure 2.4: Schematic overview of Solid Phase Crystallization process.

Excimer Laser Annealing

Excimer Laser Annealing (ELA) is another possible approach for crystallizing amorphous silicon with a typical grain size around hundreds of nanometers [Chowdhury et al., 2020, Pier et al., 2008]. However, it is possible to find poly-Si films in the literature with grains as large as 2-3 micrometers [Duan et al., 2013, Kawamoto et al., 2006].

As shown in the illustration in Figure 2.5, a pulsed laser beam is focused in on the deposited Amorphous Silicon (a-Si) layer with a duration rate of around 10 Hz [Zhang et al., 2004].

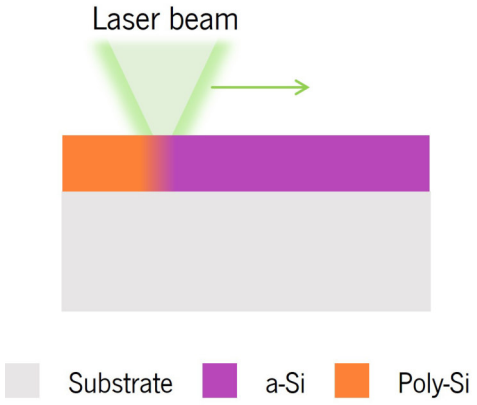


Figure 2.5: Schematic overview of Excimer Laser Annealing process.

This process is suitable for flexible substrates because the film melts rapidly and re-crystallizes with a polycrystalline structure while the substrate is kept cold. Additionally, compared to SPC, the derived poly-Si exhibits significantly fewer defects [Huang et al., 2015]. However, according to [Fortunato et al., 2000], this method can be expensive and is very reliant on the laser energy density.

Metal Induced Crystallization

The MIC crystallization process is a possible substitute for these methods. The procedure entails depositing a layer of crystalline metal on a substrate, followed by an additional layer of amorphous silicon. As seen in Figure 2.6, the previously amorphous silicon crystallizes as the metal layer rises to the top under thermal annealing. According to [Radnoczi et al., 1991], the deposited metal weakens the Si atom's bonds in this process, causing amorphous silicon to crystallize. This technique requires far less time and heat than SPC. A large group of metallic elements is capable of mediating the metal-induced crystallization process.

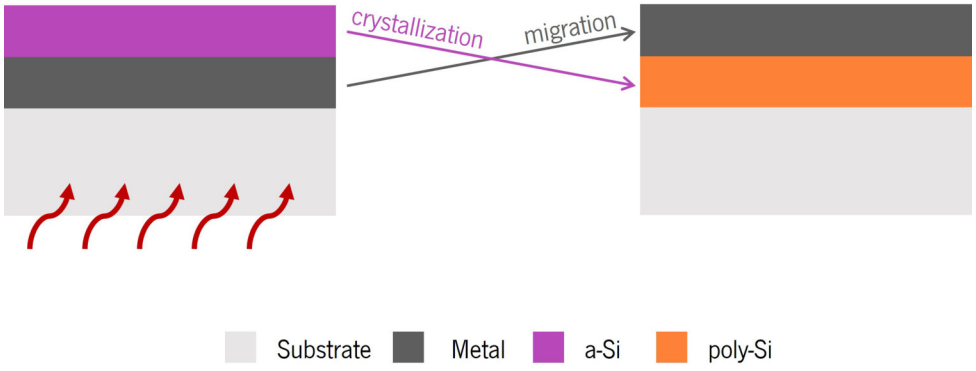


Figure 2.6: Schematic overview of Metal Induced Crystallization process.

Metals like nickel (Ni), copper (Cu) and palladium (Pd) mediate the crystallization of silicon by forming a stable silicide. According to [Hayzelden and Batstone, 1993], the driving force behind the crystallization of silicon is the reduction of free energy associated with the transformation of amorphous to crystalline silicon.

Consider the Ni/a-Si bilayer system depicted in Figure 2.7. The Si atoms initially react with the Ni layer, forming a silicide compound ($NiSi_2$). Since the chemical potential of Ni (μ_{Ni}) is lower than the chemical potential of Si (μ_{Si}) at the $NiSi_2$/a-Si interface, the formation of $NiSi_2$ is favorable. However, the opposite is true at the $NiSi_2$/poly-Si interface, which leads to the formation of polycrystalline silicon. The process repeats over time until there is no more amorphous silicon left.

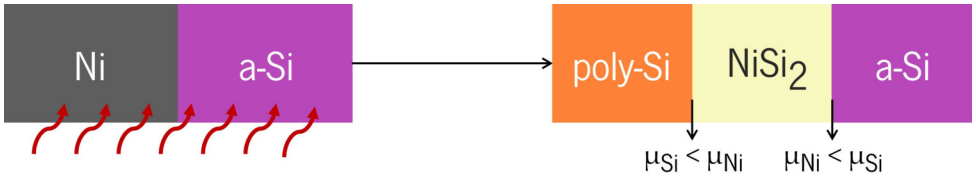


Figure 2.7: Schematic of Ni/Si bilayer system during MIC mediated by a silicide compound.

For MIC performed with aluminum (Al), silver (Ag) and gold (Au), a simple eutectic system[2] is formed where the metal acts like a catalyst. When the metal is in contact with a-Si, according to Hiraki's model [Hiraki, 1983], its free electrons perform an electronic screening of Coulomb interaction. This electronic screening turns the Si bonds unstable, facilitating their break.

Figure 2.8 illustrates the mechanism behind the process based on Nast and Wenham's model [Nast and Wenham, 2000]. In this assort of system, the silicon diffuses through the metallic layer until the solubility reaches its maximum value (Figure 2.8a). At that point, the diluted Si atoms start to nucleate with a polycrystalline structure (Figure 2.8.b) and finally a continuous poly-Si film is formed (Figure 2.8.c). This process occurs below the eutectic temperature, and its value depends on the metal used, as presented in Table 2.2.

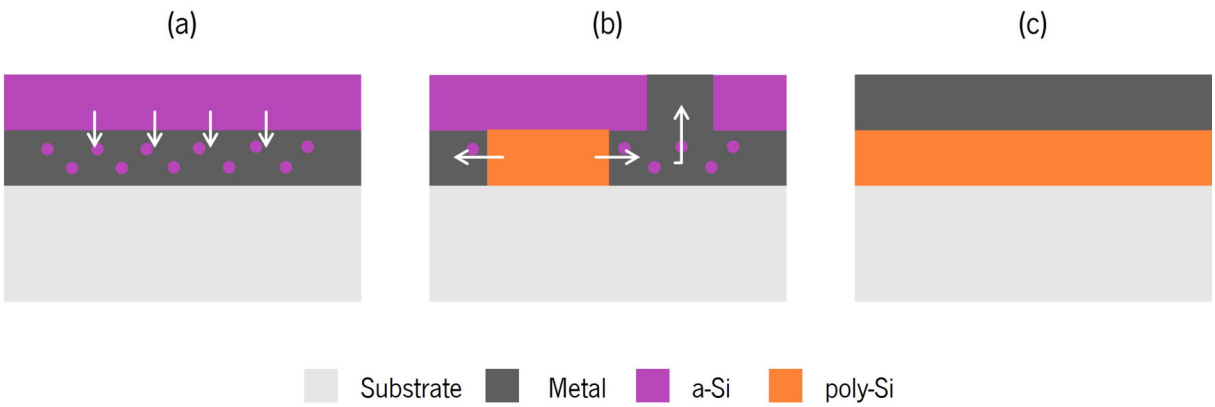


Figure 2.8: Schematic of bilayer system during MIC mediated by a non-silicide forming system.

The crystallization process occurs between 180 °C and 577 °C when aluminum serves as the catalyst metal. Because this temperature range is ideal for flexible substrates, the manufacturing approach advocated for this project is based on MIC with aluminum.

[2] **Eutectic system:** homogeneous mixture of different materials that solidifies or melts at a specific eutectic temperature. The eutectic temperature is lower than the fusion point of any substance in the system.

Table 2.2: Eutectic temperature (Te) and crystallization temperature (Tc) of various bilayer systems.

Type of system	Metal/a-Si	Te (°C)	Tc (°C)	Reference
Non-silicide forming	Al/a-Si	577	180	[Bosnell and Voisey, 1970]
	Au/a-Si	370	100	[Bosnell and Voisey, 1970]
	Ag/a-Si	830	300	[Bosnell and Voisey, 1970]
Silicide forming	Ni/a-Si	964	500	[Yoon et al., 1997]
	Cu/a-Si	802	485	[Russell et al., 1998]
	Pd/a-Si	760	500	[Lee et al., 1995]

2.4 Aluminum Induced Crystallization Process

The last section gave an overview of what happens when the bilayer system metal/a-Si is under thermal annealing. But a more profound explanation of why the layers exchange needs to be addressed.

2.4.1 Thermodynamics of AIC

The main driving force for the layer exchange is the reduction of Gibbs energy of the system, G. The Gibbs energy of a system is defined as the difference between the system's enthalpy, H and the product of temperature T times the system's entropy, S.

$$G = H - TS \tag{2.17}$$

During a reaction that occurs at a constant temperature, the change in the Gibbs energy is defined as (2.18).

$$\Delta G = \Delta H - T\Delta S \tag{2.18}$$

According to the second law of thermodynamics, if the Gibbs energy change is negative, $\Delta G < 0$, then a spontaneous reaction occurs. This happens because the system tends to minimize the free energy to the lowest value possible to reach an equilibrium state.

[He et al., 2006] stated that the Gibbs energy change, ΔG, of the AIC process is based on four contributions:

1. Crystallization of amorphous silicon (ΔG_1)
2. Relaxation of macrostress and microstrain of the Al layer (ΔG_2)

3. Surface energy difference between Al and a-Si (ΔG_3)

4. Interfacial energy difference between a-Si/Al and poly-Si/Al (ΔG_4)

The calculation of the numerical values for each ΔG has already been done in literature to specific systems, and the respective results are summarized on Table 2.3.

Table 2.3: Numerical values for Gibbs changes during the AIC process.

T [K]	ΔG_1 [J/m^2]	ΔG_2 [J/m^2]	ΔG_3 [J/m^2]	ΔG_4 [J/m^2]	Reference
523	−125.95	−0.53	0.15	0.22	[Zhao et al., 2004]
524	−121.46	−0.51	0.11	0.27	[He et al., 2005]

The principal contributor to the energy reduction is the transformation of silicon from amorphous to crystalline phase (ΔG_1). However, this phase change does not promote the layer exchange, only justifies why the previous amorphous silicon crystallizes. In fact, it is the release of strain and stress of the Al layer upon annealing that supplies the energy gain, benefiting the layer exchange since the Al atoms release this strain/stress by migrating to free spaces left by a-Si.

But these results are only valid for a specific temperature, raising the question of "what happens if the temperature increases or decreases?". He *et al.* studied the Gibbs energy change for a range of temperatures and found that, as the annealing temperature arises, ΔG_2 decreases even more, as illustrated on Figure 2.9. This suggests that the layers' interchange is more favorable at higher temperatures.

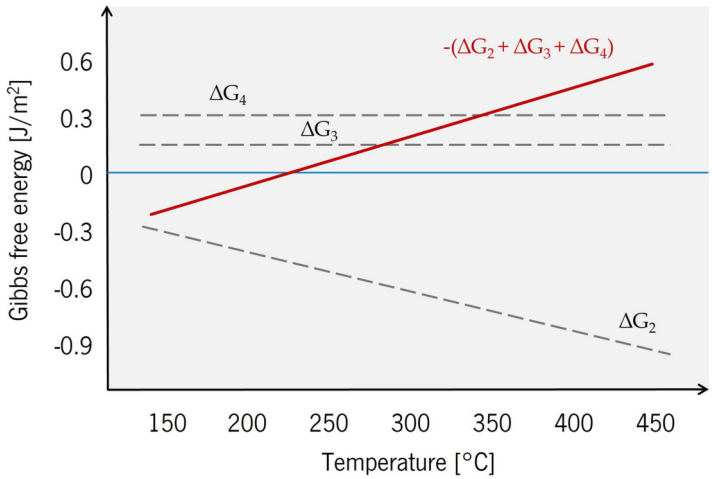


Figure 2.9: Gibbs free energy as a function of the annealing temperature. Adapted from [He et al., 2005].

This result adjudicates that some growth parameters, like temperature, influence the layer exchange, and their acknowledgment is vital for developing a good quality polycrystalline silicon film.

2.4.2 Influence of growth parameters

The physical parameters listed in Figure 2.10 significantly impact the crystallization of amorphous silicon. Variations in these parameters can boost layer exchange, but they also have an influence on the film's continuity and the corresponding grain size, allowing for fine-tuning of the polycrystalline film's piezoresistive behavior. In light of earlier studies on the subject, this section explores each parameter and how it affects the quality of the polysilicon film.

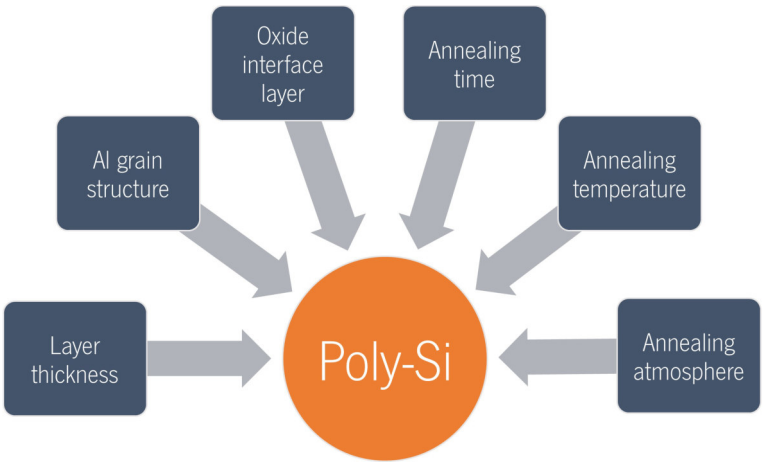


Figure 2.10: Parameters that influence the polysilicon morphology.

Layer thickness

The thickness of the a-Si and Al layers is crucial, since the process relies on these layers' interchange. [Nast and Wenham, 2000] experimentally demonstrated that the starting thickness of Al determines the final extent of poly-Si. Take into account the case where the bilayer system is Al(200nm)/a-Si(100nm), as shown in Figure 2.11a.

As the silicon atoms diffuse into the aluminum layer, the nucleation of these atoms leads to the formation of Si crystals with a 200 nm thickness (Figure 2.11b). This means that the a-Si deposited is not sufficient to produce a continuous poly-Si film after the aluminum etch (Figure 2.11c). Hereby, to develop a continuous polysilicon film, the ratio a-Si/Al must be, at least, equal to 1.

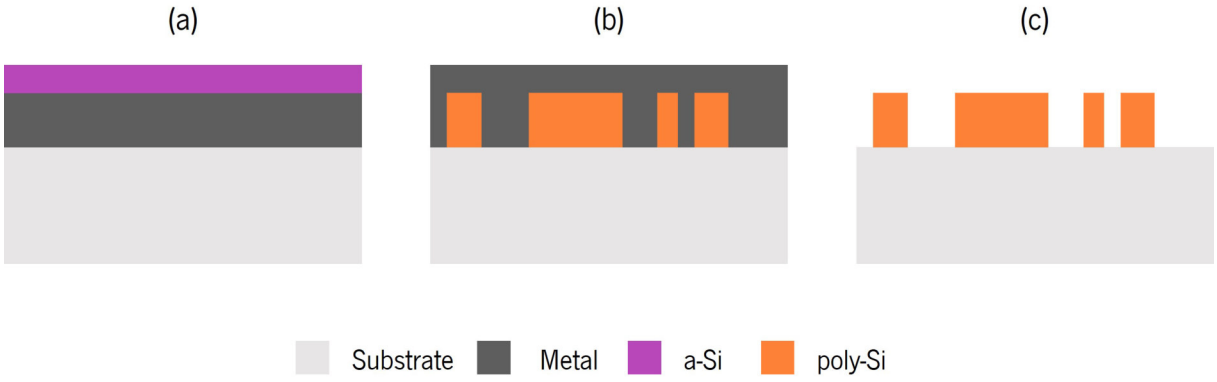


Figure 2.11: Schematic of bilayer system of AIC process for Al(200nm)/a-Si(100nm) bilayer system.

However, assuring that ratio is not sufficient. During the crystallization process, small silicon islands appear on top of the layer [Nast and Wenham, 2000, Tutashkonko and Usami, 2016] as illustrated in Figure 2.12. This means that part of the deposited a-Si is consumed on this secondary crystallization, and the ratio a-Si/Al must be higher than 1 to obtain a continuous film.

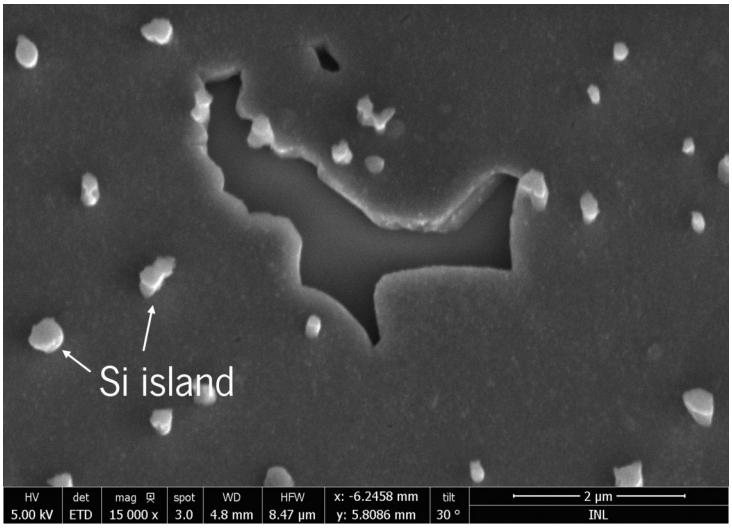


Figure 2.12: Tiled SEM picture of a poly-Si film with secondary crystallization.

Aluminum grain structure

Besides the aluminum layer thickness impact, the film's grain structure also affects the integrity of the crystallization process of a-Si. A study performed by Nast and Hartmann [Nast and Hartmann, 2000] states that for aluminum layers with smaller grains, the resultant polycrystalline silicon layer is composed of smaller grains.

This is as a result of Al grain boundaries being preferred nucleation sites. Smaller Al grains lead to

more grain boundaries, which is favorable to silicon diffusion, and the nucleation rate increases.

Since the nucleation rate is higher, the final Si grain will be smaller because the grains have less space to grow laterally.

Interface layer

After the deposition of the aluminum layer, as soon as the sample is exposed to air, an oxide layer starts to form. The process of crystallization is not indifferent to this layer. The oxide layer acts as a diffusion barrier for the Si atoms, which means that the presence of this oxide leads to a deceleration of nucleation, allowing the lateral growth of Si crystals [Nast and Hartmann, 2000].

However, since this layer constrains the silicon diffusion, the energy required to surpass this barrier is higher, meaning that higher temperatures are needed when compared to processes where there is no oxide layer.

Annealing time and temperature

After the Al and a-Si layers deposition, the sample is thermally annealed, and the layers exchange at this point. The annealing conditions significantly impact the final polysilicon layer, making this step critical. For instance, for a given temperature, as the annealing time increases, the Si grains grow further laterally, conceiving a continuous film.

The annealing temperature is an additional component to take into account since the nucleation rate rises along with the temperature. Because there are more growing grains, they are more closely packed, and their expansion is constrained, which causes a film of little grains to form [Nast et al., 2000]. Additionally, a greater nucleation rate results in a quicker surface coverage [Pihan et al., 2007].

Annealing atmosphere

Besides the effect of annealing time and temperature, the atmosphere where the annealing is performed also influences the polysilicon film morphology, as previously stated by [Dimova-Malinovska et al., 2006]. Comparing the films for three different atmospheres (N_2, N_2 + H_2, H_2), it was found that introducing H_2 into the annealing atmosphere composition leads to a smoother polysilicon film, and the grains are more packed which can be a great advantage to develop a continuous polysilicon film.

2.5 Summary

The present chapter showed that several materials exhibit piezoresistivity and can be used as sensing resistors. Metals like Au and Cu are easily deposited on flexible substrates, but their low gauge factor (GF) (< 5) is their main drawback. Semiconductors usually have substantially larger Gauge Factors due to changes in the material's resistivity and, consequently, are more common in piezoresistive devices.

From the set of materials studied, polycrystalline silicon shows to be a particularly interesting material for pressure sensing applications due to its high gauge factor. Even though this value inferior to monocrystalline silicon, it can be placed on different substrates.

This material can be directly deposited by CVD, but temperatures above 600 °C are required for obtaining a crystalline structure. Alternatively, different crystallization techniques have been employed as a way to obtain polycrystalline silicon from the amorphous phase such as Solid Phase Crystallization (SPC), Excimer Laser Annealing (ELA) and Metal Induced Crystallization (MIC).

Due to the high temperatures (500 - 700 °C) associated with the SPC process and the high cost involved in the ELA technique, the MIC procedure stands out as a viable approach to obtain poly-Si at temperatures as low as 180 °C when mediated by aluminum.

This crystallization process is influenced by some growth parameters that affect the structure of the polycrystalline silicon film. Figure 2.13 resumes which parameters must be altered for obtaining a continuous film and larger polycrystalline grains. It is possible to conclude that some of these variations may benefit one characteristic to the detriment of another, like the value of the annealing temperature and the thickness of the interface oxide layer. The impact of these factors will be discussed in more detail in the following chapter, along with the crystallization process's outcomes.

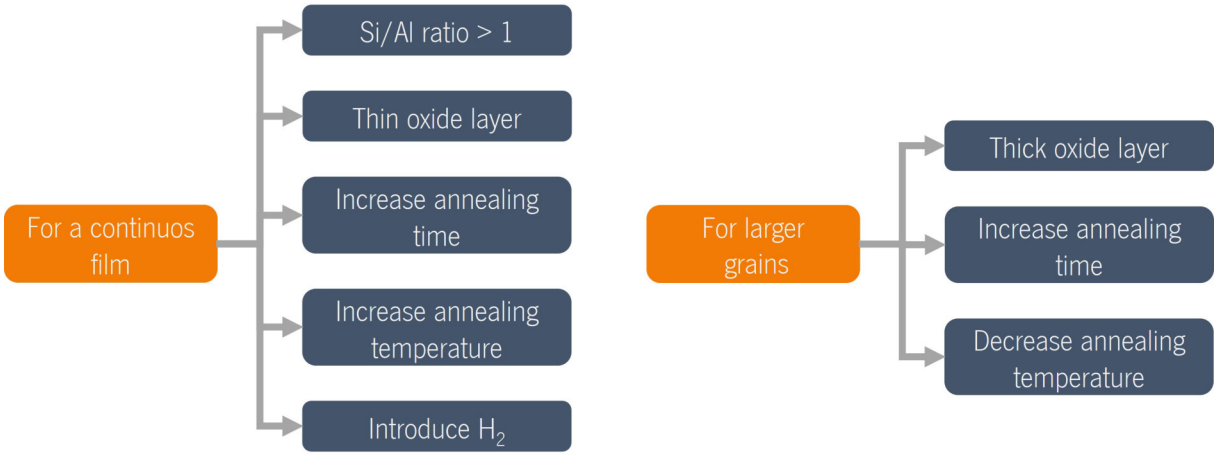


Figure 2.13: Summary of the impact of the growth parameters.

Piezoresistive material development

The current chapter presents the experimental procedures implemented to obtain a polycrystalline silicon film by the metal induced crystallization introduced in Chapter 2. A set of 14 different tests were conducted with the conditions explicit in the diagram of Figure 3.1. The tests of the crystallization process on top of a Si wafer are enumerated from T1 to T12 in chronological order of execution. The last test of this work was performed on top of a flexible layer of PI based on the best result obtained in the tests, this is the result of test 12.

The following sections provide a detailed description of the results of the tests and a justification for the decisions taken throughout the experiments.

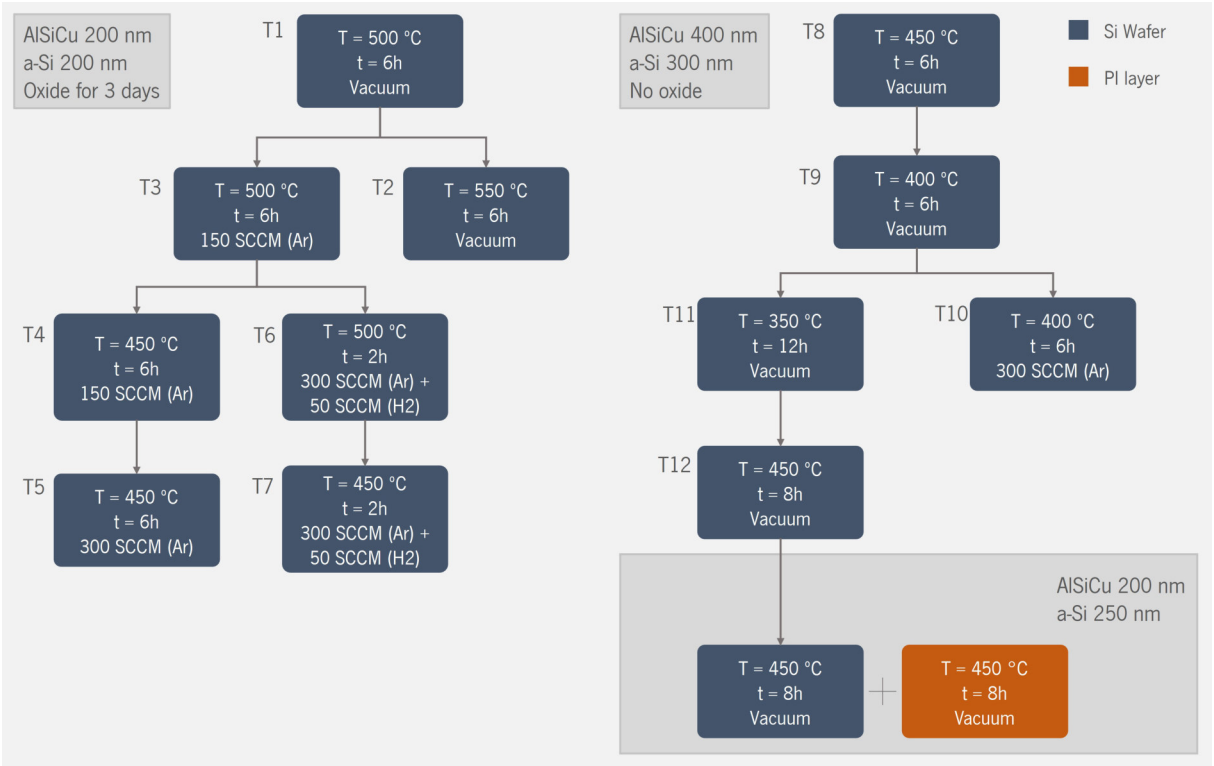


Figure 3.1: Diagram of the experimental tests conducted with the annealing conditions detailed for each test.

3.1 Materials and Methods

The metal-induced crystallization process requires the deposition of a metal and the subsequent deposition of amorphous silicon. This bilayer system goes to a thermal annealing treatment whose conditions can be adjusted. This section presents the materials and equipment used in this work, followed by the methods used to evaluate the quality of the poly-Si film.

3.1.1 Materials deposition

In this work, a single side polished (SSP) <100> p-type silicon wafer with a 724 µm thickness was used as the substrate. The wafer is passivated by depositing a 100 nm thick silicon dioxide (SiO_2) layer by Plasma Enhanced Chemical Vapor Deposition (PECVD) carried on a STPS MPX CVD equipment with a deposition rate of 46.7 nm per minute with the uniformity is shown in Figure 3.2.

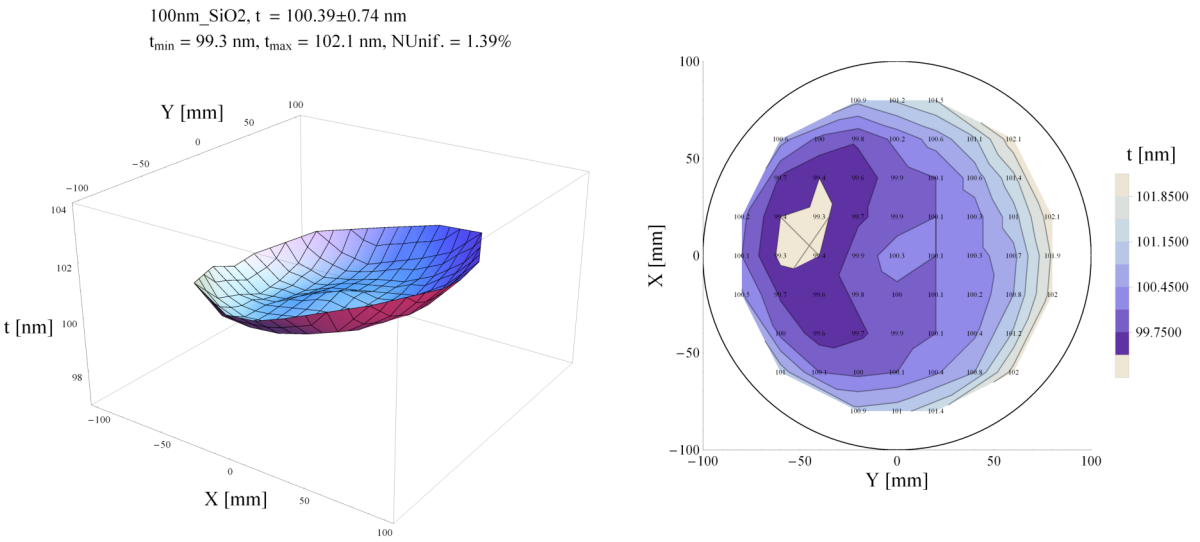


Figure 3.2: Mapping of the uniformity of the SiO_2 film deposited on a Si wafer with a target thickness of 100 nm.

Posterior to the electrical passivation step, the bilayer system composed by the catalyst metal and the amorphous silicon is assembled on top of the wafer with the following specifications:

- **Metal layer**: Posterior to the electrical passivation step, a layer of AlSiCu [1] was sputtered with an average deposition rate of 70 nm per minute using Timaris FTM PVD instrument to target thicknesses of 200 nm and 300 nm for different tests.

[1] **AlSiCu**: metallic alloy constituted by Aluminum, Silicon and Copper

A subset of samples was exposed to air for three days to form an aluminum oxide layer. In contrast, the remaining samples were in contact with air only during the transfer process between the deposition steps.

- **Amorphous silicon**: The last layer, namely the a-Si layer, was deposited by PECVD with an average deposition rate of 61.52 nm per minute with a thickness in the range of 200 nm to 400 nm.

It must be highlighted that pure aluminum was not used during the experiments, as the literature reports. This comes from the fact that AlSiCu is deposited at higher rates when compared to pure aluminum allowing the development of thicker layers without being too much time-consuming. Therefore, there is a great interest in incorporating this material into the current process. This is the first time, to the best of the author's knowledge, that this aluminum alloy has been employed in a metal induced crystallization process.

3.1.2 Thermal annealing

The thermal annealing process was tested at different temperatures, that ranged from 550 °C to 450 °C with distinct durations from 2 hours to 12 hours in a thermal CVD equipment (Roth and Rau MicroSys 400).

This heating process was mainly conducted in vacuum. However, a couple of tests were carried out using different atmospheres, consisting of argon (Ar) with a 150 SCCM to 300 SCCM flow and hydrogen (H_2) with a fixed flow of 50 SCCM.

Posterior to the thermal treatment, the remaining AlSiCu on the surface is removed by a wet etch process using a standard AlSiCu etching solution [2] at room temperature with ultrasound agitation. This step allows the further inspection of the newly formed poly-Si layer.

3.1.3 Inspection techniques

The quality of the polycrystalline silicon film asserted based on its continuity, the element constitution and the crystalline degree.

Scanning Electron Microscopy (SEM) allows the visual evaluation of the film's continuity. Figure 3.3 shows a picture of a polycrystalline layer. The region with a granulated appearance is the poly-Si film,

[2]Solution formed by 60-80 parts of phosphoric acid, 0-5 parts of nitric acid, 0-5 parts of acetic acid, and 0-10 parts of deionized water

whereas the darker areas are the holes in the film. The crystalline nature of the material is manifested by the geometrical boundaries of the film, typically associated with a crystalline structure. In the Scanning Electron Microscopy (SEM) picture is evidenced small clusters called Si islands deriving from secondary crystallization and residue of amorphous silicon not consumed.

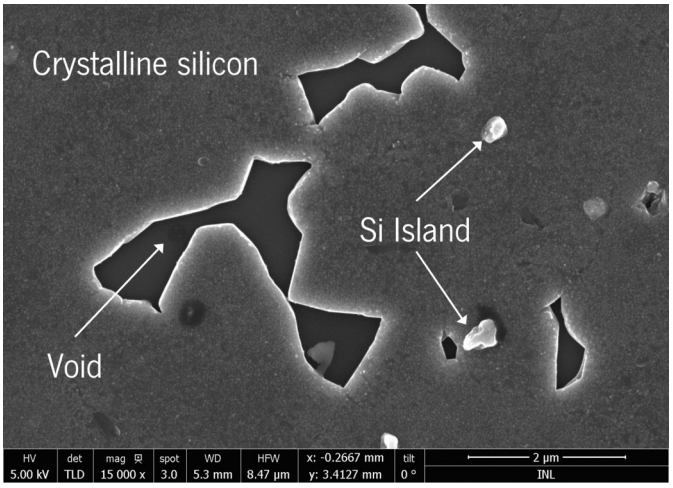


Figure 3.3: SEM picture of a polycrystalline silicon film with voids and Si islands.

The estimation of voids is performed in Python by the binary image processing method.

From the microscope images, a threshold is defined in terms of the image's brightness, allowing the binary classification of pixels, as Figure 3.4 exemplifies.

Pixels in the microscope image with a value below the threshold translate to a dark pixel in the Threshold plot. The pixels with a value above are classified as white.

This way, the voids are represented by dark pixels and the crystalline material by white pixels. The percentage of voids is calculated by the percentage of dark pixels in the Threshold plot.

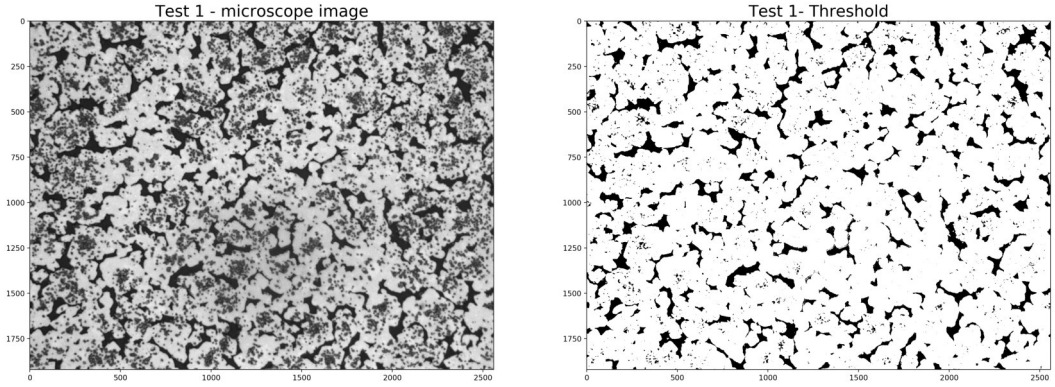


Figure 3.4: Result of the classification of voids by the binary image processing classification.

The material's element constitution is confirmed by the Energy-dispersive X-ray Spectroscopy (EDX) detector incorporated in the Nova Nano SEM equipment. Evaluating the material's constitution, only Silicon is expected to be detected. Suppose that Aluminum is one of the materials detected. In that case, the AlSiCu layer did not migrate entirely to the top, which means that the crystallization process was not completed.

The crystallinity degree of the material is evaluated by the X-ray Dispersion (XRD) technique carried out on XPERT Pro MRD. The XRD plots of crystals show peaks associated with the crystalline direction of the grains. If a material is in its amorphous state, then no peak is visible in the results. The grain size of the poly-Si is estimated using this method and will be explored further.

The polycrystalline nature of the film was analyzed using Backscattered Electron Detector (BSED).

3.2 Experimental results

The parameters imposed in each test are displayed in Table 3.1. This section provides a detailed description of the results of each test based on the characterization methods introduced in the last section.

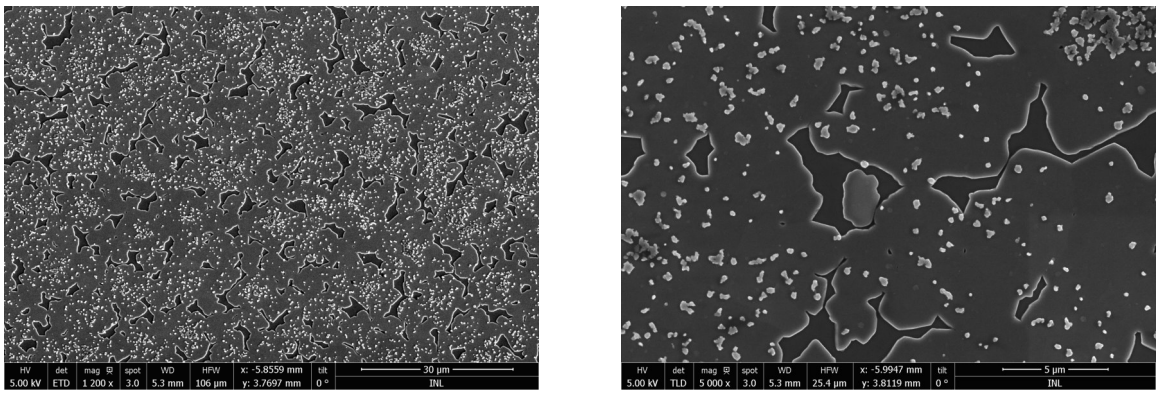
Table 3.1: Summary of conditions imposed in the metal induced crystallization process testing.

Test	AlSiCu [nm]	a-Si [nm]	Metal oxide layer	Temperature [°C]	Time [h]	Atmosphere [SCCM]	Figure
1	200	200	Present	500	6	Vacuum	3.5
2	200	200	Present	550	6	Vacuum	3.6
3	200	200	Present	500	6	Ar - 150	3.8
4	200	200	Present	450	6	Ar - 150	3.9
5	200	200	Present	450	6	Ar - 300	3.11
6	200	200	Present	500	2	Ar - 300; H_2 - 50	3.12
7	200	200	Present	450	2	Ar - 300; H_2 - 50	3.13
8	300	400	Absent	450	6	Vacuum	3.14
9	300	400	Absent	400	6	Vacuum	3.15
10	300	400	Absent	400	6	Ar - 300	3.16
11	300	400	Absent	350	12	Vacuum	3.17
12	300	400	Absent	450	8	Vacuum	3.18a

Test 1

The metal-induced crystallization process was validated by depositing the AlSiCu and a-Si layers with 200 nm thickness with intermediate oxidation for three days. The annealing conditions imposed for the first test consisted in heating the sample in vacuum up to a temperature of 500 °C for 6 hours.

In Figure 3.5 is depicted the SEM picture of the obtained crystalline silicon layer. The picture evidences that the film is not continuous and the voids represent about 13.93 % of the total area.

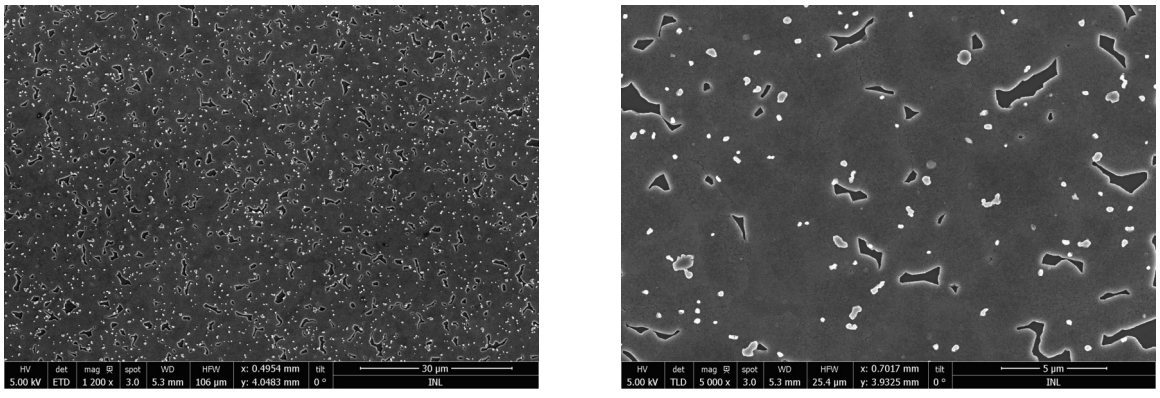


(a) (b)

Figure 3.5: SEM pictures of a poly-Si layer obtained by annealing at 500 °C for 6 hours in vacuum in (a) broad view and (b) close-up perspective.

Test 2

In a second iteration of the crystallization process, the temperature was risen 50 °C to reach an annealing temperature of 550 °C, and the obtained crystalline film is shown in Figure 3.6. In this case, the voids' percentage decreases to 3.68 %. This result validates the preposition that higher temperatures accelerate the crystallization process, providing a more continuous film when compared to crystallization performed at lower temperatures.

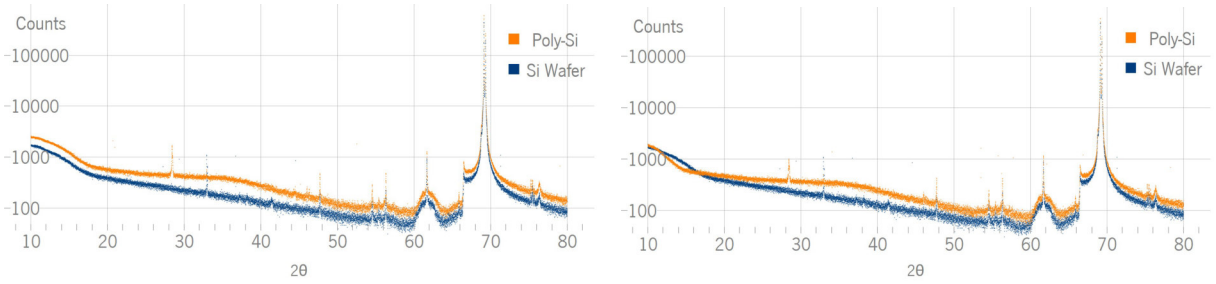


(a) (b)

Figure 3.6: SEM pictures of a poly-Si layer obtained by annealing at 550 °C for 6 hours in vacuum in (a) broad view and (b) close-up perspective.

However, the temperature not only influences the continuity of the film but also affects the grain size of the obtained crystals. To validate this claim, the previous samples were characterized using the XRD technique.

Figure 3.7a and 3.7b show the XRD results for the samples annealed at 500 °C and 550 °C, respectively.



(a) (b)

Figure 3.7: XRD results of the poly-Si layer of samples annealed in vacuum at (a) 500 °C and at (b) 550 °C.

Both figures show a peak associated with the direction $<111>$ at 2θ = 28.43 ° that is not present in the substrate plot. The diameter of the crystallites, D, associated to this peak can be estimated by the Scherrer equation, (3.1), where λ is the X-ray wavelength, β the full width at half maximum (FWHM) and θ is the Bragg angle.

$$D = \frac{0.9\lambda}{\beta \cos(\theta)} \tag{3.1}$$

With a β of 0.1285 ° for the sample annealed at 500 °C, the estimated crystallite size is 63.77 nm. As for the sample annealed at 550 °C, β is 0.105 ° which means that the crystallite's diameter is about 75.64 nm.

This result contradicts the results exhibited in previous works on the matter, where lower temperatures resulted in larger crystal grains [Nast et al., 2000]. This irregularity was already reported by Patil et al. [Patil et al., 2010] with the justification that in their work there is no oxide layer between the metal and the amorphous silicon films.

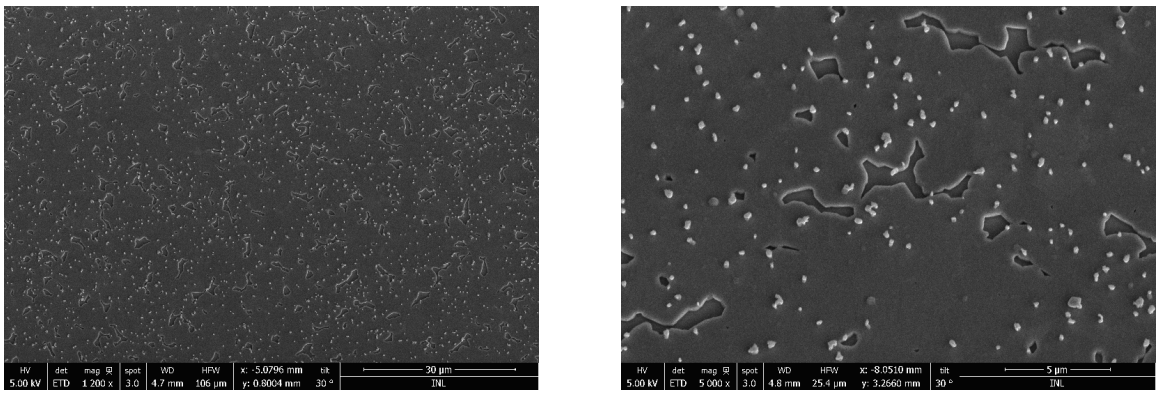
However, the samples analyzed in the current work were exposed to air for three days after the AlSiCu deposition, meaning that an oxide layer is indeed present. One plausible explanation is that, in the current case, the decrease in the nucleation rate associated with lower annealing temperatures is not enough to compensate the decrease in grain growth imposed by the temperature reduction.

3.2.1 Introduction of inert gases

Test 3

To study the influence of inert gases in the film's structure, in the third test the chamber was purged with Argon with a fixed flow of 150 SCCM. The temperature of the test was lowered to 500 °C and the duration was maintained at 6 hours. The poly-Si film derived from this annealing procedure is exhibited in the SEM picture of Figure 3.8.

The percentage of voids present in this film is about 4.64 %, a value much similar to the one obtained in the previous test in which the annealing temperature was 50 °C higher. This result concludes that introducing Argon to the annealing atmosphere provides a more continuous film. Since Argon is an inert gas, it does not react with the thin films, but the flow it provides to the annealing chamber allows the heat to spread, boosting the layer exchange process.



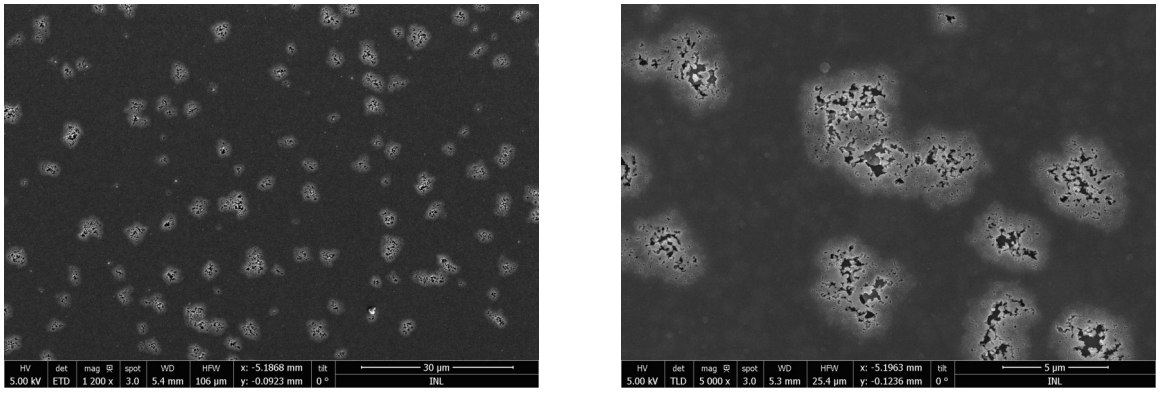
(a) (b)

Figure 3.8: SEM pictures of a poly-Si layer obtained by annealing at 500 °C for 6 hours in a chamber purged with 150 SCCM of Ar in (a) broad view and (b) close-up perspective.

Test 4

Given this outcome, in the subsequent test, the annealing temperature was reduced to 450 °C to study the possibility of obtaining a film with similar characteristics but at lower temperatures. As seen in Figure 3.9, this test did not turn out correctly. The crystallization process was ineffective since only a portion of the amorphous silicon diffused to the metallic layer.

The sample's composition was examined by EDX to demonstrate that the layer exchange procedure had not been entirely accomplished, and the results are shown in Figure 3.10.

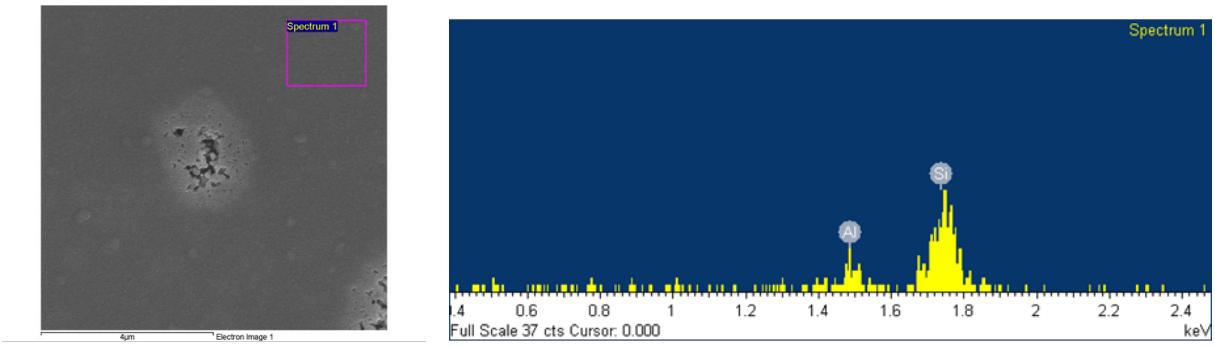


(a) (b)

Figure 3.9: SEM pictures of a poly-Si layer obtained by annealing at 450 °C for 6 hours in a chamber purged with 150 SCCM of Ar in (a) broad view and (b) close-up perspective.

The region under investigation is denoted by the rectangle in the SEM picture presented in Figure 3.10a and Figure 3.10b shows the corresponding energy spectrum.

This examination show that a significant amount of aluminum is still present in the sample, indicating that the metal did not migrate entirely to the surface, as predicted.



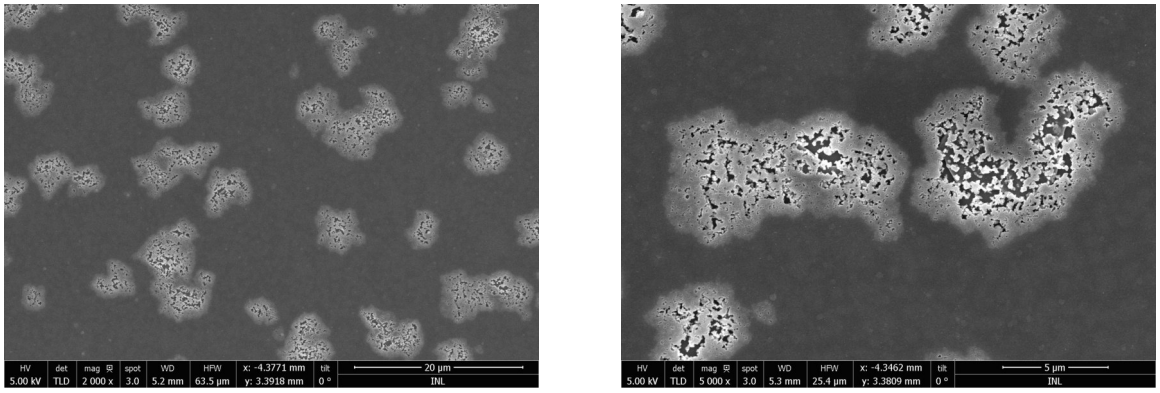
(a) (b)

Figure 3.10: (a) SEM picture and (b) EDX energy spectrum of the corresponding area.

This result lead to the conclusion that even though Argon is beneficial for the crystallization process, it is insufficient to promote the layer exchange at 450 °C in a 6 hour-period.

Test 5

As a consequence of this outcome, in the fifth test, the chamber was purged with 300 SCCM of Argon and the remaining conditions kept the same. The film structure obtained after the AlSiCu etch is shown in Figure 3.11. Similarly to the prior test, the layer exchange step is not satisfied, indicating that additional parameters need to be changed in order to obtain a totally crystalline silicon film.



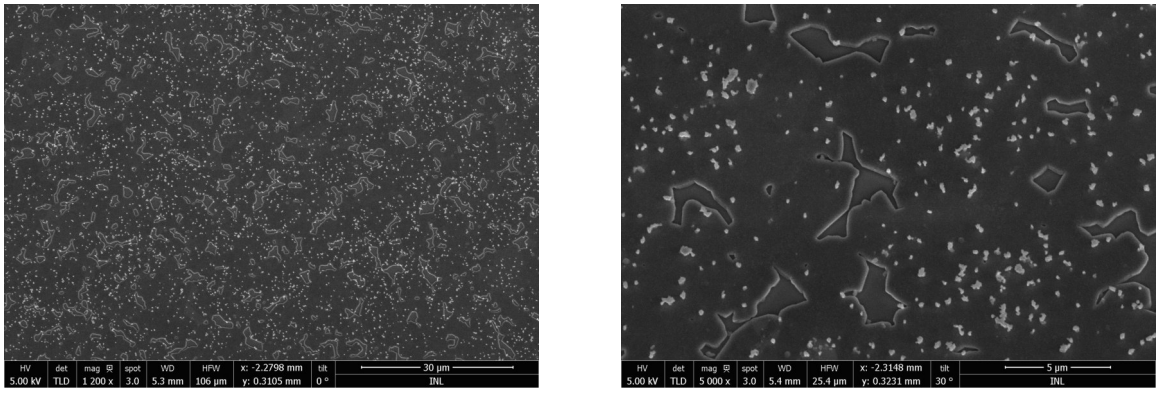
(a) (b)

Figure 3.11: SEM pictures of a poly-Si layer obtained by annealing at 450 °C for 6 hours with 300 SCCM of Argon in (a) broad view and (b) close-up perspective.

3.2.2 Introduction of Hydrogen

Test 6

Besides Argon, the possibility of using Hydrogen was studied as a way to form a continuous film. To validate this proposition, the same bilayer system previously used is annealed at 500 °C during 2 hours in an atmosphere consisting of 150 SCCM of Argon and 50 SCCM of H_2. The reduction of time between the tests comes from the fact that H_2 is a reactive gas and becomes insecure if there is a continuous flow without proper monitoring. The result of this test is presented in Figure 3.12 and shows a film with a continuity similar to the previous tests, but in a much shorter duration.



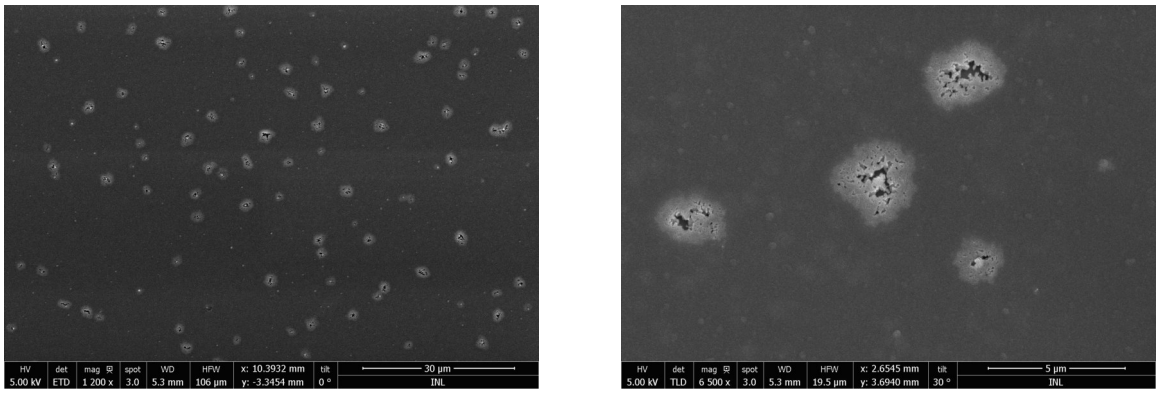
(a) (b)

Figure 3.12: SEM pictures of a poly-Si layer obtained by annealing at 500 °C for 2 hours in a chamber purged with Ar and H_2 in (a) broad view and (b) close-up perspective.

Test 7

The interest in temperature reduction lead to the next test in which the system AlSiCu/Oxide/a-Si was under thermal annealing at 450 °C while the other conditions were untouched. By observing the pictures of the obtained poly-Si in Figure 3.13 is it possible to conclude that the process is not completed.

Even though the presence of H_2 accelerates the crystallization process as predicted, the unsatisfying result at 450 °C means that higher temperatures and longer thermal treatments need to be imposed. However, due to the gas's security and supply limitations, it was impossible to proceed with this approach.



(a) (b)

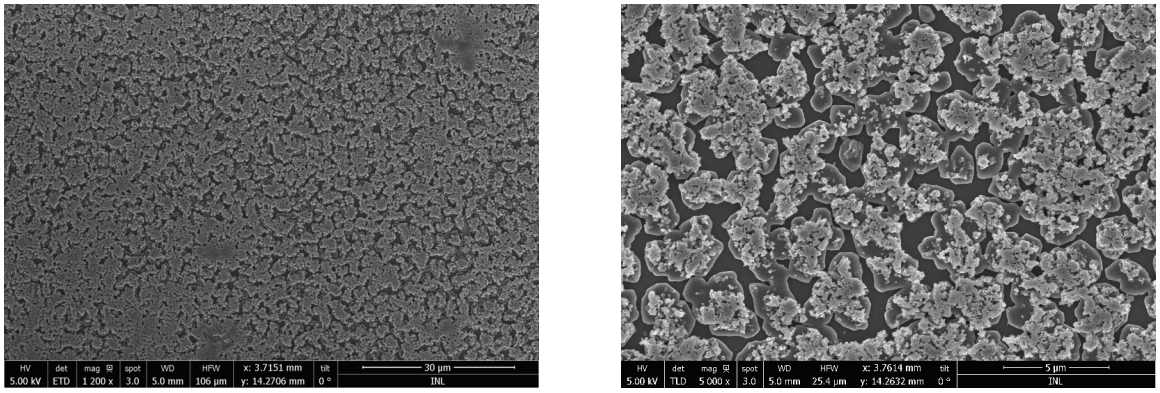
Figure 3.13: SEM pictures of a poly-Si layer obtained by annealing at 450 °C for 2 hours in a chamber purged with Ar and H_2 in (a) broad view and (b) close-up perspective.

3.2.3 Variation of layer thickness

In previous attempts, only the samples annealed at 500 °C or higher showed a complete silicon phase shift from amorphous to crystalline. This temperature remains too high for flexible substrates to withstand. Furthermore, the film could be more perfectly continuous in the cases when the technique was effective. As a result, in the following studies, the layers' system was created by first depositing 300 nm of AlSiCu, followed immediately by 400 nm of a-Si. The short exposure of AlSiCu to air precludes the formation of the metal oxide intermediate layer.

Test 8

This newly formed stack was annealed at 450 °C for a period of 6 hours in vacuum. These conditions allowed the formation of the crystals depicted in Figure 3.14.



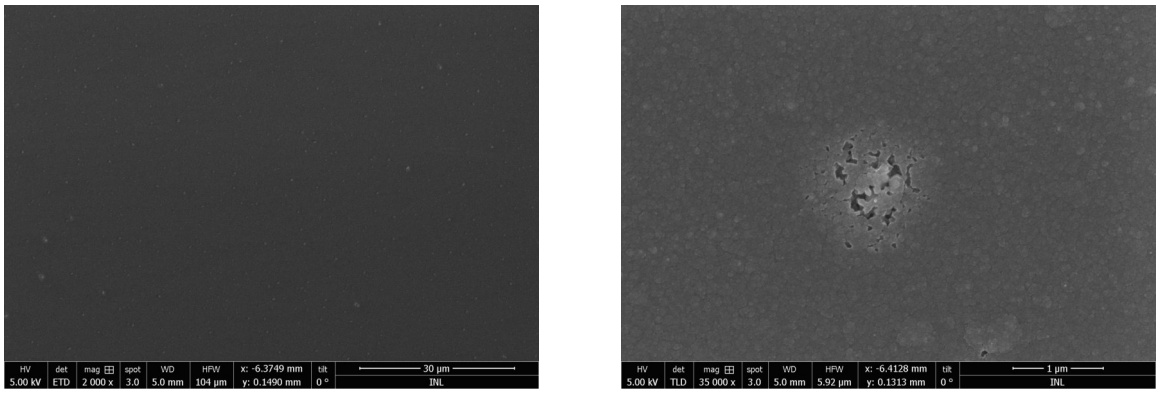
(a) (b)

Figure 3.14: SEM pictures of a poly-Si layer obtained by annealing at 450 °C for 6 hours in a chamber in vacuum in (a) broad view and (b) close-up perspective.

Although it is clear that the silicon and metallic layers exchanged positions, the crystals did not coalesce into a continuous film.

Test 9

To study the viability of using even lower temperatures, in the following test the annealing temperature was decreased to 400 °C while the remaining conditions were kept the same. The resultant film is shown in Figure 3.15 and evidences that the crystallization process was not successful.

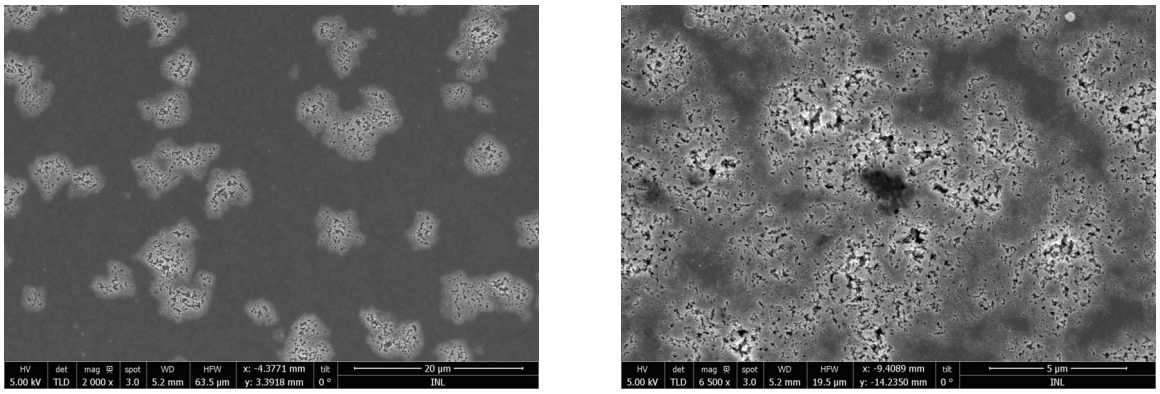


(a) (b)

Figure 3.15: SEM pictures of a poly-Si layer obtained by annealing at 400 °C for 6 hours in vacuum in (a) broad view and (b) close-up perspective.

Test 10

Based on the previous experiments with inert gases, a new test at 400 °C was conducted in which the annealing chamber was purged with 300 SCCM of Argon for 6 hours. The crystallization process was not properly performed, as it is possible to observe in Figure 3.16.



(a) (b)

Figure 3.16: SEM pictures of a poly-Si layer obtained by annealing at 500 °C for 6 hours in a chamber purged with 300 SCCM of Ar in (a) broad view and (b) close-up perspective.

3.2.4 Increase of annealing time

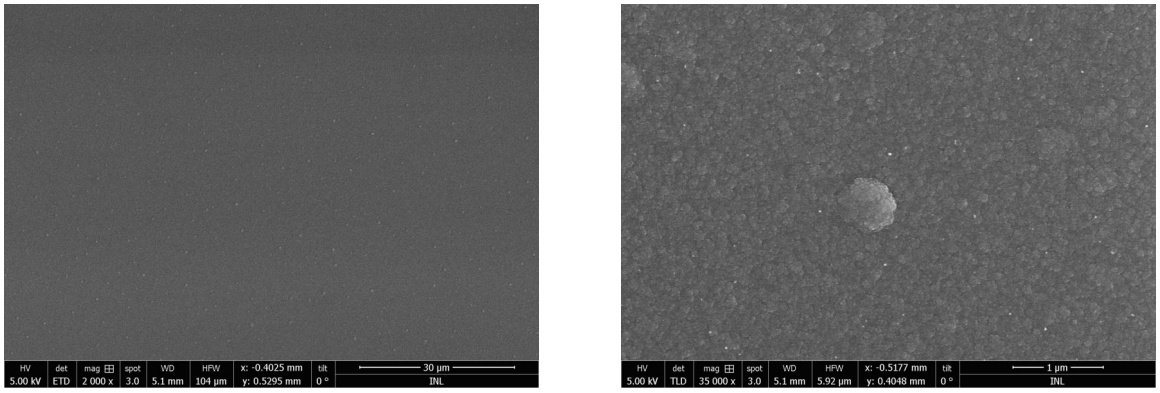
In prior testing, the majority of tests resulted in a poorly crystalline film with incomplete layer interchange. As previously mentioned in Chapter 2, the annealing time allows the crystal growth.

Test 11

This assertion led to the following test, in which the sample was annealed for 12 hours in vacuum at 350 °C. Even though the annealing time was twice as long as the previous tests, the 350 °C imposed were not sufficient to boost the crystallization process as seen in Figure 3.17.

Test 12

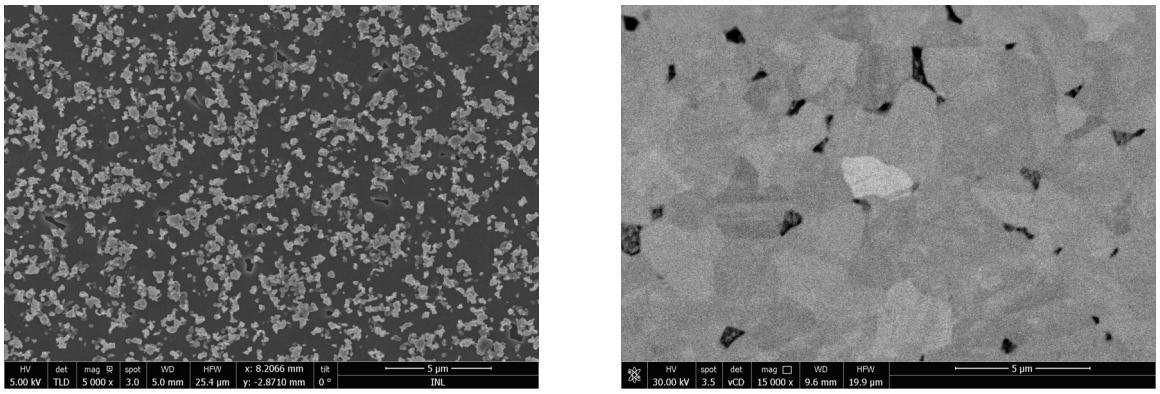
None of the tests performed below 450 °C was successful, prompting a change in the approach. In the next test, the annealing temperature rose back to 450 °C while the thermal treatment duration was extended to 8 hours in vacuum. The developed film is illustrated in Figure 3.18a.



(a) (b)

Figure 3.17: SEM pictures of a poly-Si layer obtained by annealing at 350 °C for 12 hours in vacuum in (a) broad view and (b) close-up perspective.

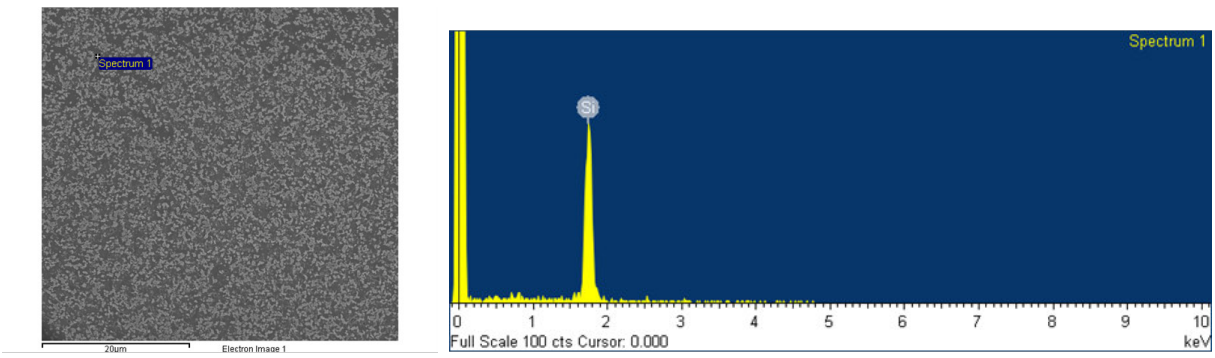
This test yielded the best results, since the amount of voids is inferior to previous tests. Figure 3.18b is captured with the BSED built within the SEM equipment (FEI QUANTA 650 FEG SEM) and displays varying tonalities related to crystals with different orientations, validating the polycrystalline nature of the produced silicon film.



(a) (b)

Figure 3.18: Polycrystalline silicon structure picture taken (a) by SEM and (b) BSED.

The sample's composition was also examined by EDX and the results are shown in Figure 3.19. The region under investigation is denoted by the point in the SEM picture presented in Figure 3.19a and Figure 3.19b shows the corresponding energy spectrum. The resultant spectrum evidences a sharp peak associated with Silicon and no peak associated with Aluminum is visible, which means that the content of Al in the obtained crystalline film is negligible.



(a) (b)

Figure 3.19: (a) SEM picture and (b) EDS energy spectrum of the corresponding area.

3.3 MIC on a flexible substrate

To validate the crystallization process on a polymeric substrate, a silicon wafer was used as carrier. The wafer was passivated by the deposition of a 100 nm thick SiO_2 layer by PECVD. The wafer was then subjected to a plasma activation process conducted in SPTS Pegasus for better adhesion of the polyimide. Subsequently, a layer of PI HD-4110 was spin coated on top of the wafer with a target thickness of 7 µm in a manual coater. The polyimide was put through a baking and developing process subdivided in the following steps:

- **Soft bake**: After the coating, the wafer went through a soft bake at 90 °C for a period of 180 seconds in a manual hotplate. The temperature of the hotplate was then increased to 110 °C where the wafer was heated for another 180 seconds. This soft bake allows the evaporation of residual solvents that might be present and improves the adherence of the polymer to the wafer surface.

- **Exposure**: The used polyimide is photosensitive, which means that it can be patterned by light exposure. The wafer covered with polyimide was exposed to UV-light using Karl Suss MA6BA6 in which a wafer cut in half was used as hard mask. The photoreaction occurs in the side exposed to the UV radiation, whereas the protected side remained intact.

- **Post-exposure bake**: Following the exposure step, the wafer was baked at 80 °C for 60 seconds. This post bake fulfills the exposure process, hardening the side previously exposed to the UV radiation.

- **Development**: After baking the polyimide, the undeveloped polyimide needs to be removed. This

is accomplished using a developer inserted in a manual coater.

- **Post-develop bake**: Following the development step, the wafer goes through another baking process in the manual hotplate at a temperature of 150 °C for 120 seconds. This baking process improves the chemical and physical stability of the polyimide.
- **Curing**: The polyimide is finally cured in an oven at 250 °C for 14 hours.
- **Post Degassing bake**: An additional post degassing bake at 350 °C in a manual hotplate was imposed in an attempt to evaporate the remaining gases trapped in the polyimide. The obtained polyimide layer on half of the wafer is depicted in Figure 3.20

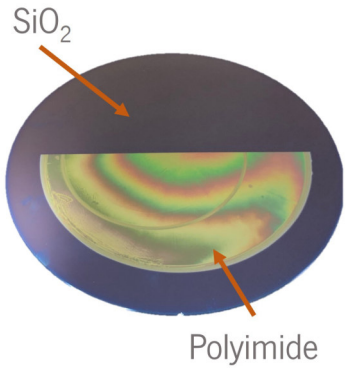


Figure 3.20: Photography taken of the wafer after patterning the polyimide.

Ensuing this step (Figure 3.21a), the AlSiCu layer was deposited with a target thickness of 200 nm, followed immediately by the deposition of a 250 nm thick a-Si layer (Figure 3.21b and 3.21c). The thicknesses of each layer were reduced to evaluate if thinner films provided an improvement in the crystallization process.

The wafer was diced in 4 cm × 4 cm square samples, creating a subset of samples with a stack formed by Si/SiO2/PI/AlSiCu/a-Si and another subset with the layer sequence Si/SiO2/AlSiCu/a-Si (Figure 3.21d). This allowed to perform the crystallization tests on the samples with the substrate covered with polyimide whereas the samples without the polymeric layer served for control. The samples from each set were annealed in vacuum at 450 °C during 8 hours (Figure 3.21e) and the remaining AlSiCu was wet etched (Figure 3.21f).

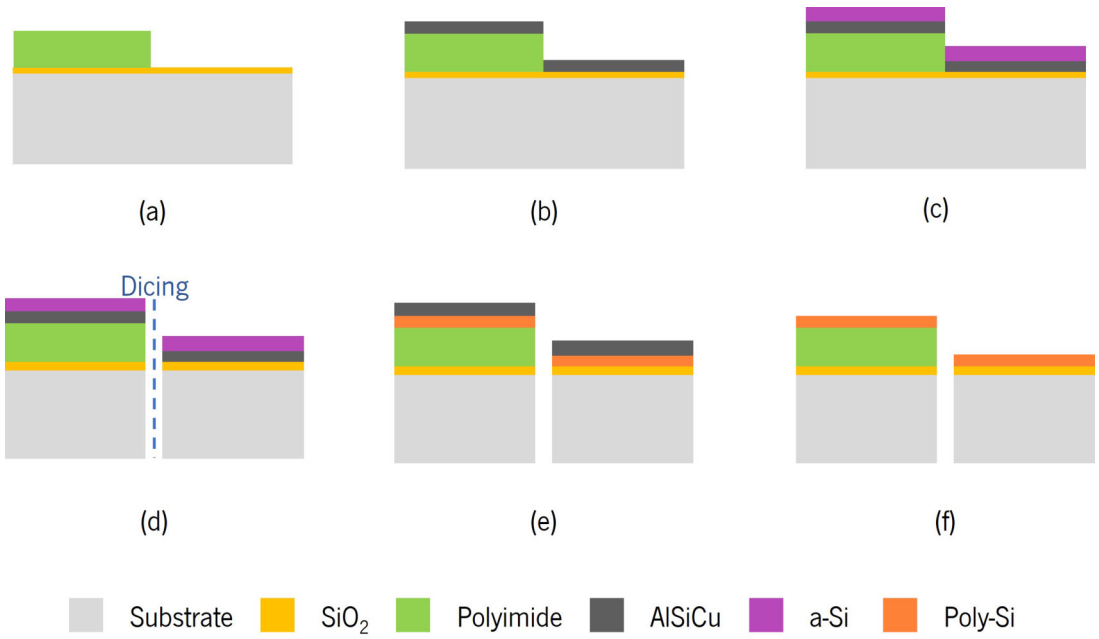
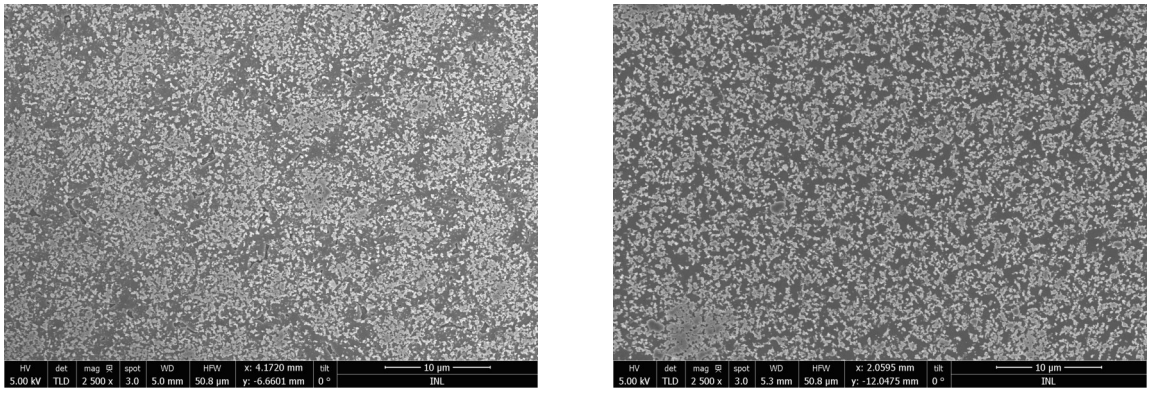


Figure 3.21: Schematic of the flow chart of the polycrystalline silicon fabrication on a flexible substrate.

The crystalline films resultant from the annealing treatment for the different samples is depicted in Figure 3.22. The poly-Si shown in Figure 3.22a is derived from the sample with the PI layer and has a structure similar to the one observed for the sample without that layer shown in Figure 3.22b, which means that the presence of the polymeric layer does not affect the final structure of the polycrystalline silicon film, which means that the process is conceivable in flexible substrates.

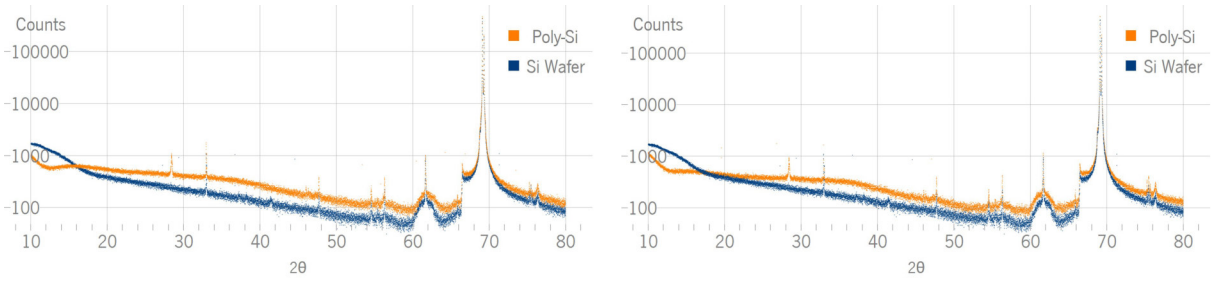


(a) (b)

Figure 3.22: SEM pictures of a poly-Si layer obtained by on top of (a) polyimide and (b) $Si0_2$.

The same samples were analyzed by the X-ray Dispersion (XRD) technique whose results are depicted in Figure 3.23. The plot derived from the inspection of the sample with the PI layer (Figure 3.23a) shows a peak at 2θ = 28.43 ° that is related to the $<111>$ direction. The FWHM of this peak is 0.142191

from a Gaussian approximation. From the Scherrer equation introduced in (3.1), the crystallite diameter is about 57.63 nm. When analyzing the resultant spectrum from the sample without the polymeric layer, there is also a peak at 2θ = 28.43 ° whose FWHM is 0.141392. This means that the crystallites of the film have an estimated diameter of 57.96 nm. The crystals from the different samples have an identical size, which reinforces the viability of using polymeric substrates in the MIC process.



(a) (b)

Figure 3.23: XRD results of the poly-Si layer obtained on top of (a) polyimide and (b) SiO_2.

The main defect of the MIC process in samples with the stack Si/SiO_2/PI/AlSiCu/a-Si is that after the annealing treatment, the polymeric layer suffered small bursts as shown in Figure 3.24. The bubble burst in the film incites that some gases were still trapped in the polyimide. One plausible explanation to this occurrence is that even though the sample was subjected to a post baking step, the amount of time that it was lead exposed to air allowed the rehydration of the polyimide, or even degassing of solvents that were not evaporating during the curing process resulting in the film fracture during the thermal annealing treatment.

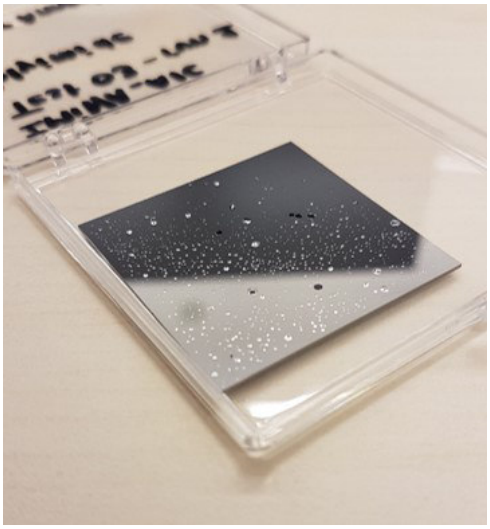


Figure 3.24: Photography taken of the sample after the annealing process showing fractures.

3.4 Key-findings

This chapter presented the experimental process behind the development of polycrystalline silicon. The route implemented in these tests consisted of the deposition of AlSiCu as the crystallization mediator and amorphous silicon. To examine how the structure affected the crystallization process, the thickness of these layers was adjusted from 200 nm to 400 nm in different ratios.

The system created by these thin films was thermally annealed for 2 to 12 hours at temperatures ranging from 350 °C to 550 °C. The annealing chamber's environment was changed during the experiments; some were conducted in a vacuum, while others included purging the chamber with hydrogen, argon or both.

During the experiments, it was validated that higher annealing temperatures lead to a faster crystallization process and consequently a more continuous crystalline film. However, in contrast to the literature review, higher temperatures do not promote the crystal growth. The XRD analysis of films annealed at 500 °C and 450 °C showed that the latter was formed by smaller crystallites. This may occur because in this process, the decrease of the nucleation rate associated with lower annealing temperatures is not enough to compensate the decrease in grain growth imposed by the temperature reduction.

The annealing atmosphere also has a significant impact on the crystallization process. It was discovered that when the chamber was purged with Argon during experiments, the resulting film could be annealed 50 °C less and retain its properties. The Hydrogen experiments showed that the crystallization process is substantially accelerated, but they could not create a continuous crystalline film in a 2-hour time period, making this strategy impracticable due to supply limitations.

One way to reduce the crystallization time required to obtain a crystalline film is by preventing the oxidation of AlSiCu since during the experiments it was proven that the presence of this oxide layer retards the crystallization process.

The set of tests performed allowed the achievement of a continuous polycrystalline silicon film by depositing 200 nm of AlSiCu immediately followed by 250 nm of a-Si, and the system must be annealed at 450 °C for 8 hours in vacuum.

The same system was implemented on top of a polymeric layer of PI HD-4110 and the obtained poly-Si film shows a structure equivalent to the one obtained without that layer. This finding suggests that the metal-induced crystallization process is conceivable on flexible substrates.

The test devices containing the created poly-Si will be discussed in the next chapters, along with the electrical behavior of the piezoresistive film.

Test devices

Last chapter presented the experimental procedures implemented to obtain polycrystalline silicon by metal-induced crystallization using AlSiCu as catalyst. The structure of this film was analyzed via SEM and XRD techniques, but a more profound study of the electrical behavior of the poly-Si is still required.

This chapter provides details about the test structures used for further electrical characterization from design to the fabrication process.

4.1 Chip design

The piezoresistive characterization of the poly-Si film developed comprises the Gauge Factor (GF) extraction. In section 2.1 it is stated that the piezoresistive coefficients can have distinct values depending on whether the piezoresistive film is preferentially oriented or not. To better understand this event, consider the piezoresistor placed at an arbitrary angle φ with respect to the applied stress direction, illustrated on Figure 4.1.

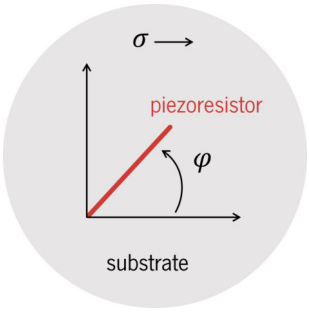


Figure 4.1: Illustration of the positioning of a piezoresistor bar subjected to a unidirectional stress.

The resistance change of the piezoresistor is given by (4.1) according to the model presented by [Bossche and Mollinger, 1997].

$$\frac{\Delta R}{R} = \sigma \left(\pi_l \cos^2 \varphi + \pi_t \sin^2 \varphi - \pi_{lt} \cos \varphi \sin \varphi \right) \tag{4.1}$$

The piezoresistive coefficients can be calculated by measuring the resistance change of three differently oriented piezoresistors while unidirectional stress is applied evenly. For an easier isolation of the piezoresistive coefficients, the test structure was designed to contain three piezoresistors oriented at 0 °, 90 ° and 135 ° as depicted in Figure 4.2. This leads to resistance values described by (4.2).

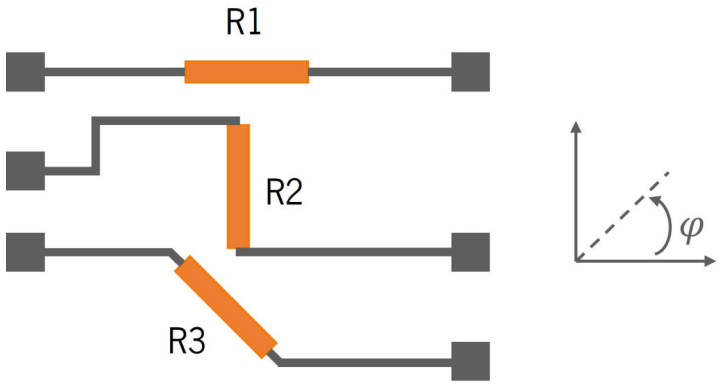


Figure 4.2: Illustration of the positioning of the resistors in the designed chip.

$$\frac{\Delta R1}{R1} = \sigma \cdot \pi_l$$

$$\frac{\Delta R2}{R2} = \sigma \cdot \pi_t \tag{4.2}$$

$$\frac{\Delta R3}{R3} = \frac{\sigma}{2} \cdot (\pi_l + \pi_t - \pi_{lt})$$

In order to apply an unidirectional stress to the devices and therefore extract their piezoresistive behavior, a four point bending fixture is used, based on [Lenci et al., 2008].

Consider a chip with a length l, width w and a thickness t where the piezoresistors are positioned, represented in Figure 4.3.

The bending set-up proposed is based on the ASTM E855-08 protocol, in which four similar cylindrical structures are positioned symmetrically to the center of the chip. Two of those beams act as support beams where the chip is laid, whereas the other two, called load beams, are subjected to an external force. According to the same protocol, the internal beams must be at a distance equivalent to 2/3 of the distance L between the external beams.

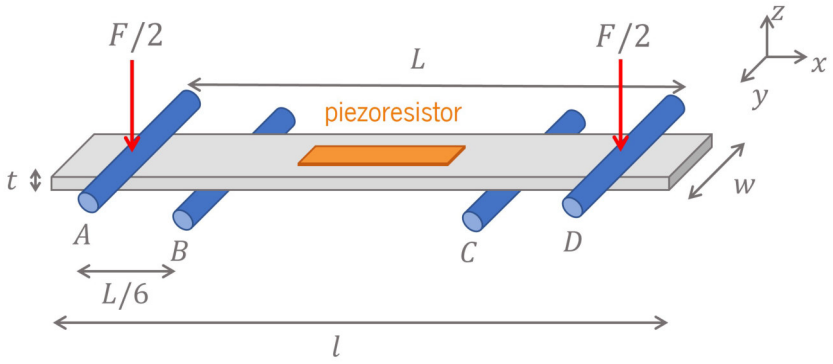


Figure 4.3: Illustration of a four point bending set up.

In this fixture, the stress applied between the support beams is given by[1]:

$$\sigma = \frac{FL}{2wt^2} \tag{4.3}$$

From the Hooke's Law (see Equation 2.3), the strain is given by:

$$\epsilon = \frac{\sigma}{Y} = \frac{FL}{2Ywt^2} \tag{4.4}$$

To validate the implementation of this setup, the structure was studied by the Finite Element Method (FEM).

The structural design of the system was executed in SpaceClaim. The conditions imposed are here stated and illustrated in Figure 4.4:

- Width, w: 10 mm
- Length, l: 30 cm
- Thickness, t: 0.725 mm
- Load beams: Parallel half cylinders with radius, $r = 1$ mm and length $l = 10$ mm. They are at a distance of 7.5 mm to the center in the x-direction.
- Support: Defined by two parallel lines at a distance of 5 mm to the center in the x-direction.

[1]This expression is derivated in Appendix A

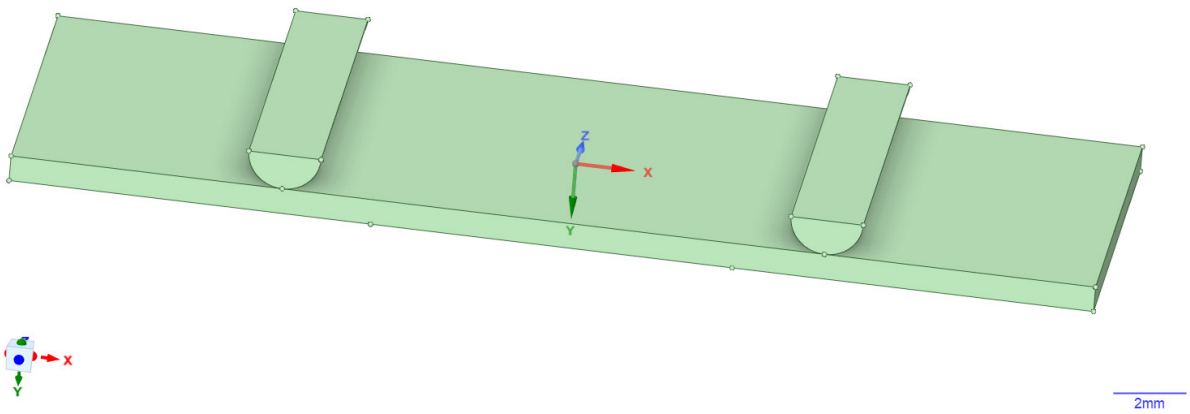


Figure 4.4: CAD model of the device with the load beams displayed as half cylinders.

The structural behavior of the model is studied using Ansys 2022 R2. When a force F = 10 N is applied to the set-up, the resultant normal stress in the x-direction is demonstrated in Figure 4.5. The color scheme evidences a maximum value in the mid-section region, as expected.

From (4.3), for a force of 10 N, it is expected a stress $\sigma = 1.43 \cdot 10^7 N/m^2$. The annotation showed in the graph declares a stress $\sigma = 1.56 \cdot 10^7 N/m^2$, a value similar to the theoretical prediction with a 9 % error.

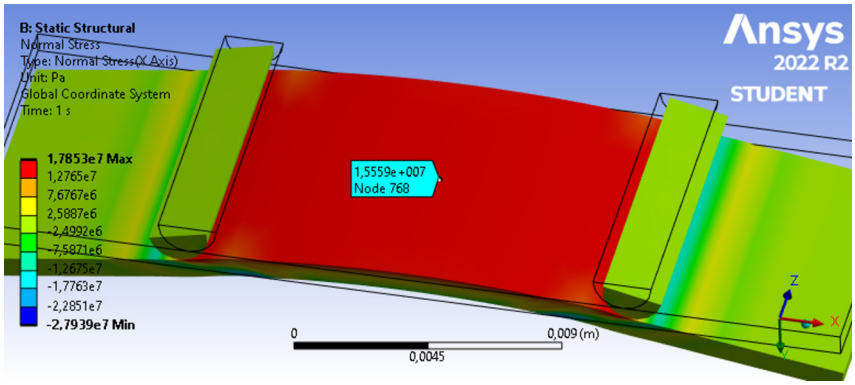


Figure 4.5: Normal stress distribution along the x-axis for a force F = 10 N.

It was previously said that this fixture allows the application of a unidirectional stress, which implies that the stress in the remaining directions must be close to zero. Figure 4.6 shows the obtained stress in the z and y-direction for the same conditions previously imposed. The annotation evidences a stress value much greater than zero for both cases, however, this values represent about 0.5% for the z-axis and 0.3% for the y-axis, which means that these stresses do not have a considerable impact in the total stress.

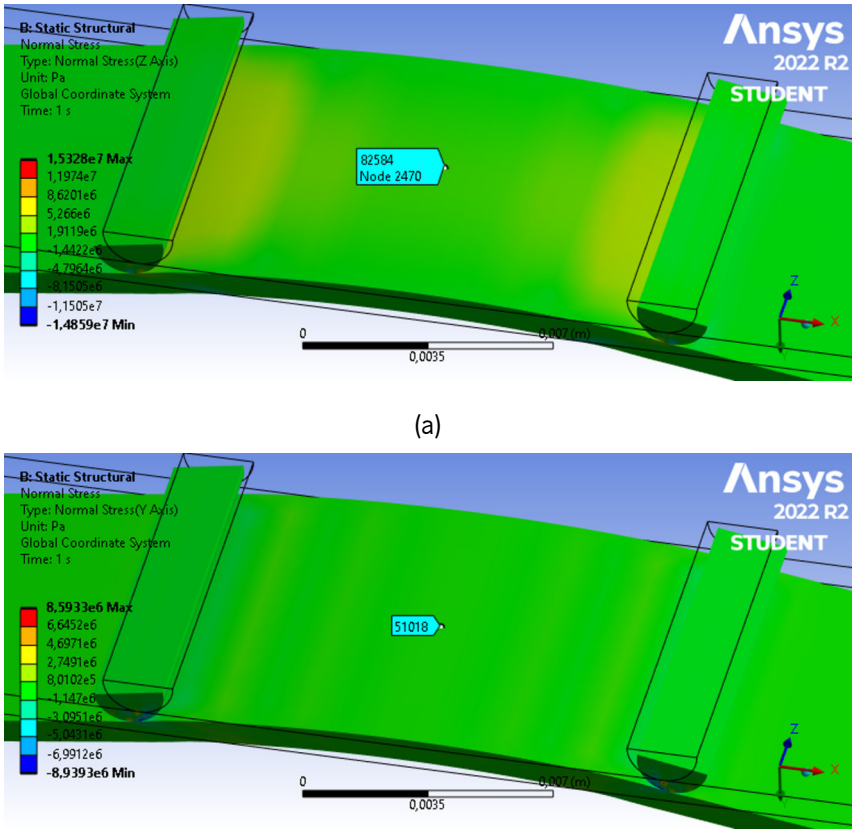


Figure 4.6: Normal stress distribution along the (a) z-axis and (b) y-axis for a force F = 10 N.

4.2 Piezoresistors fabrication

In order to dimension the resistors, the sheet resistance (R_s) of the poly-Si from Test 12 (see subsection 3.2.4) was used for the estimation of the electrical resistance of the designed resistors. This was measured in a four point probe system (AITCO CMT-SR2000N) and the results are depicted in graph of Figure 4.7 for arbitrary coordinates in the sample.

The mean value of these measurements is given by 3084.30 Ω/sq. Since the film has a thickness of 300 nm, the film resistivity is derived as:

$$\rho = R_s \cdot t = 3084.3\ \Omega/sq \cdot 0.3\ \mu m = 925.29\ \Omega \cdot \mu m \tag{4.5}$$

Since the piezoresistive behaviour of the piezoresistors is still unknown at this point, the length per width (L/w) ratio of the components was varied between 5, 10 and 20. Higher ratios are preferred due to better confinement of the stress orientation. However, the electrical resistance of resistors with smaller L/w ratios will also be lower, which can facilitate the resistance measurements.

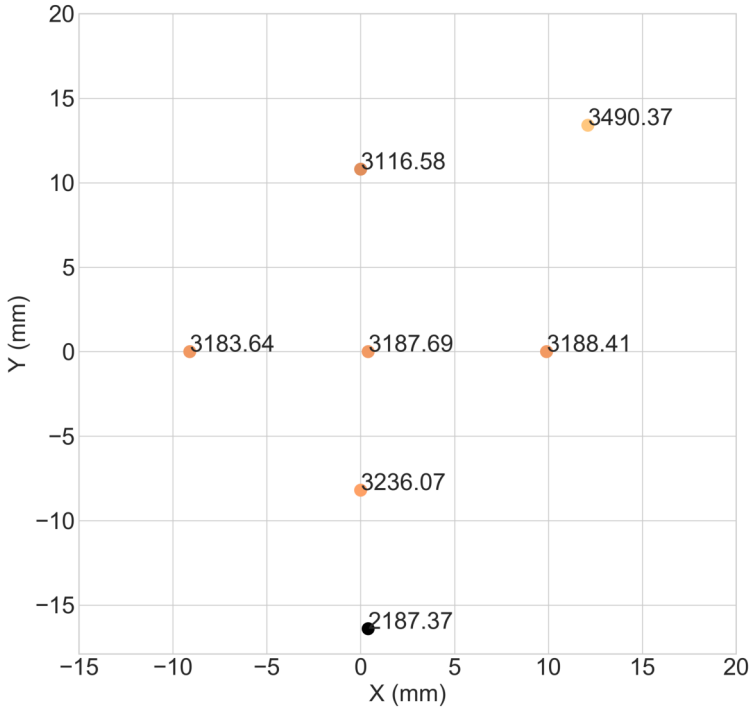


Figure 4.7: Graphic showing the sheet resistance (Ω/sq) of the film obtained in test number 12.

Based on this approach, three different chips were designed to have a width of 100 μm while the length was varied between 500 μm, 1000 μm and 2000 μm.

As for the height of the resistors, this value is imposed by the thickness of the a-Si and AlSiCu layers used in the crystallization process. For this chip fabrication, the estimation is based on the results of the crystallization process explored in Chapter 3 where the film developed in test number 12 has a thickness of 300 nm.

Knowing that the electrical resistance is given by $R = \rho l/A$ as introduced in (2.6), the estimated value for the designed piezoresistors is summarized in Table 4.1.

Table 4.1: Estimated electrical resistance for different piezoresistors based on their dimension.

Width [μm]	Length [μm]	Thickness [μm]	Resistance [$k\Omega$]
100	500	0.3	15.42
100	1000	0.3	30.84
100	2000	0.3	61.69

4.2.1 Electrical connections

Each resistor must be connected to a conductive path that allows the input of electrical signals and measurements. So, each resistor is linked to a contact pad by a Al conductive channel with a width of 200 μm as shown in Figure 4.8.

The resistor oriented at 0 ° is connected to two extra pads, so it is possible to insert a current signal if needed. It is expected that the resistance of the components can be measured using a simple ohmmeter, but if not, the extra pads will serve as input channel while the exterior pads will be used for output measurements.

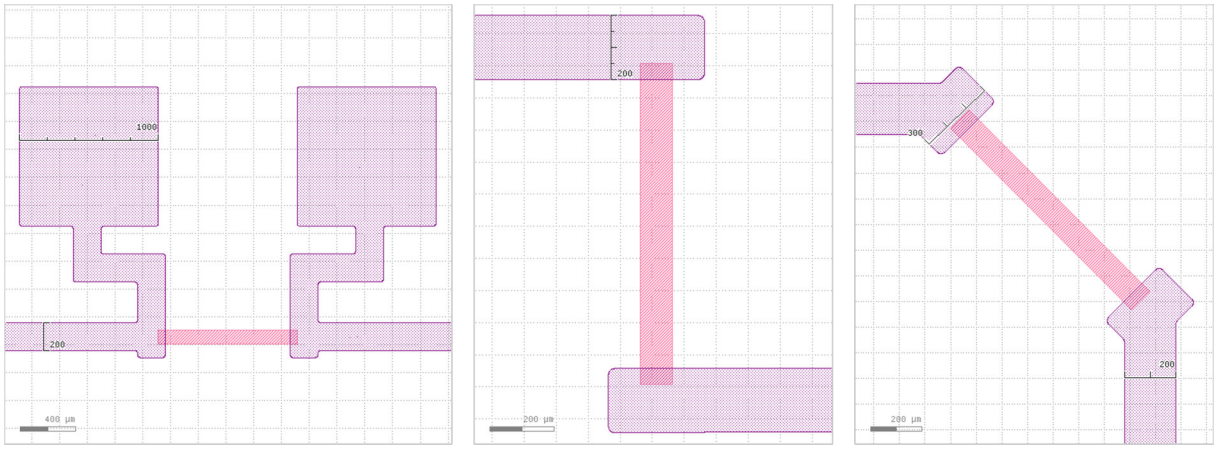


Figure 4.8: Layout of the design conductive path connected to 1000 μm long piezoresistors oriented at (a) 0 °, (b) 90 ° and (c) 135 °

The exterior contact pads connected to the resistors have a square shape and are 2000 μm wide. The pads were designed to be this large, so it is possible to perform electrical measurements manually without difficulty. Each pad is separated to one another at a distance of 1000 μm as explicit in Figure 4.9.

4.2.2 Chip dimensions

Based on the dimensions of the pads and the distance between them, it was established that each chip must have a width of 1 cm. It is preferable that the chip has a high length per width ratio to allow the better confinement of stress direction. However, if the chip is too large, fewer devices can be fabricated on an 8 inches Si wafer.

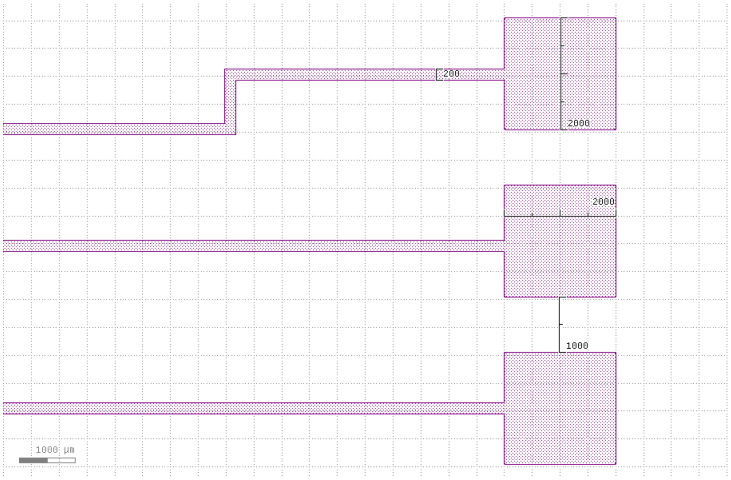


Figure 4.9: Layout of the contact pads.

Based on this limitation, the devices were designed to have a length of 3 cm, which means that the standard Si wafer can accommodate the fabrication of a total of 42 devices, 14 of each type designed as illustrated in Figure 4.10.

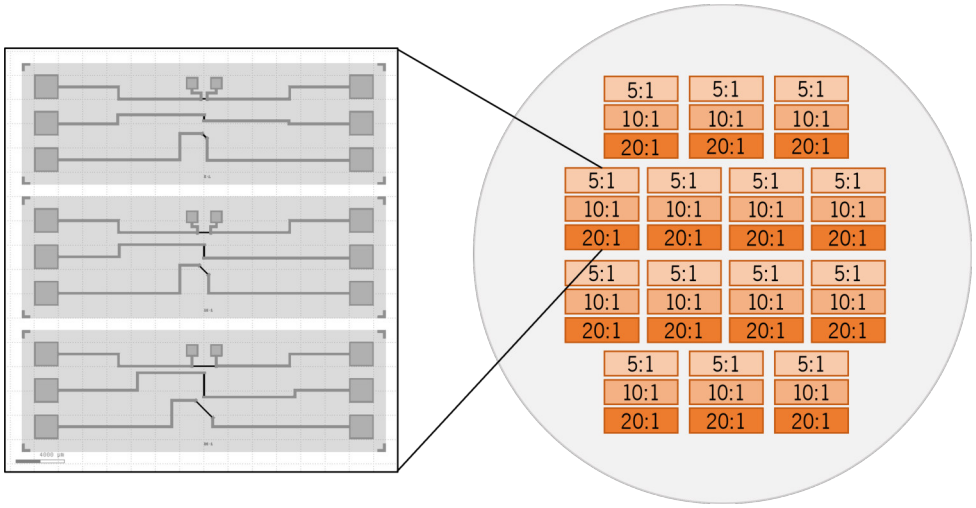


Figure 4.10: Distribution of the different chips on an 8 inch wafer.

4.3 Device fabrication

Posterior to the layout design for the test devices, this section provides a detailed description of the fabrication process of these devices. The process can be divided in 4 steps:

- **Piezoresistors layer**: The first step comprises the piezoresistive layer patterning into the piezoresistors.

- **Conductive path layer**: An AlSiCu layer is shaped to form the conductive paths that connect the resistors to the contact pads.
- **Isolation layer**: A finishing layer of SiO_2 is deposited on top of the wafer to provide isolation to the external environment.
- **Assembly**: The last step consists in releasing the chips from the wafer and the assembly of the devices for further characterization.

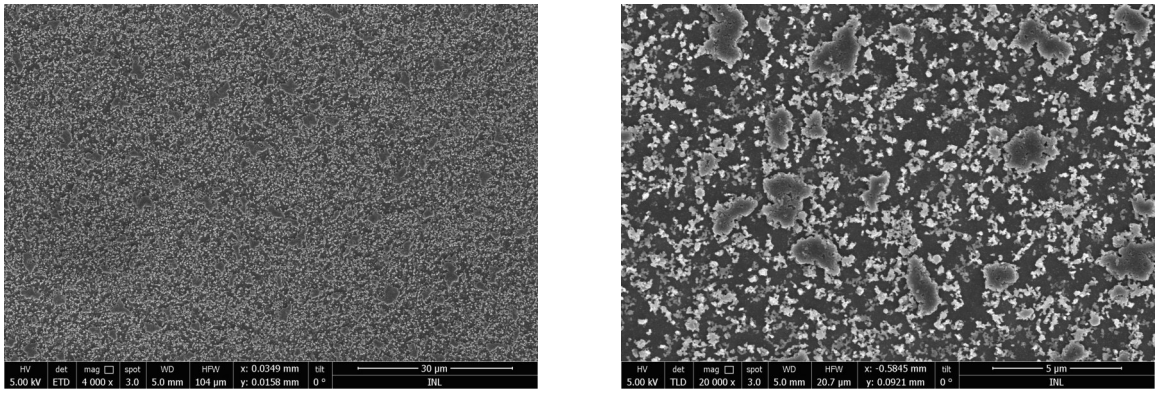
4.3.1 Piezoresistors layer

The device fabrication process starts by depositing 100 nm of SiO_2 on top of a Si wafer by PECVD (using STPS MPX CVD) with a deposition rate of 42.77 nm per minute.

Subsequently, a 200 nm thick AlSiCu layer is sputtered using Timaris FTM PVD, followed immediately by the deposition of amorphous silicon with a target thickness of 250 nm conducted in the CVD equipment previously used, at a deposition rate of 53.23 nm per minute.

The system enters the CVD chamber (Roth and Rau MicroSys 400), where the wafer is annealed at a temperature of 450 °C for 8 hours in vacuum. After the thermal treatment imposed, the AlSiCu layer that migrated to the top is removed by an etching solution at room temperature with mild agitation.

The polycrystalline film obtained was inspected via SEM and the result is depicted in Figure 4.11.



(a) (b)

Figure 4.11: SEM pictures of the poly-Si layer obtained in (a) broad view and (b) close up perspective.

The conductivity of the piezoresistive film was evaluated by sheet resistance measurement mediated by a four point probe system (AITCO CMT-SR2000N). The result of the measurement is depicted in Figure 4.12. The non uniformity of the sheet resistance values along the wafer can be explained based on

the poor distribution of the silicon islands on the piezoresistive film, however, after the metallization for the electrical contacts, it is expected to have a more uniform resistance distribution.

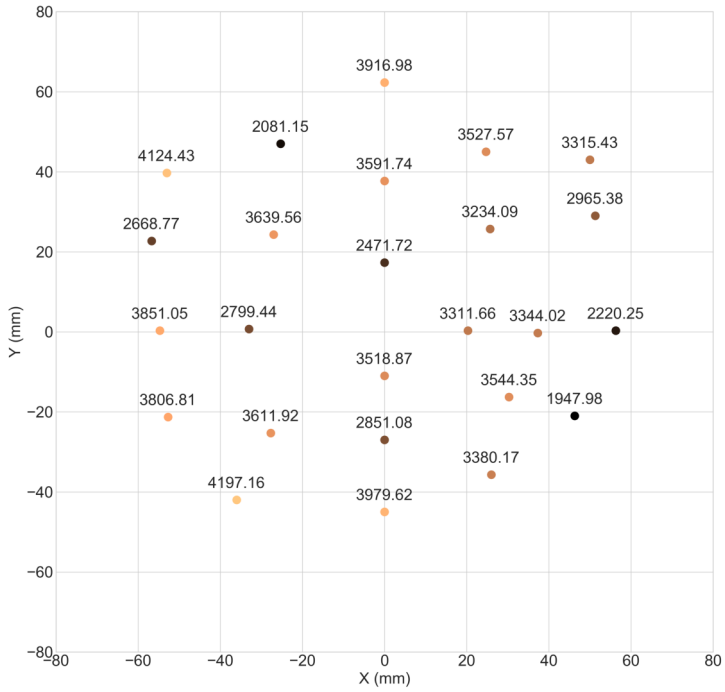


Figure 4.12: Graphic showing the sheet resistance (Ω/sq) measured in 25 points of the wafer.

To pattern the piezoresistive film into resistors, a lithography process is employed. The process is schematized in Figure 4.13 and starts by introducing the wafer into an oven where it is vapor primed with HDMS for 300 seconds at 150 °C to induce the wafer dehydration (Figure 4.13a), so the photoresist can adhere better to the substrate.

The next step consists of covering the dehydrated wafer with a positive photoresist, AZ1505, by a spin coating process using Karl Suss Optical Track equipment (Figure 4.13b). At this point, the wafer goes to the DWL 2000 lithography instrument that uses a laser to expose the designed layout. The exposure performed is a dark type which means that the laser will reach the photoresist in the area where the layout is present, hardening it (Figure 4.13c). The remaining resist not exposed in DWL is removed by a developer in Karl Suss Optical Track (Figure 4.13d). The unprotected piezoresistive film is etched by Reactive Ion Etching (RIE) using SPTS Pegasus for 40 seconds (Figure 4.13e). Finally, the remaining resist is stripped by Plasma Asher (using PVA Tepla GIGAbatch 360M) for 20 minutes, leaving the patterned film on the wafer (Figure 4.13f).

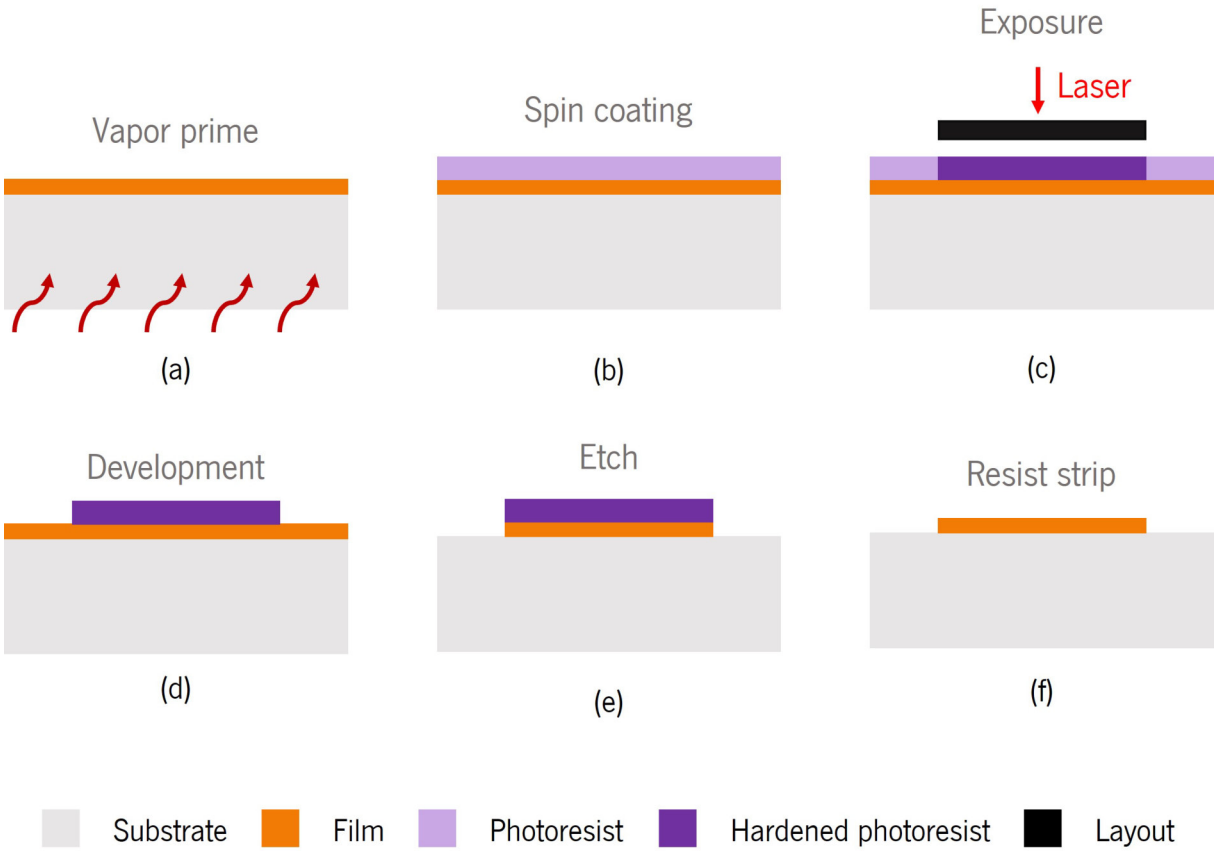
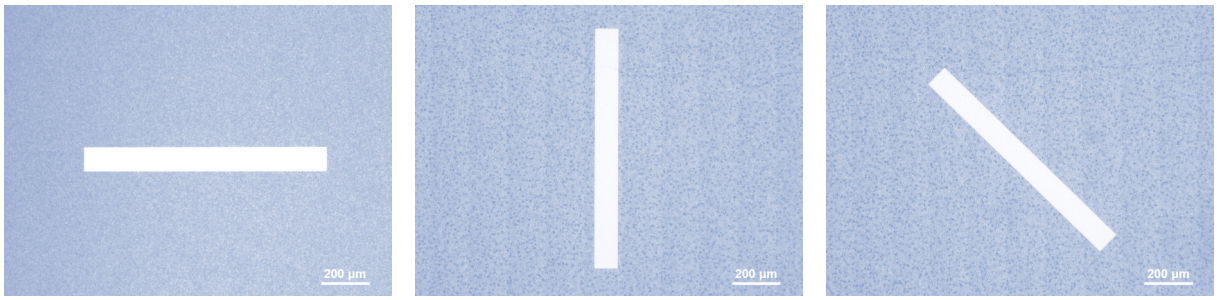


Figure 4.13: Schematic illustration of the laser patterning process employed.

Figure 4.14 shows microscope photos of the patterned piezoresistive film for the device with resistors with dimensions 1000 μm $\times$ 100 μm.

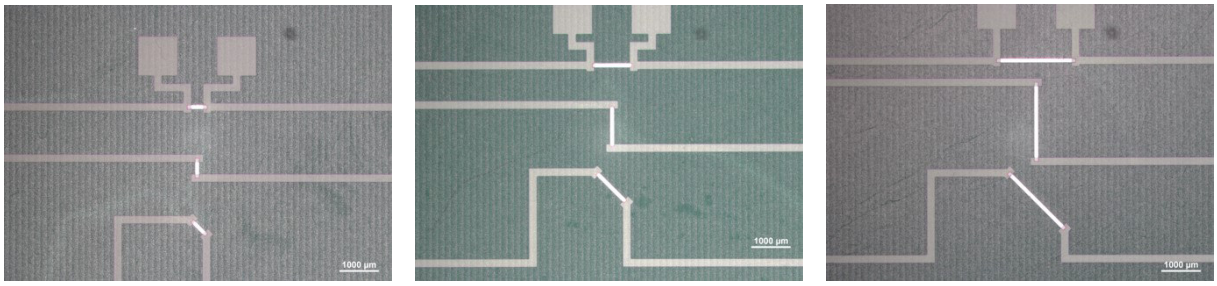


(a) (b) (c)

Figure 4.14: Microscopic photos showing the patterned piezoresistors with dimensions 1000 μm x 100 μm.

4.3.2 Conductive paths layer

Following the piezoresistors patterning, an AlSiCu layer was deposited on top of the wafer by PVD (using STPS Timaris FTM) with a target thickness of 1 μm. Similarly to the previous layer, the wafer was coated with AZ1505 and the mask was exposed using Heidelberg DWL 2000. After developing the photoresist, the contacts had the profile depicted in Figure 4.15.



(a) (b) (c)

Figure 4.15: Microscopic photos of the hardened photoresist forming the conductive paths.

The exposed AlSiCu was removed by a wet etching process and subsequently the remaining resist was etched by Plasma Asher. The resultant metallic layer from the patterning process is shown in Figure 4.16.

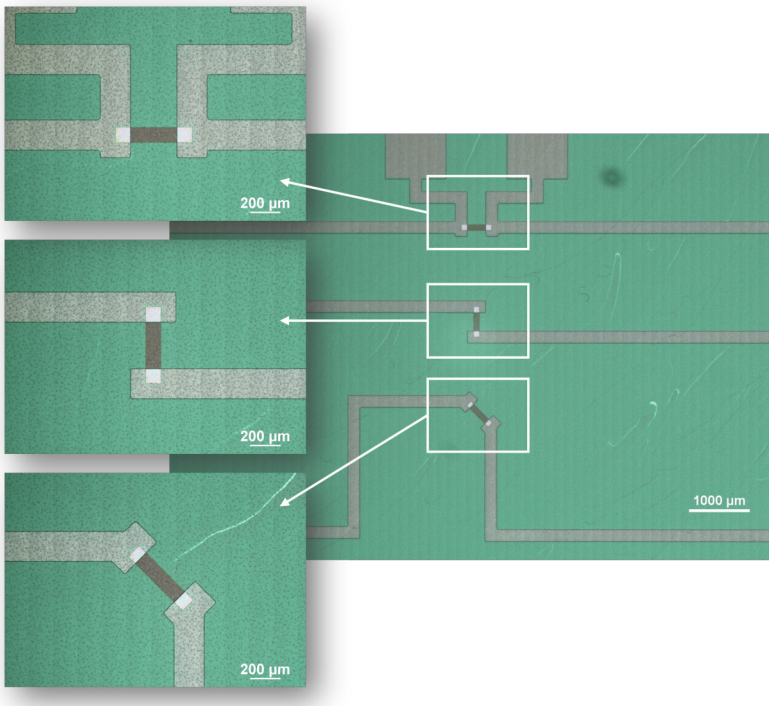


Figure 4.16: Microscopic photos of the patterned conductive paths connecting the piezoresistors with dimensions 500 μm x 100 μm.

4.3.3 Isolation layer

In order to protect the piezoresistors and the conductive paths of the environment, a 300 nm thick SiO_2 layer was deposited on top of the wafer by PECVD with a deposition rate of 42.77 nm per minute. Appendix D shows the mask used to pattern the isolation layer.

The layer is open at the contact pads, so they are reachable for future bonding. The patterning process is conducted by the same lithography process shown in subsection 4.3.1. The portion of film uncovered by the photoresist is etched by RIE using SPTS APS with an over etch of 20 %. After this step, the remaining photoresist is eliminated by Plasma Asher. Figure 4.17 shows the resultant SiO_2 layer around the pad with a borderline with a thickness approximate to 100 μm as designed.

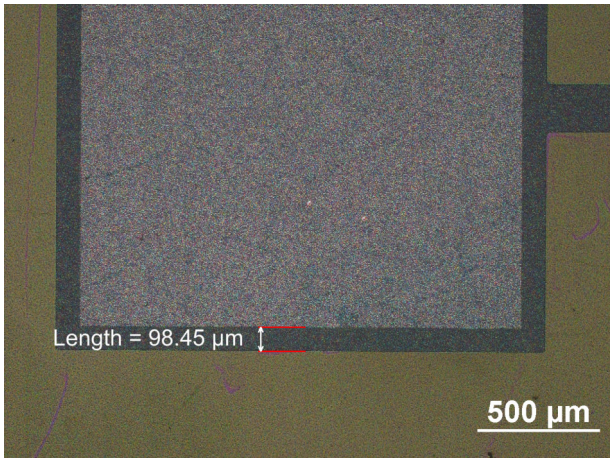


Figure 4.17: Microscopic photo of a contact pad showing the pattern of the oxide layer.

4.3.4 Backside etch

After the fabrication of the test devices, it is necessary to release the chips from the wafer. This can be accomplished by the dicing technique, in which a dicing blade mechanically saws the wafer. Alternatively, the devices' release can be done by etching the backside of the wafer on the limits around the devices. This last approach was implemented in the current fabrication process using the layout shown in Appendix E.

The first step consisted of depositing 3 μm of SiO_2 on the backside of the wafer. This layer acts as an etch stopper, so the area covered with the oxide is not etched. Similar to the process implemented in previous layers, the wafer was then vapor primed with HDMS followed by a spin coating of AZ4110 photoresist (Figure 4.18a).

It is imperative that the Backside (BS) layer is aligned with the front side layers already developed. To obtain an accurate alignment, a mask containing alignment marks was exposed using Suss MA6BA6 using UV-light (Figure 4.18b). This resulted in a wafer covered with photoresist except for the area where

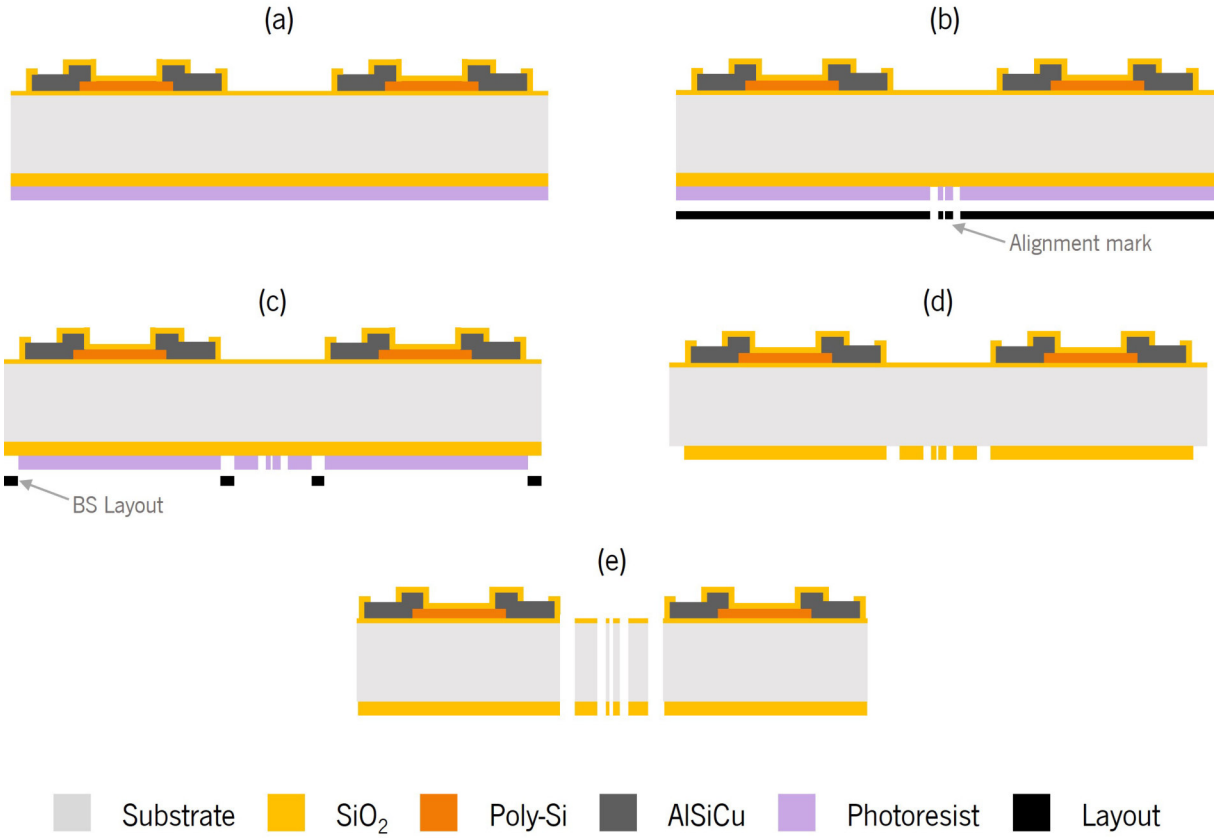


Figure 4.18: Schematic illustration of the device release process.

the alignment marks are present.

A clear-type exposure was implemented to expose the backside designed layer on the wafer. In clear-type exposures, The areas defined in the layout will not be exposed to the laser and will be removed in the development step (Figure 4.18c). This means that the photoresist will protect the wafer except in the area around the devices.

After developing the photoresist, the SiO_2 uncovered by the resist was etched by RIE in SPTS APS with an over etch of 20 % to expose the wafer substrate (Figure 4.18d). The final step of this process consist on the release of the devices from the wafer by the RIE technique performed on SPTS Pegasus with a duration time of 72.5 minutes (Figure 4.18e).

The result of this process is 42 chips segregated from the wafer with the shape shown in Figure 4.19.

4.3.5 Assembly of the devices

In order to perform the characterization step, it is necessary to adapt the fabricated chips. This is done by attaching each chip to a carrier made of Printed Circuit Board (PCB) on each side with glue, where electrical cables can be connected, avoiding the interference of manual measurements as shown in Figure 4.20.

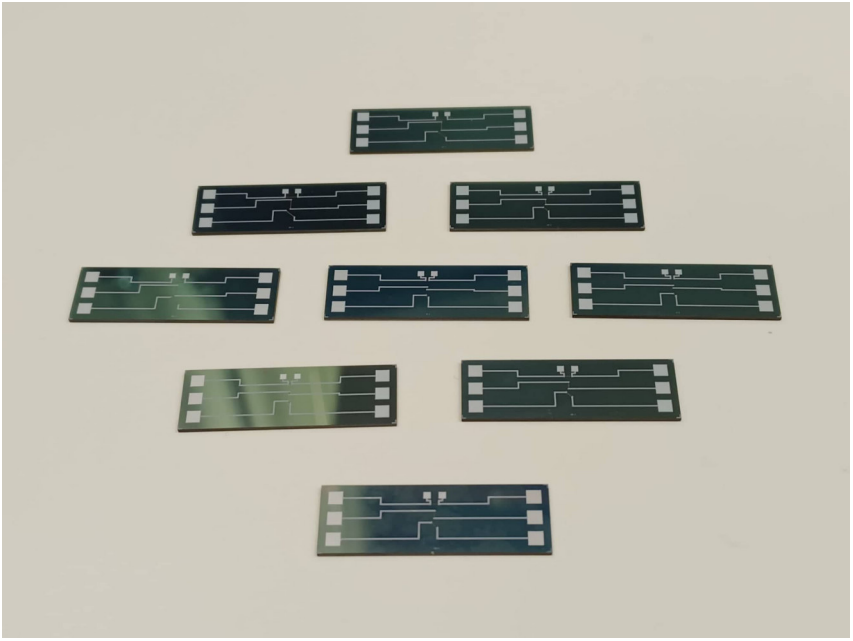


Figure 4.19: Photography of some chips fabricated for the characterization step.

After coupling the PCBs to the chips, the electrical connection between the parts is indispensable. This is carried by a wire bonding process called aluminum wedge bonding, in which a thin aluminum wire is attached to the conductive pads (usually made of aluminum or gold). The aluminum wire is positioned in the pad by the auxiliary of a needle, and the combination of ultrasounds and force allows the bond of the aluminum wire at room temperature.

Finally, six electric cables are welded in the PCB apertures to facilitate the measurements in future steps.

4.4 Layer patterning on top of Polyimide

In the last chapter, the metal-induced crystallization process was tested using a sample covered with polyimide (see section 3.3). It was shown that the layer exchange process was successful, and the obtained silicon layer showed a crystalline structure similar to the tests performed without the polymeric layer. However, it is known that the adhesion between polyimide and other materials is poor and the behavior of the developed polycrystalline silicon layer was not yet explored.

Using the design layout for the test devices, the sample containing polyimide was subjected to the same fabrication procedures employed for the test devices.

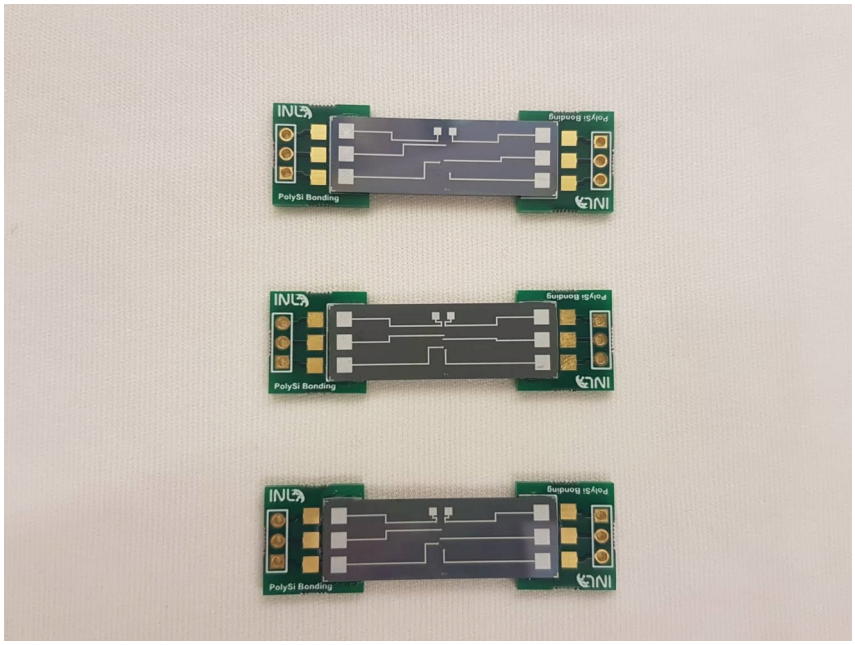
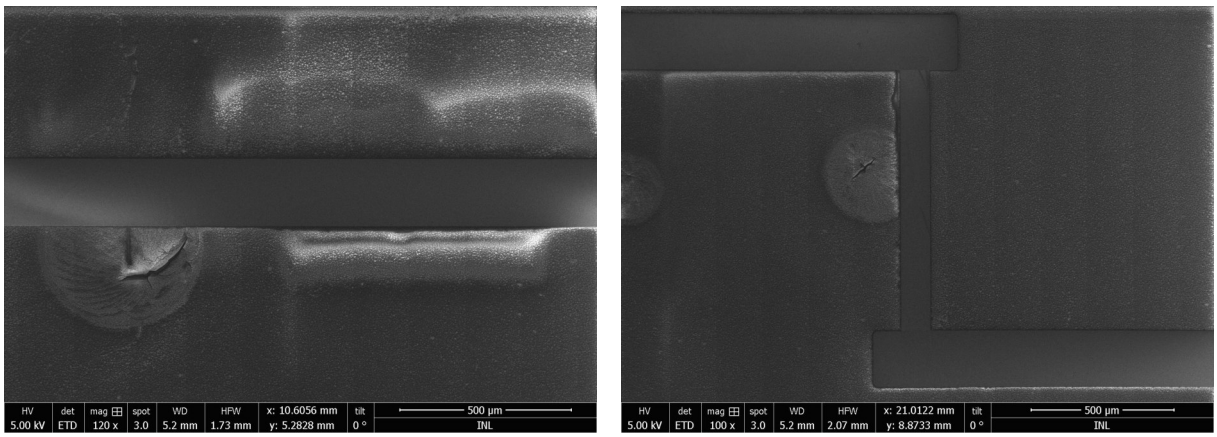


Figure 4.20: Photography of different chips attached to PCB carriers.

The SEM pictures in Figure 4.21 show two piezoresistors on top of the polyimide. It is possible to conclude that the poly-Si film did not lose the adherence to the substrate, maintaining its structure. This result leads to the conclusion that it is possible to pattern poly-Si on top of polyimide, confirming the viability of developing piezoresistive flexible devices with the fabrication polycrystalline silicon film.



(a) (b)

Figure 4.21: SEM pictures showing patterned piezoresistors on top of a polyimide layer.

4.5 Conclusions

In this chapter, the design and fabrication process of test devices is presented. Based on the fact that the piezoresistive behavior of the developed film can change with the direction of the applied stress, the test device is designed to contain 3 piezoresistors differently oriented. Since the behavior of the piezoresistors is still unknown, three different chips were designed to have a width of 100 μm while the length was varied between 500 μm, 1000 μm and 2000 μm. Every chip has dimensions 1 cm $\times$ 3 cm which allows the fabrication of 42 chips (14 of each type).

The patterning of polysilicon developed on top of polyimide was tested using the layouts designed for the test devices. When observing the obtained structures in SEM, it was shown that the polysilicon film could be patterned without flaking from the polymeric layer. This is a result that reinforces the viability of developing flexible devices with polysilicon as sensing material.

Characterization

This chapter presents the characterization tests performed on the fabricated devices, allowing the objective evaluation of the performance of the polycrystalline silicon film developed in this work. The experimental tests include the extraction of the TCR and the GF of the material. This chapter also presents the photosensitivity effect observed in the fabricated samples.

5.1 Photoelectric properties

Previous to the characterization process, the resistance of each piezoresistor was measured. However, the values obtained were not consistent since they varied between measurements. To understand the behavior of the resistors, their stability was evaluated by connecting one resistor with dimensions 1000 μm $\times$ 100 μm to the Agilent 34410A Multimeter. The resistance value is acquired at a rate of 1 Hz for 24 hours, and the multimeter transfers the measurements to a computer to which it is connected.

It was expected that the resistance value would progress to a stable value at the beginning of the measurements and maintain this value for the remain of the testing. However, the resistance value acquired during the 24 hours did not behave as predicted and is illustrated in Figure 5.1.

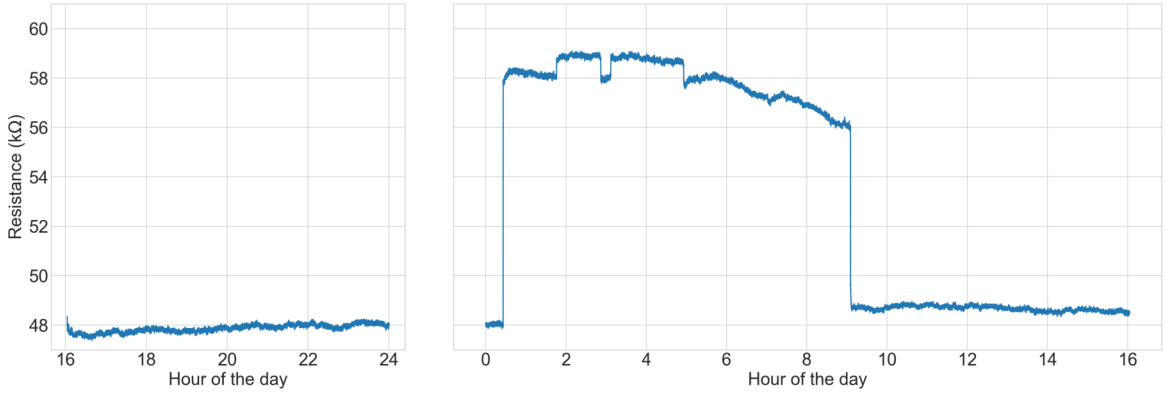


Figure 5.1: Resistance change measured during 24 hours.

The plot shows that for the first 8 hours of the test (from 16:00 to 00:00), the resistance value stayed stable at 48kΩ. Surprisingly, around 2:00 of the following day, this resistance abruptly changed to 58 kΩ, a value 20% higher than at the beginning of the test. This value started to decay gradually at 6:00, and at 9:00, the resistance returned to its original value instantaneously.

This result concludes that some environmental change must be causing this unpredicted effect. The temperature effect was easily discarded because the laboratory where the tests were conducted did not suffer drastic temperature changes.

The second proposal was the possible defects in electrical contacts, so as soon as one person came close to the chip to investigate, the resistance value started to rise again. It was then found that the incidence of light in the laboratory led to the changes in the electrical resistance.

Knowing that it is the light effect that boosts the variance of the electrical resistance, the result from the 24 hour-long test can be interpreted in the following way,depicted in Figure 5.2:

- **16:00 to 00:15**: During this time of the day, the lamps in the laboratory are turned ON, which translates to an electrical resistance value of 48 kΩ
- **00:15 to 6:00**: At night, the laboratory is not being used, so the lamps are turned OFF, making the electrical resistance value instantly rise to 58kΩ. Some fluctuations of the resistance occur during the night, possibly due to lamps being turned ON and OFF on spaces around the laboratory, which has windows.
- **6:00 to 9:00**: Around 6:00 in the morning, the light provident from the sunrise starts to illuminate the laboratory, leading to a gradual decay of resistance until 56 kΩ.
- **9:00 to 16:00**: At 9:00, the laboratory is used again, and the lights are turned back ON, leading to the instant decay to the original resistance value, 48kΩ.

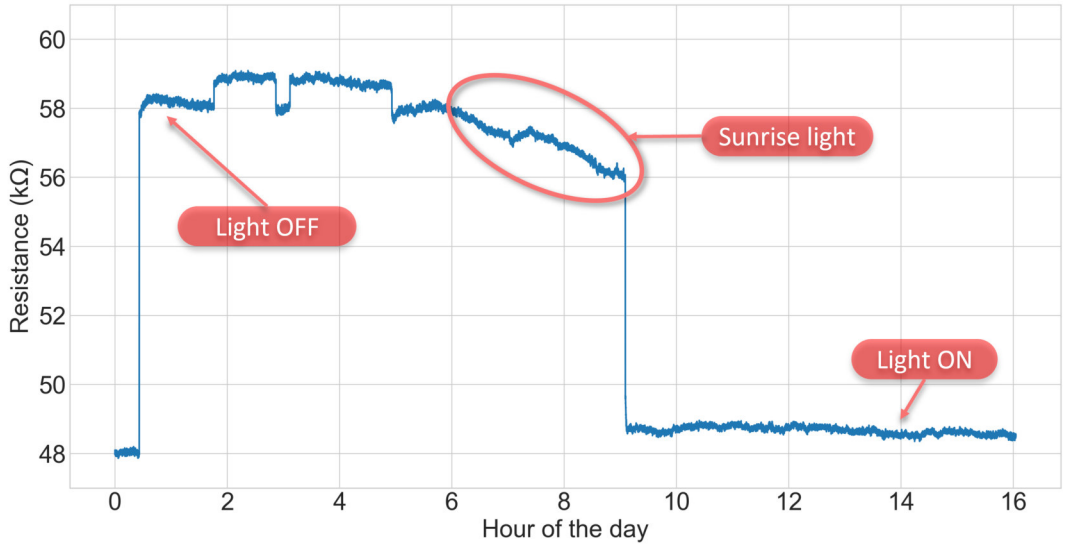
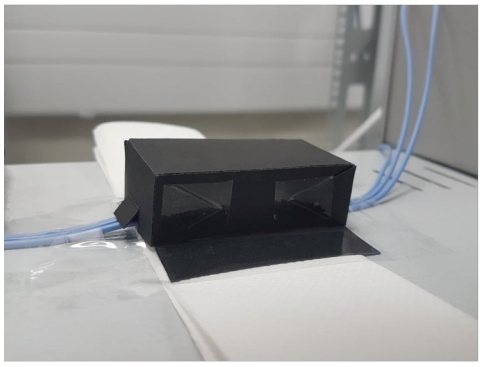


Figure 5.2: Main events associated with the resistance change.

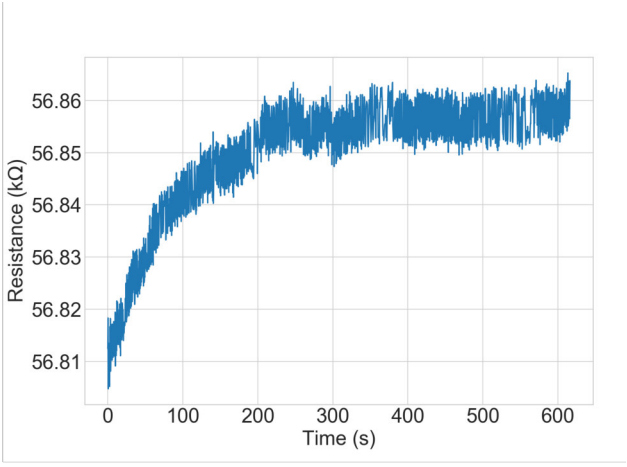
5.1.1 Setup for stability measurements

To understand if the resistors had a stable value without the influence of the light, a black box was built only with apertures for the cables, as shown in Figure 5.3a.

In this configuration, the resistors behaved as predicted, reaching a stable value after 3 minutes as the plot of Figure 5.3b shows, for a resistor with dimensions 1000 μm $\times$ 100 μm oriented at $\phi = 90°$.



(a)



(b)

Figure 5.3: (a) Black box covering the device for stability measurements; (b) Resistance change with time.

The nominal value of the resistors chosen for further characterization are summarized on Table 5.1. Each device is named after its dimensions, so R5 means that the device is constituted by resistors with L/w = 5. The second number, 1 or 2, attributed to the devices, is arbitrary to distinguish the devices with the same characteristics.

Table 5.1: Summary of electrical resistance of the piezoresistors used in characterization steps.

Device	Orientation [°]	Resistance [kΩ]	Device	Orientation [°]	Resistance [kΩ]
R5.1	0	20.3	R5.2	0	19.3
	90	20.1		90	19.1
	135	23.6		135	22.5
R10.1	0	58.3	R10.2	0	57.2
	90	57.4		90	57.2
	135	57.9		135	57.5
R20.1	0	113.5	R20.2	0	125.6
	90	110.3		90	126.3
	135	116.5		135	131.4

5.1.2 Physics behind the photoelectric behavior

The contact between two different materials like poly-Si and AlSiCu is called a heterojuction. If this contacts show low resistivity and insensibility to the direction of the current that flows through, then the contact is called an ohmic contact [Ferreira and Vasilevskiy, 2006].

If a semiconductor has two ohmic contacts, then it forms a photoconductor.

If the beam of photons that hit the ohmic contact have an energy superior to the gap energy of the semiconductor, E_g, then they will be absorbed and form an electron-hole pair.

When an electric field is applied to the device, the electron-hole pairs are transported, resulting in a photocurrent [Saleh and Teich, 2003].

By Ohm's law, this current emergence leads to an increase of the semiconductor conductivity. This increase is then proportional to the photon flux that reaches the material.

This is why, in the experiments, it was observed an abrupt drop of the resistance value when the devices were exposed to environment light.

5.2 Temperature effect

The behavior of the piezoresistive material can be influenced by the environment temperature, and this effect is quantified by the TCR previously introduced in section 2.2.

5.2.1 Setup

To extract this coefficient, the experimental tests were conducted in a climate chamber (Weiss WKL 34/70) where the temperature was varied between 25 °C and 40 °C with a heating rate of 4 °C per minute. The climate chamber is connected to a computer that collects the temperature felt in the course of the test. Three arbitrary samples were chosen to be tested to confirm the consistency of the values acquired.

By turns, each sample was inserted in the climate chamber and one of the resistors is connected to the Agilent 34410A Multimeter that acquires its resistance value, as shown in Figure 5.4. This multimeter is then connected to the computer in which the data in collected.

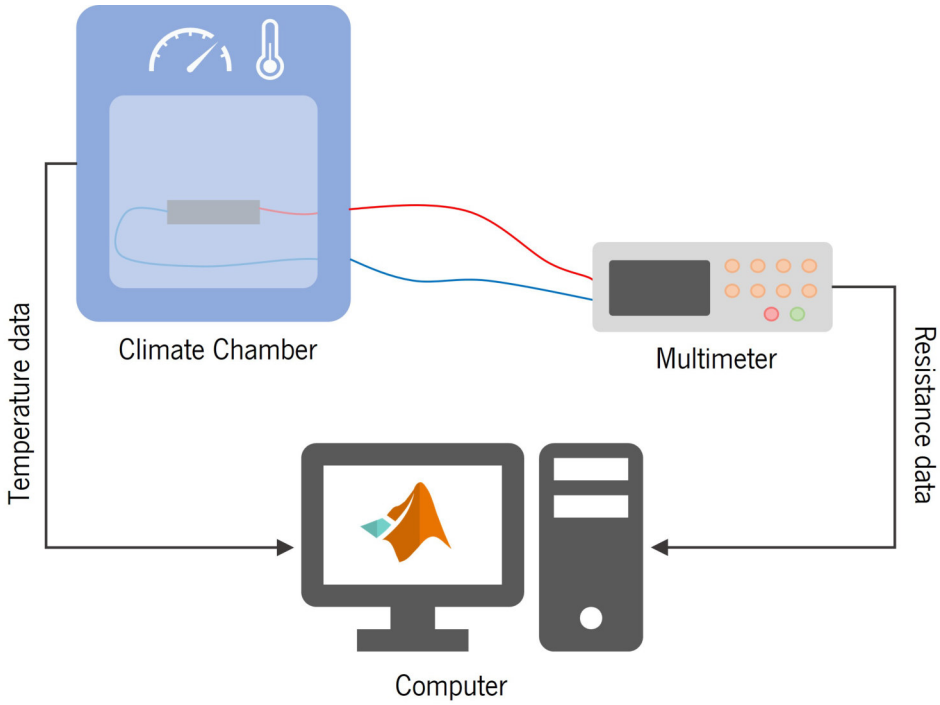


Figure 5.4: Diagram of the connections between equipments for TCR measurements.

5.2.2 Results

Using the MATLAB software, the data from the climate chamber is correlated to the multimeter data, generating a file with the electrical resistance value in order to the temperature of the chamber. The

data from each resistor is visually explicit in the plots of Figure 5.5. By adapting the data with a linear regression, it is possible to extract the TCR for each resistor.

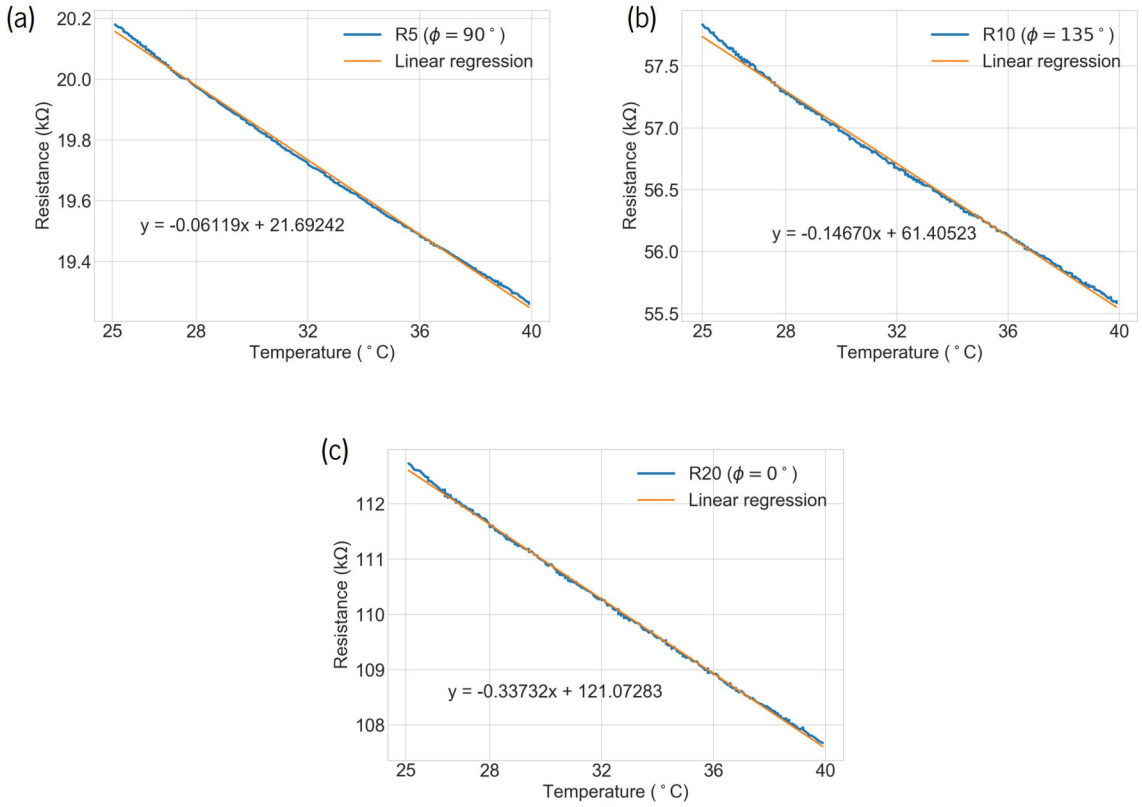


Figure 5.5: Resistance change with temperature for different piezoresistors.

In Table 5.2 are the calculated coefficients, where the mean value is -0.00298 /°C with a standard deviation, σ_s, of 0.00024. The low value of σ_s proves the consistency of the TCR for different samples, so further testing was not required.

Table 5.2: TCR values calculated for three different piezoresistors.

Device	**TCR [/°C]**
R5.1 ($\phi = 90°$)	-0.00317
R10.1 ($\phi = 135°$)	-0.00264
R20.1 ($\phi = 0°$)	-0.00313

This result shows that the resistors are sensitive to the environment's temperature and can be applied to temperature-sensing devices. In contrast, if this effect is not desired, it can be canceled by positioning the piezoresistors in a Wheatstone bridge configuration.

5.3 Piezoresistive performance

5.3.1 Setup assembly

The tests were conducted on the Universal Testing Machine Shimadzu AGX-V 10 kN presented in Figure 5.6, a precision testing machine to evaluate the mechanical behavior of materials. This equipment is supported by TRAPEZIUMX-V software, in which the test conditions are imposed. This conditions can be applied in terms of force and displacement, and the load cell fixed in the equipment applies the conditions on the sample being tested.

In these tests, a force ranging from 0 to 50 N was applied to study the possibility of using this material in a broad range of forces.

The setup where the sample is tested can be adapted for different tests, which allows the placing of a personalized four point bending fixture on the stage.

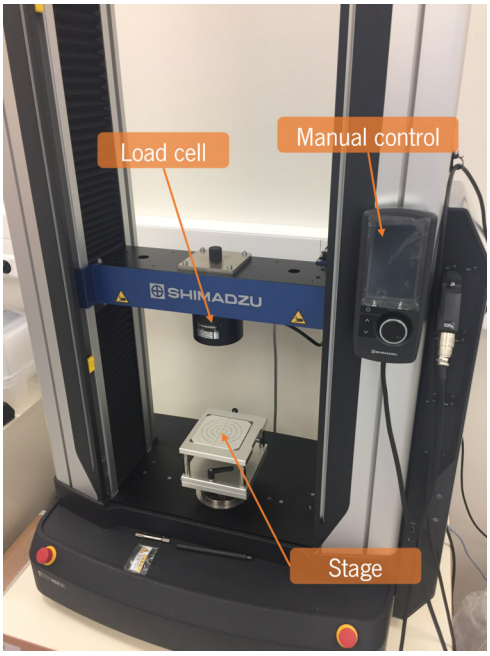


Figure 5.6: Picture of the Universal Testing Machine used for the application of force.

The structures corresponding to the load beams and support beams were fabricated in aluminum by the micro-machining technique. In this process, a piece of the chosen material, in this case aluminum, is carved with a high precision to assemble the designed piece. The resultant structures produced by the machining process are shown in Figure 5.8a and 5.8b, respectively.

The structure of the load beams is fixed to the load cell, whereas the structure of the support beams is fixed to the stage. The devices are positioned on top of the support beams as shown in Figure 5.8c.

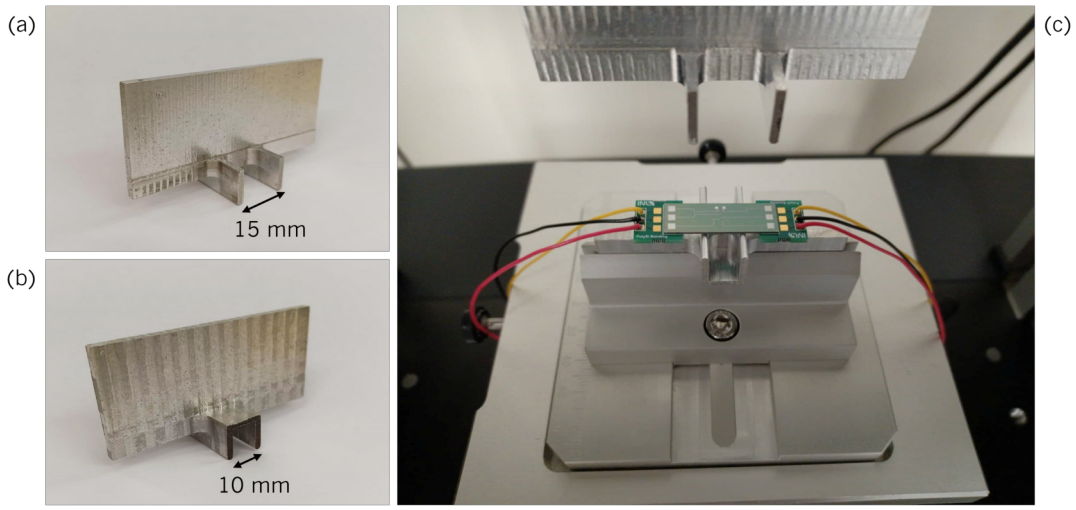


Figure 5.7: Machined pieces for the (a) load beams and (b) support beams; (c) Positioning of the device in the setup.

One resistor per test is connected to the Agilent Multimeter that exports the resistance data to a computer. The data treatment from the testing machine is performed in TRAPEZIUMX-V software. The outputs are correlated by a Python script that also estimates the GF of the material. This setup is illustrated in Figure 5.8

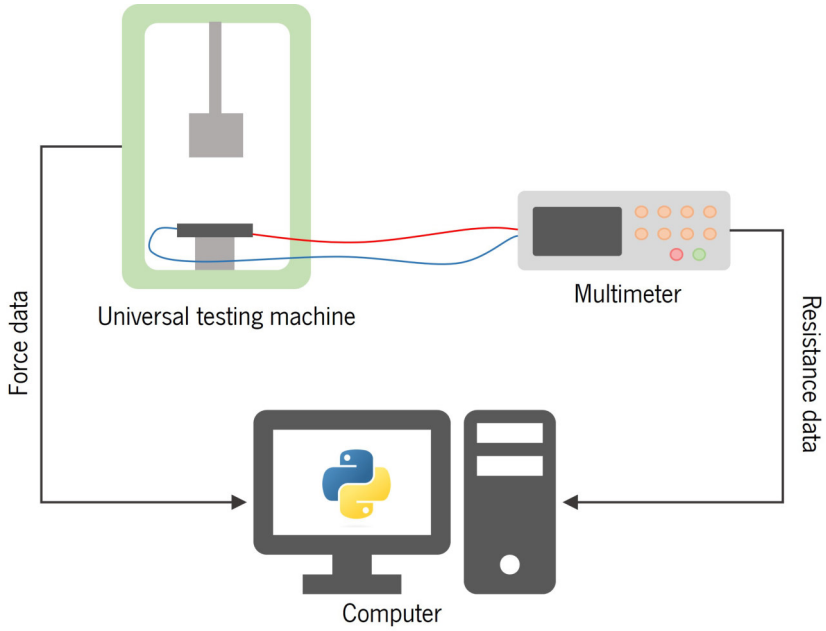


Figure 5.8: Diagram of the connections between equipments for Gauge Factor extraction.

5.3.2 Results

As seen in Equation 4.2, the relative resistance change can be dependent on the direction of orientation of the piezoresistors. Typically, silicon-based resistors oriented at $\phi = 0°$ show a positive resistance variance, whereas for the resistors oriented at $\phi = 90°$, the variance is less significant and has a tendency to decrease. Since the resistor oriented at $\phi = 135°$ is the intersection between the both effects, it is expected that the resistance has an increasing tendency, but less significant than the first.

Figure 5.9 shows the resistance variance with strain for the device R5.1. The resistors behaved as expected, with the resistors oriented at $\phi = 0°$ and $\phi = 135°$ showing a rising behavior, while the resistor oriented at $\phi = 90°$ shows a tendency to decrease with strain.

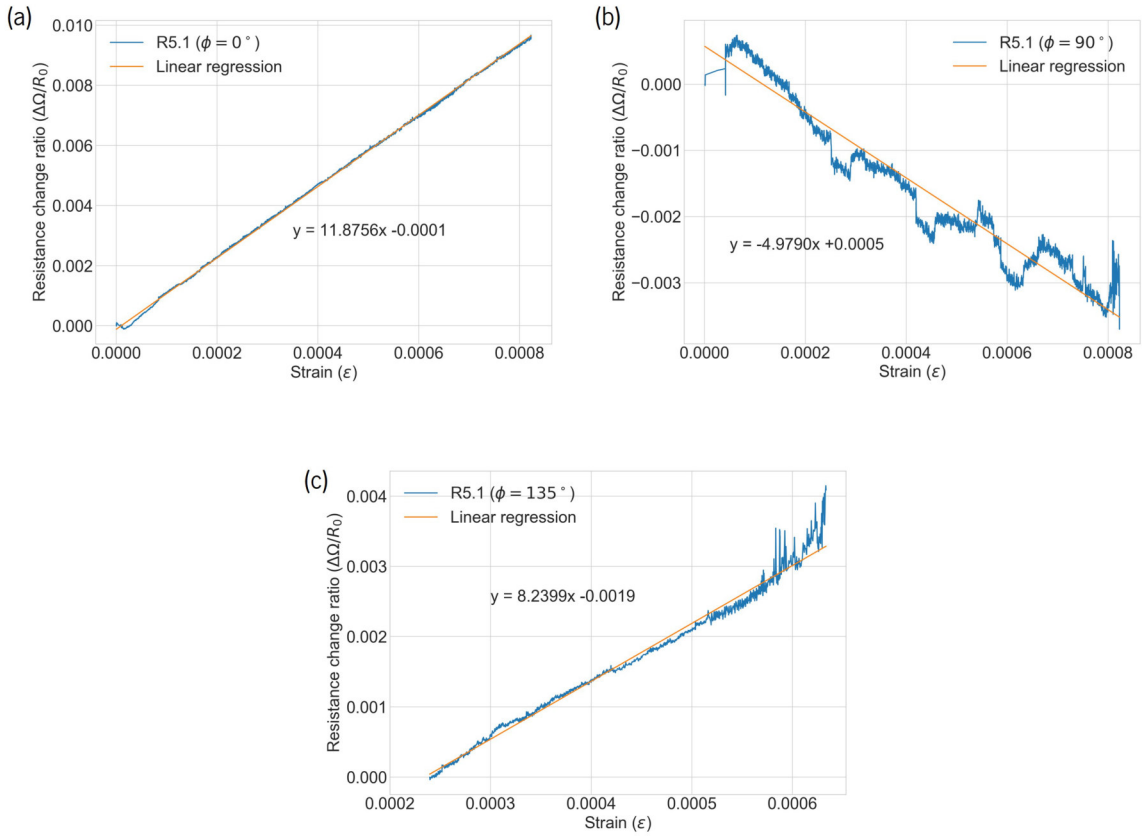


Figure 5.9: Resistance change with strain of R5.1 device resistors oriented at (a) ϕ = 0 °, (b) ϕ = 90 ° and (c) ϕ = 135 °

The GF of the remaining devices are detailed in Table 5.3. The resistors oriented at $\phi = 0°$ a better sensitivity, as expected, with a mean value of GF = 12.31 and σ_s = 0.33.

As for the piezoresistors oriented at $\phi = 90°$, GF = -4.90 and σ_s = 0.35. This value coincides with the expectations that these piezoresistors showed less sensitivity and that the resistance value decreases

with the increase of strain.

Finally, the piezoresistors oriented at $\phi = 135°$ evidences a mean value of GF = 6.73 and σ_s = 2.64.

The high σ_s associated with the measurements of the resistors oriented at ϕ = 135 ° suggests that the bending test can have occasional malfunctions. These malfunctions can be derived from imperfect positioning of the sample on the set-up or intrinsic failure of the testing machine.

Table 5.3: Gauge Factor obtained for different piezoresistors.

Device	Orientation [°]	GF	Device	Orientation [°]	GF
R5.1	0	11.87	R5.2	0	12.07
	90	-4.97		90	-4.64
	135	8.24		135	5.98
R10.1	0	12.71	R10.2	0	12.79
	90	-4.96		90	-4.57
	135	4.09		135	5.07
R20.1	0	12.22	R20.2	0	12.21
	90	-4.66		90	-5.61
	135	5.08		135	11.89

5.4 Conclusions

This chapter presents the characterization procedures of the piezoresistive material using the test devices previously fabricated.

During the resistance measurements of the different piezoresistors, it was found out that the fabricated devices were sensitive to light. The resistance value of this piezoresistors increased with in the absence of light and decreased abruptly when exposed to light. This phenomenon occurs due to the heterojunction formed between poly-Si and AlSiCu. These heterojunctions form a Schottky contact on opposite sides of the resistor, creating a Metal-Semiconductor-Metal (MSM) photodetector. This finding leads to the conclusion that the developed polycrystalline silicon film can be used in photonic circuits. Also, the fact that the material can be developed on top of polyimide indicates that flexible photonic circuits can be developed in future projects.

The temperature effect on the electrical behavior of the resistors was tested on a climate chamber for temperatures between 25 °C and 40 °C. It was found that the electrical resistance decreases with the

temperature rise with a rate of -0.00298 /°C, suggesting that the polycrystalline silicon can be used in temperature sensing devices.

The last characterization step comprises the Gauge Factor extraction. The set-up for the measurements consists of a four point bending fixture that allows the application of a unidirectional stress in the device. The tests were performed for forces between 0 and 50 N to study the possibility of using this material is different force ranges. These tests demonstrated that piezoresistors oriented in the direction of the applied stress are more sensitive with a GF = 12.21. This is a satisfactory value since it is comprehended in the range of Gauge Factors found in the literature review.

Conclusion and Future Work

This dissertation proposed the development of a piezoresistive material to be implemented in MEMS devices. Since the methods used to fabricate MEMS are low-temperature processes (< 500 °C), the developed piezoresistive material must follow this condition to be completely compatible. In addition, expanding the application of the developed material to flexible MEMS is an exciting step since it broadens the applicability of the piezoresistive material. The achievement of this goal was oriented by the research question imposed in Chapter 1. The work allowed the answer to these questions as follows:

- **Question 1**: Which piezoresistive materials have been implemented in the literature, and what differentiates them?

This question is addressed by Chapter 2. Several materials show piezoresistivity. Metals are easily obtained on top of flexible substrates. However, they are the materials less sensitive to strain with a Gauge Factor (GF) < 5. On the other hand, semiconductors have higher GF and are more commonly used in piezoresistive devices. From the group of semiconductors studied, polycrystalline silicon has a high GF that typically ranges from 10 to 77. This material is less sensitive than monocrystalline silicon. However, it can be placed on different substrates. One attractive characteristic of this material is that its electrical behavior can be tuned with the doping level and variation of structural properties.

- **Question 2**: Which strategies have already been used to obtain piezoresistive material at low temperatures?

This question is answered in Chapter 2. The material chosen to be developed in this dissertation was polycrystalline silicon, so the processes studied apply to this material. The direct growth of poly-Si is commonly achieved by CVD. However, the resultant film has a crystalline structure if the process is carried out at temperatures above 600 °C. This temperature has been decreased by applying a bias current to

the substrate, but this method damages the material creating fractures, thus reducing its quality. Another proposition is the introduction of HCl in the CVD chamber to mitigate the deposition of amorphous silicon. This strategy does not satisfy the conditions of this work because this gas is highly corrosive.

Apart from the direct growth method, there is the possibility of refining the silicon phase from amorphous to crystalline by crystallization techniques. One possibility for maintaining the substrate at a low temperature is Excimer Laser Annealing (ELA), where a laser is focused on the amorphous film that melts and re-crystallizes. The main drawback of this approach is the high cost associated with and relies on the laser energy density. Another possibility is crystallizing the material by the mediation of a metal. The presence of the metal reduces the crystallization temperature, proving a crystalline film at temperatures as low as 180 °C if aluminum is used as the catalyst metal.

- **Question 3:** Which parameters should be considered to evaluate the quality of the developed piezoresistive film?

The quality of the piezoresistive film can be evaluated by its structure and electrical behavior.

The parameters that influence the structure quality of the film are assessed in Chapter 2 and Chapter 3. The polysilicon film is said to have a good structure if the film is continuous, does not have undesired trapped elements, and has a crystalline structure. The film's continuity is visually evaluated using Scanning Electron Microscopy (SEM), whereas the element constitution is evaluated using Energy-dispersive X-ray Spectroscopy (EDX). Finally, the crystalline nature of the material is investigated by X-ray Dispersion (XRD).

The parameters that influence the film's continuity are the Si/AlSiCu ratio, the thickness of the oxide layer between the semiconductor and the metal, and the annealing conditions. It was found in Chapter 3 that higher annealing temperatures, a thinner oxide layer, and the introduction of gases in the annealing chamber (namely Argon and Hydrogen) boost the crystallization, providing a more continuous film.

The electrical behavior of the piezoresistive film is usually evaluated by the Gauge Factor (GF) of the material since higher gauge factors imply a better sensitivity to strain.

Polysilicon with Gauge Factors ranging from 10 to 77 can be found in the literature since the fabrication conditions influence this figure of merit. For instance, poly-Si films composed of bigger grains are expected to show a higher GF. In this work, the resultant poly-Si film annealed at 500 °C is composed of grains with a diameter of 63.77 nm, whereas the resultant film from the annealing treatment at 550 °C is composed of grains with a diameter of 75.64 nm. This result suggests that higher annealing temperatures favor the desired grain growth and, consequently, higher GF.

- **Question 4:** What is the feasibility of acquiring the piezoresistive material on a flexible layer?

This question is answered in Chapter 3 and Chapter 4. To conclude about the possibility of obtaining the poly-Si on top of flexible substrates, it is required that the crystalline process is well succeeded, meaning that the resultant film has a quality comparable to the film obtained directly on a rigid substrate namely a Si wafer. The SEM and XRD results showed that the polycrystalline silicon film developed on top of polyimide has a structure equivalent to the piezoresistive material developed on top of a Si wafer, as desired.

Once a favorable result for the crystallization step was obtained on top of a flexible substrate, the possibility of patterning the piezoresistive film was assessed by etching the material by Reactive Ion Etching (RIE). The obtained structure stayed attached to the polymeric layer without visible flaking, which means there is a possibility of exploring the application of this material in flexible devices.

- **Question 5:** In which way can the piezoresistive material response be influenced by external factors?

The poly-Si response to external factors is assessed in Chapter 5. The influence of the environment temperature was studied by introducing devices with piezoresistors and measuring the resistance for in a range of temperatures from 25 °C to 40 °C. The resistance value decreased with the temperature rise with a rate of -0.00298 /°C. This result evidences that the resistance is sensible to the environment's temperature, a behavior that is essential for temperature sensing devices. However, if this effect negatively affects the device's performance, the temperature effect can be canceled in a Wheatstone bridge configuration.

In this work, it was found out that the test devices fabricated are sensitive to light. When light reaches the piezoresistors, their electrical voltage drops instantaneously. This is due to the fact that when a beam of photons reaches the semiconductor, the photon is absorbed and forms an electron-hole pair. These pairs form a photocurrent and lowering the resistance of the semiconductor component. This finding suggests that the developed film can be applied in flexible photonic circuits.

6.1 Future Work

The work developed in this dissertation opens the possibility of developing sensing devices based on the piezoresistive transduction mechanism at low temperatures. Based on this achievement, future work can incorporate the following research lines:

- **Standard MEMS piezoresistive devices**: The developed material proved to be adequate to produce piezoresistive-based devices. Therefore, it is possible to proceed with the fabrication of Silicon-based MEMS for applications such as pressure and temperature sensing.

- **Flexible MEMS piezoresitive devices**: In this work, it was confirmed that it is possible to develop and pattern polycrystalline silicon on top of polymeric substrates. This opens the possibility of producing flexible devices based on the piezoresistive transduction mechanism.

  However, in the first phase, it is necessary to test the crystallization on top of other types of polyimide in an attempt to improve the degassing process introduced in this work.

- **Photonic devices**: The fabricated devices showed sensitivity to light, meaning that this effect can be explored to achieve photonic devices, namely photodetectors. The pursuit of this research line requires first characterizing the material's behavior, namely the extraction of the I-V characteristic and the detection bandwidth.

Bibliography

[Almassri et al., 2015] Almassri, A. M., Hasan, W. Z. W., Ahmad, S. A., Ishak, A. J., Ghazali, A. M., Talib, D. N., and Wada, C. (2015). Pressure sensor: State of the art, design, and application for robotic hand. *Journal of Sensors*, 2015.

[Atanackovic and Guran, 2000] Atanackovic, T. M. and Guran, A. (2000). *Theory of Elasticity for Scientists and Engineers*. Birkhäuser Boston, MA, 1 edition.

[Bardeen and Shockley, 1950] Bardeen, J. and Shockley, W. (1950). Deformation potentials and mobilities in non-polar crystals. *Physical Review*, 80.

[Barlian et al., 2009] Barlian, A. A., Park, W. T., Mallon, J. R., Rastegar, A. J., and Pruitt, B. L. (2009). Review: Semiconductor piezoresistance for microsystems. *Proceedings of the IEEE*, 97.

[Becker et al., 2013] Becker, C., Amkreutz, D., Sontheimer, T., Preidel, V., Lockau, D., Haschke, J., Jogschies, L., Klimm, C., Merkel, J. J., Plocica, P., Steffens, S., and Rech, B. (2013). Polycrystalline silicon thin-film solar cells: Status and perspectives. *Solar Energy Materials and Solar Cells*, 119:112–123.

[Bosnell and Voisey, 1970] Bosnell, J. R. and Voisey, U. C. (1970). The influence of contact materials on the conduction crystallization temperature and electrical properties of amorphous germanium, silicon and boron films. *Thin Solid Films*, 6.

[Bossche and Mollinger, 1997] Bossche, A. and Mollinger, J. R. (1997). Calibration procedure for piezoresistance coefficients of polysilicon sheets and application to a stress test chip. *Sensors and Actuators A: Physical*, 62:475–479.

[Cen-Puc et al., 2021] Cen-Puc, M., Schander, A., Vargasgleason, M. G., and Lang, W. (2021). An assessment of surface treatments for adhesion of polyimide thin films. *Polymers*, 13.

[Chang et al., 2020] Chang, Y., Zuo, J., Zhang, H., and Duan, X. (2020). State-of-the-art and recent developments in micro/nanoscale pressure sensors for smart wearable devices and health monitoring systems. *Nami Jishu yu Jingmi Gongcheng/Nanotechnology and Precision Engineering*, 3:43–52.

[Chowdhury et al., 2020] Chowdhury, S., Park, J., Kim, J., Kim, S., Kim, Y., Cho, E. C., Cho, Y., and Yi, J. (2020). Crystallization of amorphous silicon via excimer laser annealing and evaluation of its passivation properties. *Energies*, 13.

[Chuang et al., 2018] Chuang, I., Michael, A., Soeriyadi, A., and Kwok, C. Y. (2018). Aluminum induced crystallization of in-situ phosphorus doped e-beam evaporated silicon films for high gauge factor piezo-resistors. *IEEE Electron Device Letters*, 39.

[Corzo et al., 2020] Corzo, D., Tostado-Blázquez, G., and Baran, D. (2020). Flexible electronics: Status, challenges and opportunities. *Frontiers in Electronics*, 1.

[Crabb and Treble, 1967] Crabb, L. and Treble, C. (1967). Thin silicon solar cells for large flexible arrays. *Nature*, pages 1223–1224.

[Dimova-Malinovska et al., 2006] Dimova-Malinovska, D., Grigorov, V., Nikolaeva-Dimitrova, M., Angelov, O., and Peev, N. (2006). Investigation of structural properties of poly-si thin films obtained by aluminium induced crystallization in different atmospheres. volume 501, pages 358–361.

[Dong et al., 2017] Dong, W., Xiao, L., Hu, W., Zhu, C., Huang, Y., and Yin, Z. (2017). Wearable human-machine interface based on pvdf piezoelectric sensor. *Transactions of the Institute of Measurement and Control*, 39.

[Duan et al., 2013] Duan, C. Y., Ai, B., Li, R. X., Liu, C., Lai, J. J., Deng, Y. J., and Shen, H. (2013). Polycrystalline silicon films on sio2 substrate treated by excimer laser annealing. *Advanced Materials Research*, 750-752:946–951.

[Ferreira and Vasilevskiy, 2006] Ferreira, I. C. and Vasilevskiy, M. (2006). *Física dos Semicondutores - Fundamentos, Aplicações e Nanoestruturas*. Edições Almedina, 1 edition.

[Fiorillo et al., 2018] Fiorillo, A. S., Critello, C. D., and Pullano, A. S. (2018). Theory, technology and applications of piezoresistive sensors: A review. *Sensors and Actuators, A: Physical*, 281:156–175.

[Fortunato et al., 2000] Fortunato, G., Mariucci, L., Carluccio, R., Pecora, A., and Foglietti, V. (2000). Excimer laser crystallization techniques for polysilicon tfts. *Applied Surface Science*, 154.

[French, 2002] French, P. J. (2002). Polysilicon: A versatile material for microsystems. *Sensors and Actuators, A: Physical*, 99:3–12.

[French and Evans, 1989] French, P. J. and Evans, A. G. R. (1989). Piezoresistance in polysilicon and its applications to strain gauges. 32:10.

[Fu et al., 2004] Fu, X., Yao, S., Hou, S., Zhang, W., Zhao, Y., Zhang, S., and Zhang, W. (2004). Simulation and test of a novel soi high temperature pressure sensor. volume 3.

[Gonzalez et al., 2010] Gonzalez, P., Haspeslagh, L., Meyer, K. D., and Witvrouw, A. (2010). Evaluation of the piezoresistive and electrical properties of polycrystalline silicon-germanium for mems sensor applications.

[Grech et al., 2016] Grech, D., Tarazona, A., Leon, M. T. D., Kiang, K. S., Zekonyte, J., Wood, R. J., and Chong, H. M. (2016). Large gauge factor of hot wire chemical vapour deposition in-situ boron doped polycrystalline silicon. *Materials Research Express*, 3.

[Hayzelden and Batstone, 1993] Hayzelden, C. and Batstone, J. L. (1993). Silicide formation and silicide-mediated crystallization of nickel-implanted amorphous silicon thin films. *Journal of Applied Physics*, 73.

[He et al., 2005] He, D., Wang, J. Y., and Mittemeijer, E. J. (2005). Reaction between amorphous si and crystalline al in al/si and si/al bilayers: microstructural and thermodynamic analysis of layer exchange. *Applied Physics A 2004 80:3*, 80:501–509.

[He et al., 2006] He, D., Wang, J. Y., and Mittemeijer, E. J. (2006). Thermodynamic and kinetic criteria for layer exchange in amorphous silicon/crystalline aluminium bilayers during annealing. *Scripta Materialia*, 54:559–561.

[Hiraki, 1983] Hiraki, A. (1983). Low temperature reactions at si/metal interfaces; what is going on at the interfaces? *Surface Science Reports*, 3:357–412.

[hoon Lee et al., 2016] hoon Lee, S., soo Jung, J., soo Lee, S., bo Lee, S., and moon Hwang, N. (2016). Low temperature deposition of polycrystalline silicon thin films on a flexible polymer substrate by hot wire chemical vapor deposition. *Journal of Crystal Growth*, 453.

[Huang et al., 2015] Huang, J., Varlamov, S., Dore, J., Yun, J. S., and Green, M. A. (2015). Microstructural defects in polycrystalline silicon thin-film solar cells on glass by solid-phase crystallisation and laser-induced liquid-phase crystallisation. *Solar Energy Materials and Solar Cells*, 132.

[Huang et al., 2019] Huang, Y., Fan, X., Chen, S. C., and Zhao, N. (2019). Emerging technologies of flexible pressure sensors: Materials, modeling, devices, and manufacturing. *Advanced Functional Materials*, 29.

[Jen et al., 2003] Jen, S. U., Yu, C. C., Liu, C. H., and Lee, G. Y. (2003). Piezoresistance and electrical resistivity of pd, au, and cu films. *Thin Solid Films*, 434:316–322.

[Kanda, 1991] Kanda, Y. (1991). Piezoresistance effect of silicon. *Sensors and Actuators: A. Physical*, 28.

[Kawamoto et al., 2006] Kawamoto, N., Masuda, A., Matsuo, N., Seri, Y., Nishimori, T., Kitamon, Y., Matsumura, H., Hamada, H., and Miyoshi, T. (2006). Grain enlargement of polycrystalline silicon by multipulse excimer laser annealing: Role of hydrogen. *Japanese Journal of Applied Physics, Part 1: Regular Papers and Short Notes and Review Papers*, 45:2726–2730.

[Kazi et al., 2006] Kazi, I. H., Wild, P. M., Moore, T. N., and Sayer, M. (2006). Characterization of sputtered nichrome (ni-cr 80/20 wt.strain gauge applications. *Thin Solid Films*, 515:2602–2606.

[Kervran et al., 2015] Kervran, Y., Sagazan, O. D., Crand, S., Coulon, N., Mohammed-Brahim, T., and Brel, O. (2015). Microcrystalline silicon: Strain gauge and sensor arrays on flexible substrate for the measurement of high deformations. *Sensors and Actuators, A: Physical*, 236.

[Latif et al., 2021] Latif, R., Noor, M. M., Yunas, J., and Hamzah, A. A. (2021). Mechanical energy sensing and harvesting in micromachined polymer-based piezoelectric transducers for fully implanted hearing systems: A review. *Polymers*, 13.

[Lee et al., 1995] Lee, S.-W., Jeon, Y.-C., and Joo, S.-K. (1995). Pd induced lateral crystallization of amorphous si thin films articles you may be interested in. *Cite as: Appl. Phys. Lett*, 66:1671.

[Lenci et al., 2008] Lenci, S., Gonzalez, P., Meyer, K. D., Hoof, R. V., Frederickx, D., and Witvrouw, A. (2008). Determination of the piezoresistivity of microcrystalline silicon-germanium and application to a pressure sensor. *Proceedings of the IEEE International Conference on Micro Electro Mechanical Systems (MEMS)*, pages 427–430.

[Li et al., 2018] Li, J., Bao, R., Tao, J., Peng, Y., and Pan, C. (2018). Recent progress in flexible pressure sensor arrays: From design to applications. *Journal of Materials Chemistry C*, 6:11878–11892.

[Li et al., 2020] Li, M., Liang, J., Wang, X., and Zhang, M. (2020). Ultra-sensitive flexible pressure sensor based on microstructured electrode. *Sensors (Switzerland)*, 20.

[Liu et al., 2020] Liu, J., Zhang, Y., Fan, Z., Sun, H., and Shan, F. (2020). Low-temperature deposition of large-grain polycrystalline si thin films on polyethylene terephthalate. *Thin Solid Films*, 707.

[Liu et al., 2009] Liu, X., Lu, X., Chuai, R., Shi, C., and Suo, C. (2009). Polysilicon nanofilm pressure sensor. *Sensors and Actuators, A: Physical*, 154.

[Liu et al., 2017] Liu, Y., Pharr, M., and Salvatore, G. A. (2017). Lab-on-skin: A review of flexible and stretchable electronics for wearable health monitoring. *ACS Nano*, 11.

[Nast and Hartmann, 2000] Nast, O. and Hartmann, A. J. (2000). Influence of interface and al structure on layer exchange during aluminum-induced crystallization of amorphous silicon. *Journal of Applied Physics*, 88:716–724.

[Nast et al., 2000] Nast, O., Puzzer, T., Chou, C. T., and Birkholz, M. (2000). Grain size and structure analysis of polycrystalline silicon on glass formed by aluminium-induced crystallisation.

[Nast and Wenham, 2000] Nast, O. and Wenham, S. R. (2000). Elucidation of the layer exchange mechanism in the formation of polycrystalline silicon by aluminum-induced crystallization. *Journal of Applied Physics*, 88:124–132.

[Nozawa et al., 1997] Nozawa, R., Takeda, H., Ito, M., Hori, M., and Goto, T. (1997). Substrate bias effects on low temperature polycrystalline silicon formation using electron cyclotron resonance sih4/h2 plasma. *Journal of Applied Physics*, 81.

[Oerke et al., 2014] Oerke, A., König, C., Büttgenbach, S., and Dietzel, A. (2014). Investigation of different piezoresistive materials to be integrated into micromechanical force sensors based on su 8 photoresist. volume 613, pages 244–250. Trans Tech Publications Ltd.

[Patil et al., 2010] Patil, S. K., Çelik Butler, Z., and Butler, D. P. (2010). Piezoresistive polysilicon film obtained by low-temperature aluminum-induced crystallization. *Thin Solid Films*, 519:479–486.

[Patra and Das, 2022] Patra, C. and Das, D. (2022). Room temperature synthesized highly conducting b-doped nanocrystalline silicon thin films on flexible polymer substrates by icp-cvd. *Applied Surface Science*, 583:152499.

[Phan et al., 2014] Phan, H. P., Dao, D. V., Tanner, P., Wang, L., Nguyen, N. T., Zhu, Y., and Dimitrijev, S. (2014). Fundamental piezoresistive coefficients of p-type single crystalline 3c-sic. *Applied Physics Letters*, 104.

[Pier et al., 2008] Pier, T., Kandoussi, K., Simon, C., Coulon, N., Mohammed-Brahim, T., and Lhermite, H. (2008). Excimer laser annealing of microcrystalline silicon. *physica status solidi c*, 5:3234–3238.

[Pihan et al., 2007] Pihan, E., Slaoui, A., and Maurice, C. (2007). Growth kinetics and crystallographic properties of polysilicon thin films formed by aluminium-induced crystallization. *Journal of Crystal Growth*, 305:88–98.

[Qin et al., 2021] Qin, J., Yin, L. J., Hao, Y. N., Zhong, S. L., Zhang, D. L., Bi, K., Zhang, Y. X., Zhao, Y., and Dang, Z. M. (2021). Flexible and stretchable capacitive sensors with different microstructures. *Advanced Materials*, 33.

[Radnoczi et al., 1991] Radnoczi, G., Robertsson, A., Hentzell, H. T., Gong, S. F., and Hasan, M. A. (1991). Al induced crystallization of a-si. *Journal of Applied Physics*, 69.

[Russell et al., 1998] Russell, S. W., Li, J., and Mayer, J. W. (1998). In situ observation of fractal growth during a-si crystallization in a cu3si matrix. *Journal of Applied Physics*, 70:5153.

[Saleh and Teich, 2003] Saleh, B. E. A. and Teich, M. C. (2003). *Semiconductor Photon Detectors*.

[Shi et al., 2018] Shi, J., Wang, L., Dai, Z., Zhao, L., Du, M., Li, H., and Fang, Y. (2018). Multiscale hierarchical design of a flexible piezoresistive pressure sensor with high sensitivity and wide linearity range. *Small*, 14.

[Smith, 1954] Smith, C. S. (1954). Piezoresistance effect in germanium and silicon. *Physical Review*, 94.

[Tibrewala et al., 2007] Tibrewala, A., Peiner, E., Bandorf, R., Biehl, S., and Lüthje, H. (2007). The piezoresistive effect in diamond-like carbon films. *Journal of Micromechanics and Microengineering*, 17.

[Tiwana et al., 2012] Tiwana, M. I., Redmond, S. J., and Lovell, N. H. (2012). A review of tactile sensing technologies with applications in biomedical engineering. *Sensors and Actuators, A: Physical*, 179:17–31.

[Tutashkonko and Usami, 2016] Tutashkonko, S. and Usami, N. (2016). Effects of the si/al layer thickness on the continuity, crystalline orientation and the growth kinetics of the poly-si thin films formed by aluminum-induced crystallization. *Thin Solid Films*, 616:213–219.

[Wang et al., 2015] Wang, J., Chuai, R., Yang, L., and Dai, Q. (2015). A surface micromachined pressure sensor based on polysilicon nanofilm piezoresistors. *Sensors and Actuators, A: Physical*, 228.

[Wortman and Evans, 1965] Wortman, J. J. and Evans, R. A. (1965). Young's modulus, shear modulus, and poisson's ratio in silicon and germanium. *Journal of Applied Physics*, 36.

[Wu et al., 2016] Wu, Z., Li, C., Hartings, J. A., Narayan, R., and Ahn, C. (2016). Polysilicon thin film developed on flexible polyimide for biomedical applications. *Journal of Microelectromechanical Systems*, 25:585–592.

[Yang and Zhang, 2021] Yang, X. and Zhang, M. (2021). Review of flexible microelectromechanical system sensors and devices. *Nami Jishu yu Jingmi Gongcheng/Nanotechnology and Precision Engineering*, 4.

[Yin et al., 2021] Yin, R., Wang, D., Zhao, S., Lou, Z., and Shen, G. (2021). Wearable sensors-enabled human–machine interaction systems: From design to application. *Advanced Functional Materials*, 31.

[Yoon et al., 1997] Yoon, S. Y., Kim, K. H., Kim, C. O., Oh, J. Y., and Jang, J. (1997). Low temperature metal induced crystallization of amorphous silicon using a ni solution. *Journal of Applied Physics*, 82.

[Zhang et al., 2004] Zhang, F., Liu, X., Ni, G., and Du, Y. (2004). Controlled growth of high-quality polysilicon thin films with huge grains on glass substrates using an excimer laser. *Journal of Crystal Growth*, 260:102–108.

[Zhao et al., 2004] Zhao, Y. H., Wang, J. Y., and Mittemeijer, E. J. (2004). Microstructural changes in amorphous si/crystalline al thin bilayer films upon annealing. *Applied Physics A 2003 79:3*, 79:681–690.

[Özmen et al., 2014] Özmen, T., Karaman, M., and Turan, R. (2014). Polysilicon thin films fabricated by solid phase crystallization using reformed crystallization annealing technique. *Thin Solid Films*, 551.

Four point bending fixture

Consider that a force F is evenly applied to the load beams located at $x = A$ and $x = D$ and the support beams are situated at $x = B$ and $x = C$. This fixture leads to a tensile stress on the surface containing the piezoresistors.

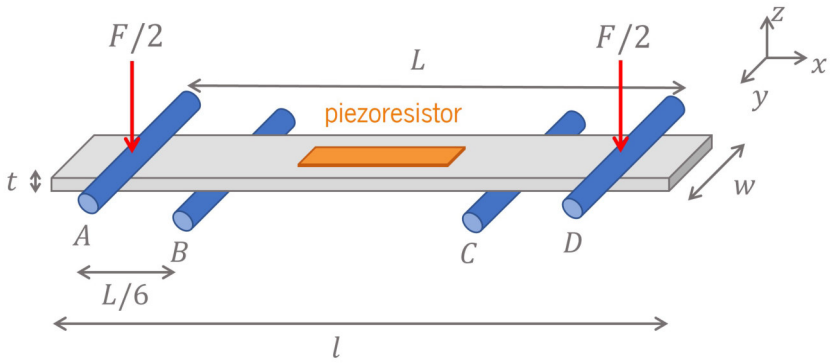


Figure A.1: Illustration of a four point bending set up.

To better understand what happens to the chip containing the piezoresistor, the analysis can be performed on three different sections: from point A to B, from point B to C and from point C to D.

Section A to B

Consider a cross-section at $A < x < B$ represented in Figure A.2. At that point, there will be a shear force and a moment.

Knowing that the region is in static equilibrium, the sum of all forces is null.

$$\sum F = 0 \Leftrightarrow -\frac{F}{2} - V = 0 \Leftrightarrow V = -\frac{F}{2} \tag{A.1}$$

The momentum associated with this force can be obtained knowing that the total momentum is also null.

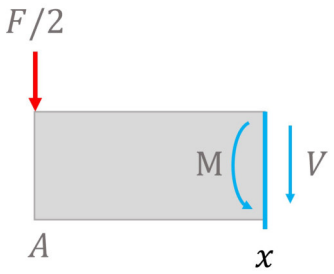


Figure A.2: Schematic of the shear force and momentum in a cross-section between points A and B.

$$\sum M = 0 \Leftrightarrow -\frac{F}{2}x - M = 0 \Leftrightarrow M = -\frac{F}{2}x \tag{A.2}$$

Section B to C

If now the cross-section is performed between points B and C, the sum of all forces is still zero, but now there is an additional contribution associated with the force that the support beam exerts on the chip.

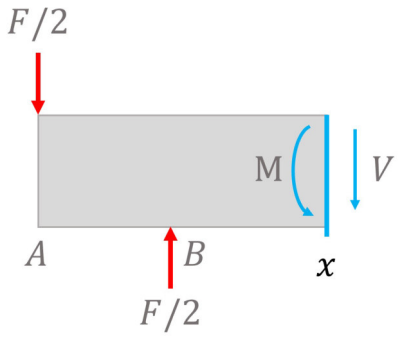


Figure A.3: Schematic of the shear force and momentum in a cross-section between points B and C.

$$\sum F = 0 \Leftrightarrow -\frac{F}{2} + \frac{F}{2} - V = 0 \Leftrightarrow V = 0 \tag{A.3}$$

$$\sum M = 0 \Leftrightarrow -\frac{F}{2}x + \frac{1}{2}F\left(x - \frac{L}{6}\right) - M = 0 \Leftrightarrow M = -\frac{FL}{12} \tag{A.4}$$

Section C to D

Finally, if the cross-section is performed between C and D, the other support beam contributes to the net force with a value of $F/2$ as explicit in (A.5).

$$\sum F = 0 \Leftrightarrow -\frac{F}{2} + \frac{F}{2} + \frac{F}{2} - V = 0 \Leftrightarrow V = \frac{F}{2} \tag{A.5}$$

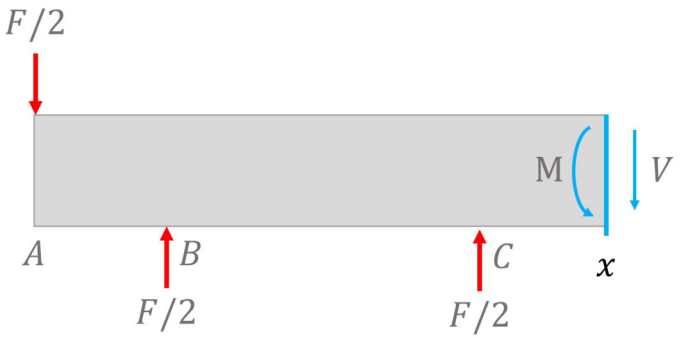
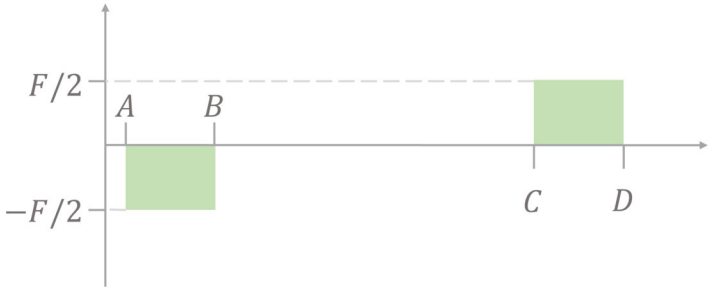


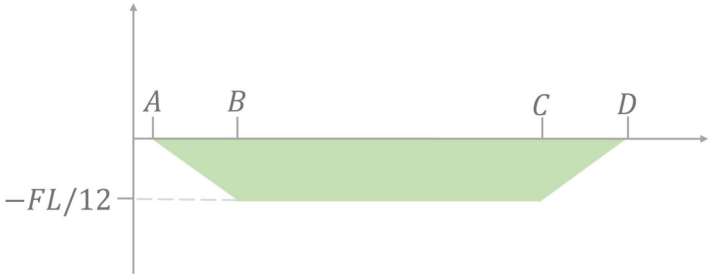
Figure A.4: Schematic of the shear force and momentum in a cross-section between points C and D.

$$\sum M = 0 \Leftrightarrow -\frac{F}{2}x + \frac{1}{2}F\left(x - \frac{L}{6}\right) + \frac{1}{2}F\left(x - \frac{5L}{6}\right) - M = 0 \Leftrightarrow M = -\frac{1}{2}\left(FL - Fx\right) \tag{A.6}$$

By connecting the results for the shear force and the moment in all regions, it is possible to plot the shear force and moment diagrams illustrated in Figure A.5



(a)



(b)

Figure A.5: (a) Shear force and (b) Moment diagrams from point A to D in the bending fixture.

The moment diagram evidences the area of the chip situated between the support beams at $x = B$ and $x = C$, is subjected to a constant moment with the maximum value of $FL/12$.

The stress on a surface is related to the bending moment by Equation A.7.

$$\sigma = -\frac{M(x) \cdot z}{I} \tag{A.7}$$

Here z is the distance between the piezoresistor and the neutral plane. The moment of inertia,I of a rectangular cross-section is given by

$$I = \frac{wt^3}{12} \tag{A.8}$$

Substituting (A.8) in (A.7), the stress in the section B to C is maximum can be written as:

$$\sigma_{max} = \frac{\frac{FL}{12} \cdot \frac{1}{2}}{\frac{wt^3}{12}} = \frac{FL}{2wt^2} \tag{A.9}$$

From the Hooke's Law (see (2.3)), the strain in the piezoresistors is given by (A.10).

$$\varepsilon = \frac{\sigma}{Y} = \frac{FL}{2Ywt^2} \tag{A.10}$$

Layout of test devices - Piezoresistors Mask

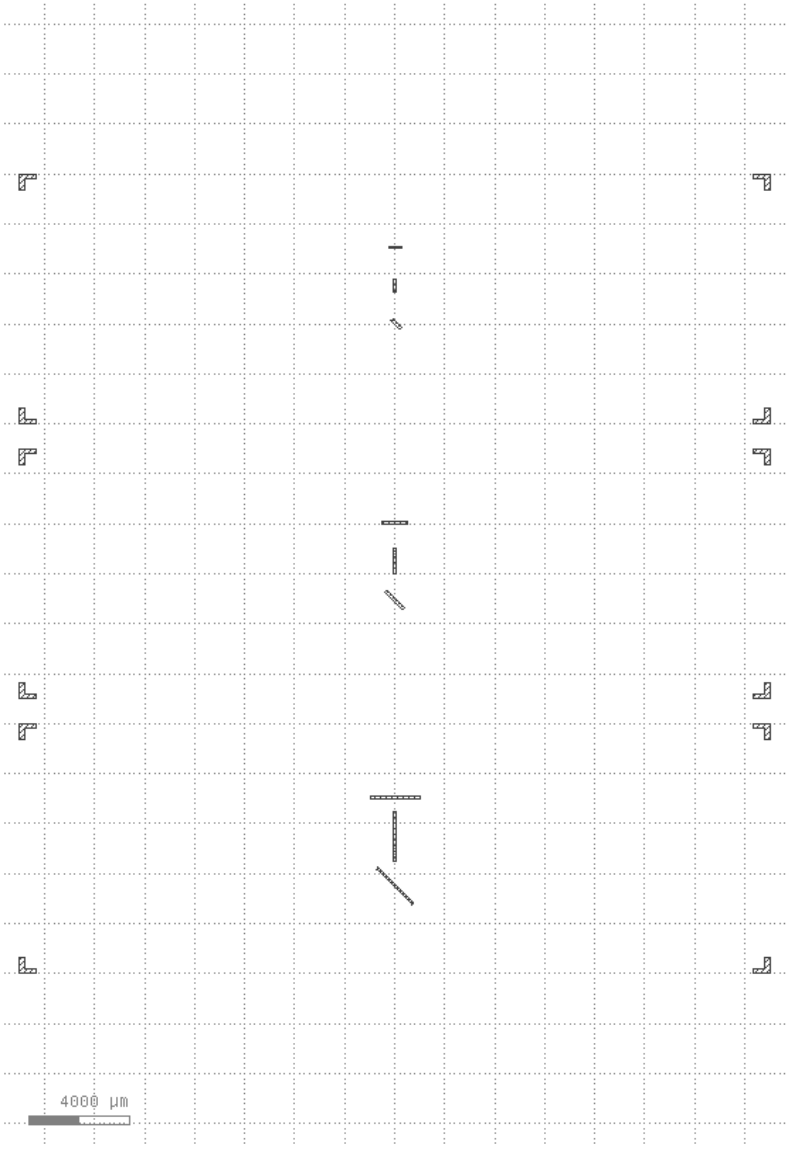


Figure B.1: Layout of the piezoresistors and boundaries of the device.

Layout of test devices - Conductive paths Mask

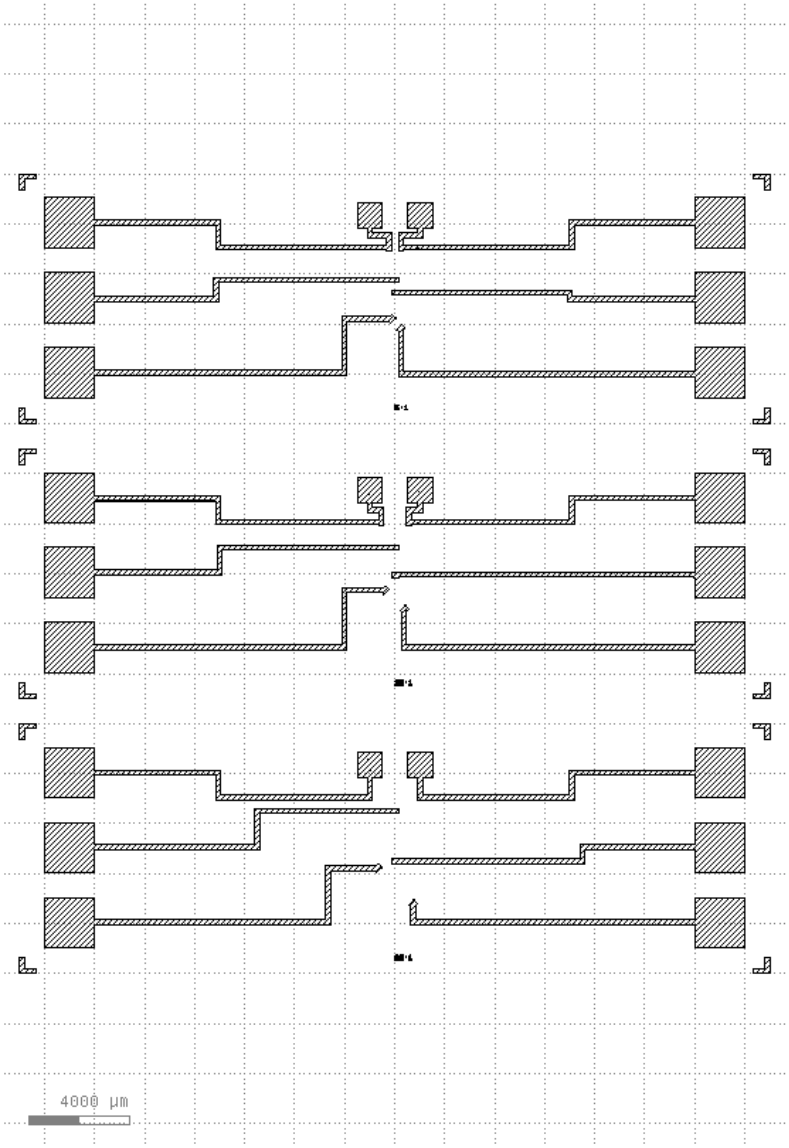


Figure C.1: Layout of the conductive channel connecting the resistors and boundaries of the device.

Layout of test devices - Isolation layer Mask

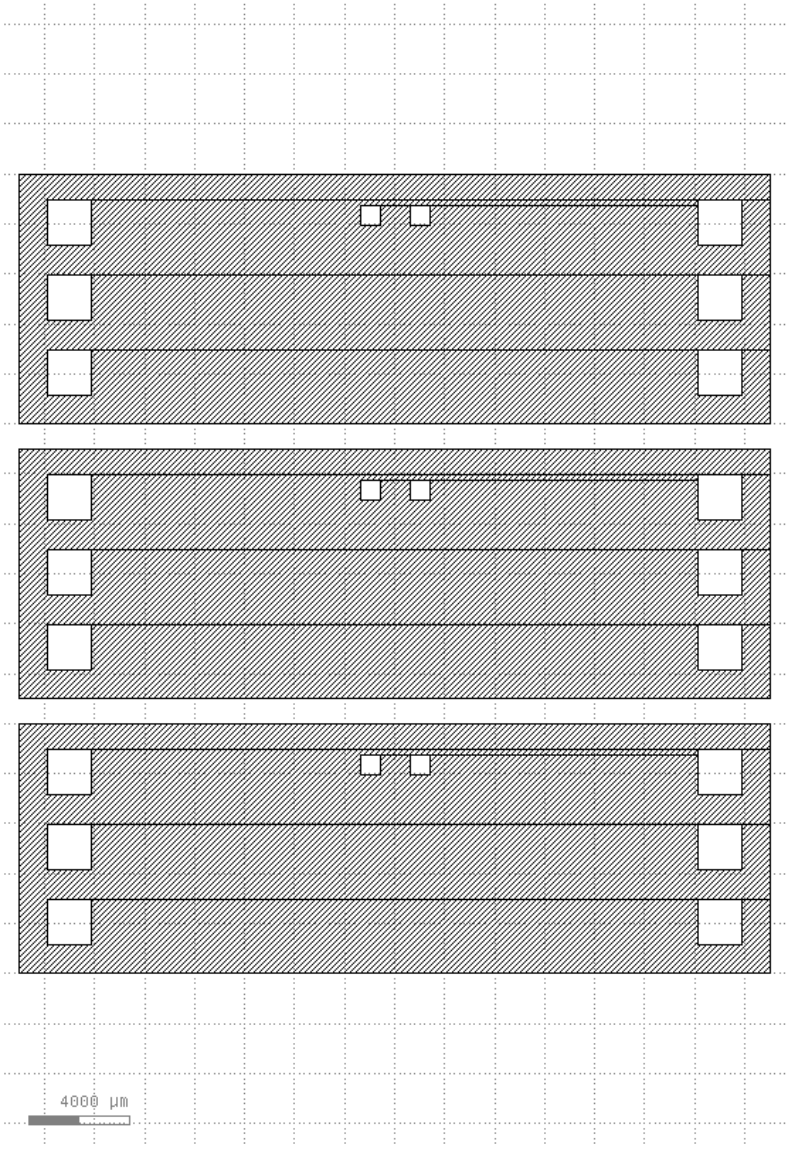


Figure D.1: Layout of the isolation layer.

Layout of test devices - Backside layer Mask

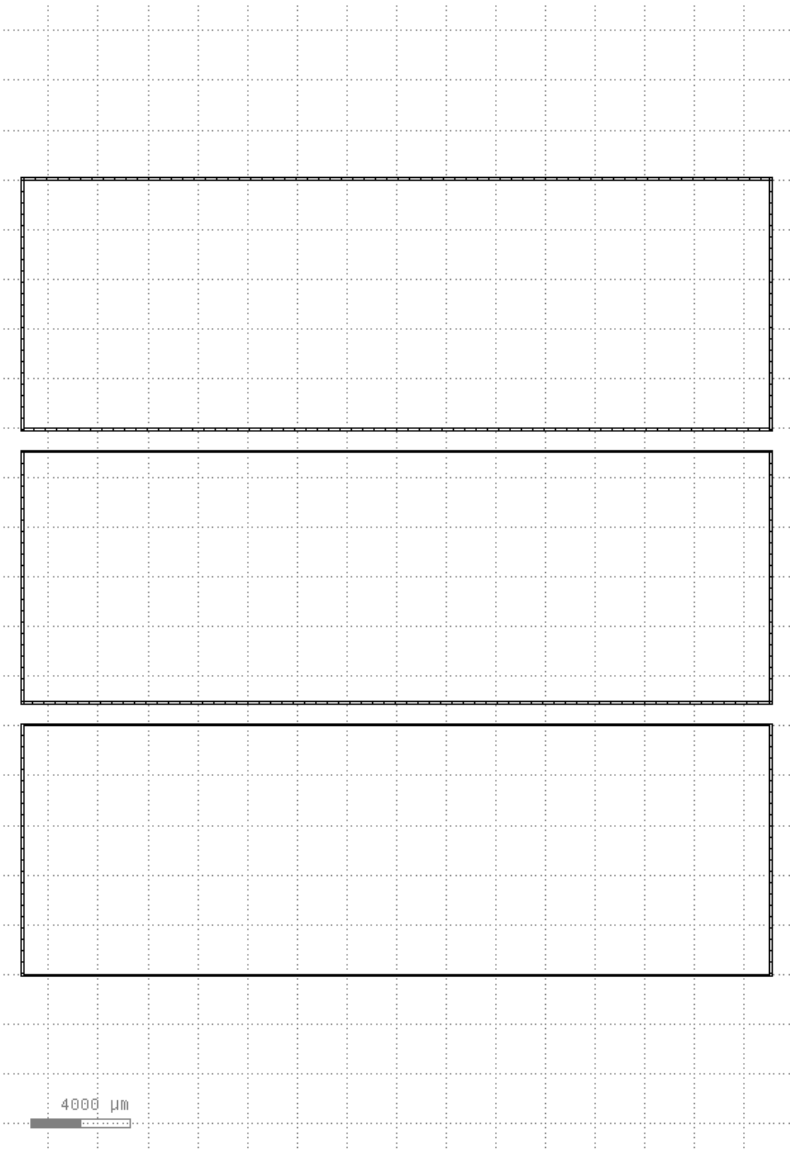


Figure E.1: Layout of the layer used to etch the backside of the wafer to release the devices.