University of Minho
School of Engineering

Tiago Rafael Marques Pereira

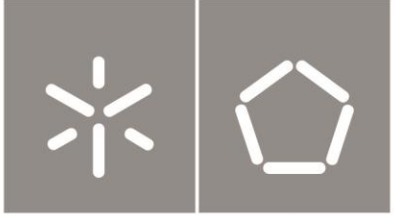
Graphene Transistor Integration in Flexible and Transparent Substrates for Optogenetic Neural Interfaces

January 2024

Graphene Transistor Integration in Flexible and Transparent Susbtrates for Optogenetic Neural Interfaces

Tiago Rafael Marques Pereira

UMinho | 2024



University of Minho
School of Engineering

Tiago Rafael Marques Pereira

Graphene Transistor Integration in Flexible and Transparent Sustrates for Optogenetic Neural Interfaces

Master's Dissertation
Master's in Engineering Physics
Devices, Microsystems and Nanotechnologies

Dissertation supervised by
Professor João Pedro Santos Hall Agorreta Alpuim
Professor Luís Ricardo Monteiro Jacinto

January de 2024

COPYRIGHT AND TERMS OF USE FOR THIRD-PARTY WORK

ACKNOWLEDGMENTS

I sincerely thank my supervisors Dr. Pedro Alpuim and Dr. Luís Jacinto for the continuous mentorship during this work. Their distinct knowledge and guidance allowed me to achieve better results and significantly improve my critical thinking and problem-solving skills, pushing me to be a better student, scientist and engineer.

I extend my acknowledgments to the NeuralGRAB project funded by “la Caixa” Foundation, for the opportunity of working in an enriching, multidisciplinary and relevant project.

I would like to particularly thank Mafalda and Jérôme for their time and patience in aiding me during experiments and the shared knowledge during the development of this work at INL. I extend my gratitude towards all of the 2DMD past and current members, without which the time spent working would not have been as productive, enriching, or even fun. Specially to my friends Gabriel and Vicente, with whom I closely shared the struggles of doing a master thesis, a deep thank you – we did it!

I am grateful for my friends and the memories we share. A special thank you to my “TekkenLab” friends that shared the adventure of graduating in Engineering Physics with me. I also deeply thank Clara for being the kind and supportive girlfriend I needed. Without them it would not have been as easy, nor fun. Finally, I express my deepest gratitude towards my parents, for always providing me with the resources I needed to finish my studies and become the person I am, and my sister, to whom I aspire to be a role model she can pursue and overtake.

FUNDING - The work included in this dissertation was performed in the International Iberian Nanotechnology Laboratory (INL) and the Faculty of Medicine of the University of Porto (FMUP). Financial support was provided by "la Caixa" Banking Foundation under grant agreement LCF/PR/HR21-00410.

STATEMENT OF INTEGRITY

I hereby declare having conducted this academic work with integrity.

I confirm that I have not used plagiarism or any form of undue use of information or falsification of results along the process leading to its elaboration.

I further declare that I have fully acknowledged the Code of Ethical Conduct of the University of Minho.

University of Minho, Braga, January 2024

Tiago Rafael Marques Pereira

RESUMO

Integração de Transístores de Grafeno em Substratos Flexíveis e Transparentes para Interfaces Neuronais Optogenéticas

As doenças do cérebro têm vindo a demonstrar prevalência a nível global. Como tal, perceber e tratar tais doenças é fundamental. As interfaces neuronais são cruciais para se perceber como o cérebro funciona e como as suas doenças podem ser eficientemente tratadas. O grafeno, devido à sua biocompatibilidade, flexibilidade e transparência, emerge como um material adequado para interfaces neuronais, tendo já encontrado aplicação na aquisição de sinais elétricos do cérebro. Este pode também ser modificado de forma a atuar como um sensor químico, demonstrando grande sensibilidade e seletividade, características relevantes para deteção de neurotransmissores. Para além disso, a transparência de materiais como o grafeno é benéfica em aplicações optogenéticas, que permitem o controlo do cérebro com luz. No entanto, o uso do grafeno em larga escala enfrenta problemas devido ao seu processo de transferência lento e ineficiente, o que levanta obstáculos à sua transição desde um material experimental para um largamente acessível. Assim, neste projeto investigou-se a fabricação de um dispositivo à base de grafeno capaz de deteção neuroquímica, com díodos emissores de luz micrométricos incorporados para estimulação optogenética em substrato biocompatível e flexível, como a poliimida. Simultaneamente, explorou-se uma forma eficiente e económica de transferir o grafeno para óxido de silício e poliimida. Um desenho e fabrico de transístores de grafeno em poliimida foi desenvolvido e parcialmente testado, incorporando várias técnicas de microfrabricação. Foi ainda desenvolvido um processo para a montagem de díodos emissores de luz micrométricos em cima do substrato fabricado, testando duas abordagens distintas envolvendo soldadura e resinas condutoras. Finalmente, um processo de transferência de grafeno a seco foi explorado, utilizando álcool polivinílico como um polímero de suporte aplicado por diferentes técnicas, e analisando a forma como pontos de nucleação, fronteiras de grão e a orientação cristalográfica dos grãos subjacentes influenciam o desacoplamento desde o substrato de crescimento. Em resumo, este projeto de tese aborda o desenvolvimento de um sensor neuroquímico flexível à base de grafeno com díodos emissores de luz micrométricos integrados para estimulação optogenética, usando métodos de fabrico económicos e pré-estabelecidos.

Palavras-chave: interfaces neuronais, sensor de grafeno, microfabricação, díodos emissores de luz mcirométricos, transferência seca.

ABSTRACT

Graphene Transistor Integration in Flexible and Transparent Substrates for Optogenetic Neural Interfaces

Brain disorders are increasingly prominent globally, thus understanding and treating such conditions are paramount. Neural interfaces are crucial for understanding the brain's functioning and how disorders can be efficiently treated. Graphene, due to its biocompatibility, flexibility, and transparency, is an emerging material for neural interfaces. It has already found application in the recording of electrical information from the brain. It has also shown that it can be modified as a chemical sensor with exceptional sensitivity and selectivity, which is relevant for neurotransmitter detection. Additionally, the transparency of materials like graphene proves highly advantageous in optogenetic applications, enabling brain activity control with light. Nevertheless, graphene's large-scale use faces drawbacks due to its slow and inefficient transfer processes, which hinder the transition from an experimental material to a widely available one. As such, in this project, one worked towards the fabrication of a graphene device capable of neurotransmitter detection, with incorporated micron-sized light emitting diodes for optogenetic stimulation, on top of a biocompatible and flexible substrate such as polyimide. At the same time, a more effective and inexpensive way of transferring graphene to silicon oxide and polyimide was explored. A fabrication process and layout for graphene field-effect transistors on a polyimide substrate were designed and partially tested, encompassing various microfabrication techniques. Additionally, a process for mounting micron-sized light emitting diode chips on top of the fabricated substrate was developed and tested by two approaches involving soldering and conductive resins. Finally, a dry transfer of graphene was explored, using polyvinyl alcohol as a support polymer applied by different techniques, and analyzing how nucleation sites, grain boundaries, and the underlying crystallographic grain orientation influenced the decoupling from the growth substrate. In summary, this thesis project addresses the development of a flexible graphene-based neurochemical sensor with integrated micron-sized light emitting diodes for optogenetic stimulation, using inexpensive and already established methods for its fabrication.

Keywords: neural interface, graphene sensor, microfabrication, micro-LEDs, dry transfer

CONTENTS

List of Abbreviations and Acronyms

ChR2	Channelrhodopsin
CVD	Chemical Vapor Deposition
DI	De-ionized
EDL	Electrical Double Layer
EVA	Ethylene Vinyl Alcohol
FCC	Face Centered Cubic
GFET	Graphene Field-Effect Transistor
IPA	Isopropanol
LOD	Limit of Detection
µLED	Micron-sized Light Emitting Diode
NpHR	Halorhodopsin
NI	Neural Interface
noOxGr	CVD graphene grown on non-pre-oxidized Cu substrate
OM	Optical Microscope
OxGr	CVD graphene grown on pre-oxidized Cu substrate
PECVD	Plasma-enhanced Chemical Vapor Deposition
PEN	Polyethylene Naphthalate
PET	Polyethylene Terephthalate
PF	Pole Figure
PI	Polyimide
PVA	Polyvinyl Alcohol
PMMA	Polymethyl Methacrylate
RIE	Reactive Ion Etching
SEM	Scanning Electron Microscope
SNR	Signal-to-Noise Ratio
UHV	Ultra-High Vacuum
UV	Ultraviolet
XRD	X-Ray Diffraction
ZIF	Zero-insertion Force

LIST OF FIGURES

LIST OF TABLES

1. Introduction and Motivation

The brain has been a matter of study throughout human history. Although progress has been made in understanding it, there is still a lot to unveil, and our knowledge probably only scratches the tip of the iceberg. With technological and scientific development, humanity has been able to create progressively more complex tools to probe the physiology of the brain in such a way that allows for a deeper understanding of its inner workings. The human brain is a complex organ comprising roughly 86 billion neuron cells [1], [2] that process and communicate information via electrochemical signals with each other, reaching up to trillions of connections. The transmission of information between neurons is done at the synapse, where specialized molecules called neurotransmitters are typically released in tiny quantities to signal to the next neuron "what to do." Abnormal concentrations or activity of these molecules in the brain have been linked to several neurological disorders, such as Parkinson's [3], [4], or Alzheimer's disease [5], which are very prevalent in the global population. As such, there is a great interest in understanding and studying potential correlations between neurotransmitters' dynamics and these diseases to potentiate the development of new diagnostics, therapeutics, and even cures for these disorders.

Neural Interface (NI) tools allow brain physiology study by bridging the brain and external electronics where one can acquire, decode, process, and send information, even allowing for back-and-forth communication [6]. Neural Interfaces (NI) should be sensitive to allow for detection of subtle brain dynamics, reliable for long term operation, small and biocompatible to minimally disrupt the brain and subject's normal functioning and behavior. These aspects are critical in determining the performance of these devices. Different types of NIs can operate in the interior or exterior of the brain. The former allows for more sensitive and localized operation of the devices than the latter, at the expense of more complex and dangerous implantation procedures and enhanced invasiveness. Different challenges, be it their biocompatibility, biological integration, or minimally damaging the surrounding tissue can be assessed by adequate choice of materials in implantable NIs. These should not present degradation and induce immune responses from the subject's body. Chemical inertness in a biological medium and mechanically matching the surrounding tissue's properties are crucial to achieve biocompatibility. Consequently, there is a special interest in incorporating one or more modalities for recording or modulation of brain activity in flexible devices. NIs can read or stimulate brain signals via different electrical, optical, and

pharmaceutical methods. Optogenetics is an optical brain modulation modality that enables control of brain behavior by exposing genetically modified brain tissue to light. This requires a light source that can be integrated in the NI, for example, in the form of micron-sized light-emitting diodes (μLED) [7], [8]. It can be combined with other recording modalities. Although recording of brain activity is typically associated with its electrical component, the neurochemical activity can also be studied with chemical sensing methods. These methods require high sensitivity due to the reduced amounts of target chemicals, the neurotransmitters. High selectivity is also paramount as multiple similar molecules can be present while presenting distinct functionality.

The high complexity of the brain and the challenges associated in studying it push for the development of better NIs This opens the way for new functional materials and techniques to enter this research field, including the one-atom-thick conductive material graphene. Graphene has been a focus of study over the past ten years. The emergence of a reliable fabrication technique for graphene on top of metallic catalyst substrates boosted research and development of different applications. Graphene has been used to fabricate a wide range of sensors due to its outstanding electrical properties. It proved reliable when it comes to chemical detection of a diverse range of substances, ranging from gases to liquids, while also showing high sensitivity and selectivity upon surface chemical modification, known as functionalization. Furthermore, graphene is transparent, chemically inert, and biocompatible, making it an optimal candidate for usage in NIs [9]. In a recent study, ultrasensitive detection of dopamine, an important neurotransmitter, in cerebral spinal fluid, utilizing functionalized graphene field-effect transistors (GFET) [10] was demonstrated, reaching an attomolar limit of detection (LOD). This result paved the way for integrating this technology into a single flexible biocompatible device capable of being implanted, as in [11]. These studies established graphene as a material capable of sensitive and selective reading of neurochemical activity while implanted in a living being. An integration of graphene-enabled recording of neurochemical signals with a brain modulating modality in a single device is still yet to be accomplished. Furthermore, the accessibility, manufacturing cost, and reliability of such devices should be considered if one aims to mass produce and make such a technology widely available. One of the biggest challenges in the scalability of graphene-based devices is the complex and expensive transfer methods utilized to transfer graphene from the metal catalyst, where it is usually grown, onto the final substrate. Generally used transfer methods require the etching of the metal catalyst, typically copper. Waste is generated and non-environmentally friendly chemical solutions are required, which, in addition to raising manufacturing costs, can dope the graphene, altering its electronic properties and generating non-removable residues. Different kinds of approaches to graphene transfer have been a matter of research [12], [13], with one

of them being the direct detachment of this material from the substrate without etching of the metal catalyst [14]. This would allow for mass transfer methods, for example, with roll-to-roll technology [15], while maintaining lower doping and residues' levels than traditional transfer methods and the possibility to re-use the catalyst, hence lowering fabrication costs.

With all of this in mind, the main goal of this dissertation was the definition of a fabrication process of a non-implantable flexible device with GFETs capable of being chemically modified for the detection of dopamine in real biological samples while at the same time integrating μLEDs for optical modulation of neuronal activity. Furthermore, a dry transfer method of graphene was explored, and its feasibility studied. All these objectives were framed inside the project NeuralGRAB: Graphene Aptasensor Bioelectronics, a neural interface for neurotransmission probing in neurological disorders, and contribute to its development. A rigid GFET-based neurochemical sensor for dopamine has already been established inside the NeuralGRAB project. Development of an implantable version with capabilities of brain activity modulation is one of project's ultimate goals. In this work, the integration of the GFET-based neurochemical sensor was translated onto a flexible substrate. Integration of optical modulation capabilities provided by μLEDs were also studied. This master thesis project thus provides a crucial step between the rigid GFET devices [10] and a fully integrated biocompatible, flexible, and implantable platform for neurochemical sensing in a living brain with optical stimulators.

2. STATE OF THE ART

2.1 GFET Flexible Biosensors

The outstanding graphene's electrical properties make this material suitable for a number of applications. The development of large-scale growing methods on metallic catalysts made this material increasingly available. Interesting applications have been found in the biosensing field, enabling highly sensitive detection of biomolecules of interest.

2.1.1 Graphene

Graphene is a transparent, conductive material comprised of a layer of sp^2-hybridized carbon atoms (Figure 1b) arranged in a honeycomb structure with a theoretical thickness of only 0.335 nm [16]. It is an allotrope of carbon, with each carbon atom connected by three σ-bonds to the nearest neighbors, each bond spanning about 0.142 nm, while graphene's lattice parameter is about 0.246 nm, with each primitive cell comprising two atoms [17], [18] (Figure 1a). Each carbon atom forms one π-bond with its first neighbors, using the unpaired p_z electrons (Figure 1d), giving rise to the π- and π*-bands, the valence and conduction bands, respectively. It is a zero-bandgap semiconductor, with the valence and conduction bands touching at the K and K' points named the Dirac points. Electrons with energy in a range close (≈ 1 eV) to this singularity behave as massless Dirac fermions [19], with an effective Fermi velocity, v_F≈10^6 $m.s^{-1}$ [20]. A linear electron energy-momentum dispersion relation is observed in this region, which is very similar for both bands, originating the cones in the Brillouin zone near the K and K' points (Figure 1d). Graphene possesses remarkable electronic properties [21], such as high charge carrier mobility (μ) that can be maintained at high temperatures (300 K) and high electric fields, with a pseudospin quantum number, low intrinsic electronic noise, chemical stability, and high sensitivity to electric charges and dipoles in its proximity. It is also deemed transparent, absorbing less than 3% of visible light [22], [23], [24] (Figure 1c).

One of the most prominent techniques for graphene characterization is Raman spectroscopy. Graphene's quality and number of layers can be assessed mainly by the measurement of three distinct peaks: the D peak, at 1350 cm^{-1}, the G peak, at 1580 cm^{-1}, and the 2D peak at 2700 cm^{-1}. The G peak arises from a first order Raman scattering process involving one optical phonon whilst the D and 2D peaks arise from second order processes. The D peak is associated with a second order process involving an in-plane

transverse optical phonon and a defect and, as such, is associated with the defect density of graphene. Meanwhile, the 2D peak is associated with two in-plane transverse optical phonons near the K point and is typically associated with the number of graphene layers (when compared to the G peak).

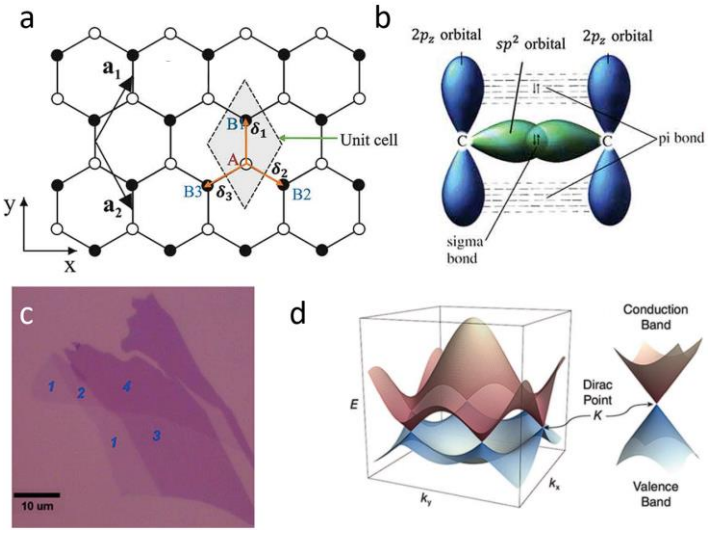


Figure 1 – Graphene properties.
(a) Schematic representation of graphene structure. Vectors a_1 and a_2 represent the two primitive vectors with an amplitude of 0.246 nm and δ vectors represent the sigma bonds connecting neighboring carbon atoms. (b) Representation of the electronic clouds around the carbon atoms in graphene. (c) Image of different numbers of graphene layers transferred onto a 285 nm thick SiO2 substrate under the microscope. The numbers represent the number of graphene layers in each area. An increase in the number of graphene layers leads to less light transmission. (d) Representation of graphene's band structure where multiple Dirac Cones are visible (left). Detail of band structure near the Dirac point and linear behavior of the energy-momentum dispersion relation (right). (a),(b) adapted from [25], (c) adapted from [26], (a),(b) adapted from [27].

2.1.2 Graphene Growth

Although graphene had long been theorized, it was first achieved by mechanical exfoliation from highly oriented pyrolytic graphite [28] using Scotch tape. However, this method lacked scalability and reproducibility. Since then, various methods have emerged that can be labeled bottom-up or top-down [29].

One can name mechanical or chemical exfoliation and chemical synthesis from graphite or its derivatives within top-down methods. As already mentioned, the first was the first-way isolated graphene was obtained. Typically, exfoliation methods rely on the fact that graphite is comprised of graphene sheets bonded by Van der Waals force. Graphene can be successfully isolated if one breaks these weak bonds (Figure 2a). Mechanical methods rely on applying a normal or parallel (shear) force to the graphene sheets' plane. In contrast, chemical methods try to intercalate molecules between graphene sheets to weaken the Van der Waals bond [30]. Chemical synthesis methods from graphite or its derivatives are helpful if one aims to obtain non-pure forms of graphene, such as graphene oxide, that can be used to

form reduced graphene oxide [31]. By starting with graphite and then applying strong acids or oxidants that alter the graphene sheets' chemistry, making them hydrophilic or intercalating molecules between them, they can more easily separate by sonication.

Bottom-up methods include a variety of methods for graphene growth. Some examples are the epitaxial growth on SiC substrates and chemical vapor deposition (CVD) growth, which can be plasma-enhanced to lower the growth temperature.

Epitaxial growth on SiC substrates is achieved by heating the substrate to a point where silicon atoms start to be desorbed from the bulk material, leaving behind carbon atoms that form graphene sheets (Figure 2b). This technique can be applied in ultra-high vacuum (UHV) or at ambient pressure, resulting in a higher ratio of monolayer graphene in the latter due to a more well-controlled Si sublimation rate. Also, this technique is well-suited for integration in the widely established complementary metal-oxide-semiconductor fabrication, as it can be used to grow graphene directly in the substrate where it will be utilized, provided high temperatures achieved during growth can be endured [32], [33], [34].

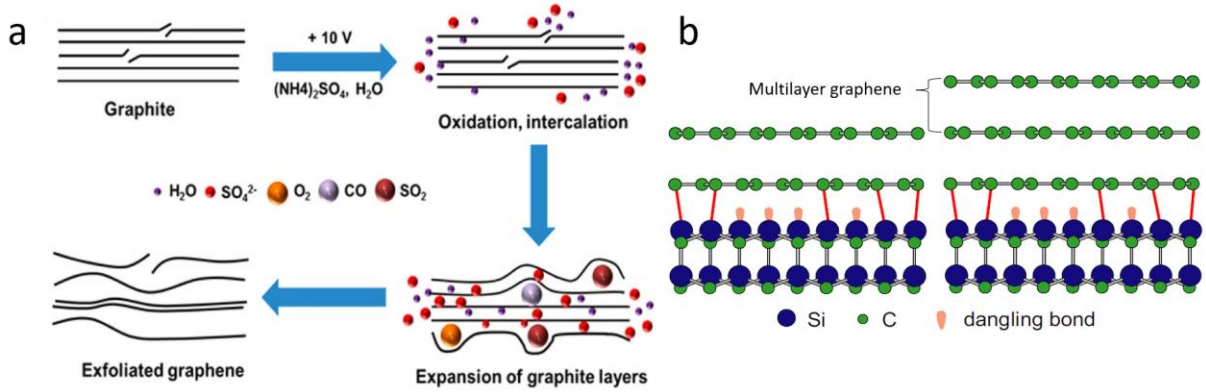


Figure 2 – Graphene exfoliation and epitaxial growth on SiC.
(a) Schematic representation of electrochemical exfoliation. Molecules in an electrolyte solution intercalate between the graphene sheets in graphite due to an applied potential between the graphite and another immersed electrode. [30] (b) Proposed mechanism for forming a bilayer of graphene by thermal decomposition of SiC. [34]

CVD growth has a high yield and can produce high-quality large-area graphene sheets. Here, graphene is grown on top of a substrate capable of adsorbing carbon, allowing other carbon atoms to attach to these nucleation sites and make the graphene grow laterally [35], [36], [37]. Using plasmas can decrease the temperature needed for the growth process to begin while also shortening the growth time. Typical substrates for this type of growth are metallic ones, such as the most widely used Cu [38] and Ni [37]. At the same time, others can also be used, such as Co, Pt, Ir, and Ru, among others [35], although graphene can be grown on top of other kinds of substrates like hexagonal boron nitride [39]. This process can be divided into four crucial steps: substrate pre-treatment, annealing, graphene growth, and cooling. The growth mechanism differs on Ni and Cu substrates as these two materials possess very different

carbon solubilities, with the latter material presenting a magnitudes lower solubility [40]. In both substrates, the process can be described as an initial transport of the reactants onto the chamber, followed by a vapor-phase reaction where carbon species are formed.

Ni substrate's growth mechanism is usually described as a saturation and segregation/precipitation process. Here, after hydrocarbons are pumped inside the CVD chamber and carbon atoms diffuse inside the bulk Ni, they saturate and are segregated from the bulk material onto the surface and precipitated at the grain boundaries when the chamber temperature is lowered [37]. This process then realizes the growth of mono to multilayers of graphene.

As for Cu substrates, carbon atoms are adsorbed onto the catalyst's surface, where on-surface reactions form active species that eventually overcome the energy barrier to begin nucleation. The subsequent formation of active carbon species can help the growth of already-formed nuclei or start new ones [41]. As Cu solubility is very low for carbon, the graphene growth process occurs only at the surface, where carbon atoms from hydrocarbon precursors attach to the available nucleation sites and seed the growth. This process usually occurs at temperatures higher than those required for Ni substrates. Cu reaches a semi-molten state at temperatures close to its melting point (1085 °C) or lower for higher impurity Cu samples. Here, the process is self-limiting. Once the surface is completely covered with graphene, nucleation cannot occur, resulting in a higher yield of monolayer graphene on this type of substrate. If too many nucleation sites are available, the graphene will have a small crystallite size, typically presenting higher defect density and a higher number of graphene layers around the nucleation sites [42]. The nucleation sites can be defects on the Cu surface or even deleterious carbon residues. These can be reduced by electro-polishing the substrate and oxidizing it in a pre-growth cleaning stage. Electro-polishing lowers Cu substrate roughness, reducing the number of nucleation sites, and pre-oxidizing stores oxygen inside of the substrate that will be released during heating and scavenge deleterious carbon [43] that could otherwise serve as a nucleation site [44].

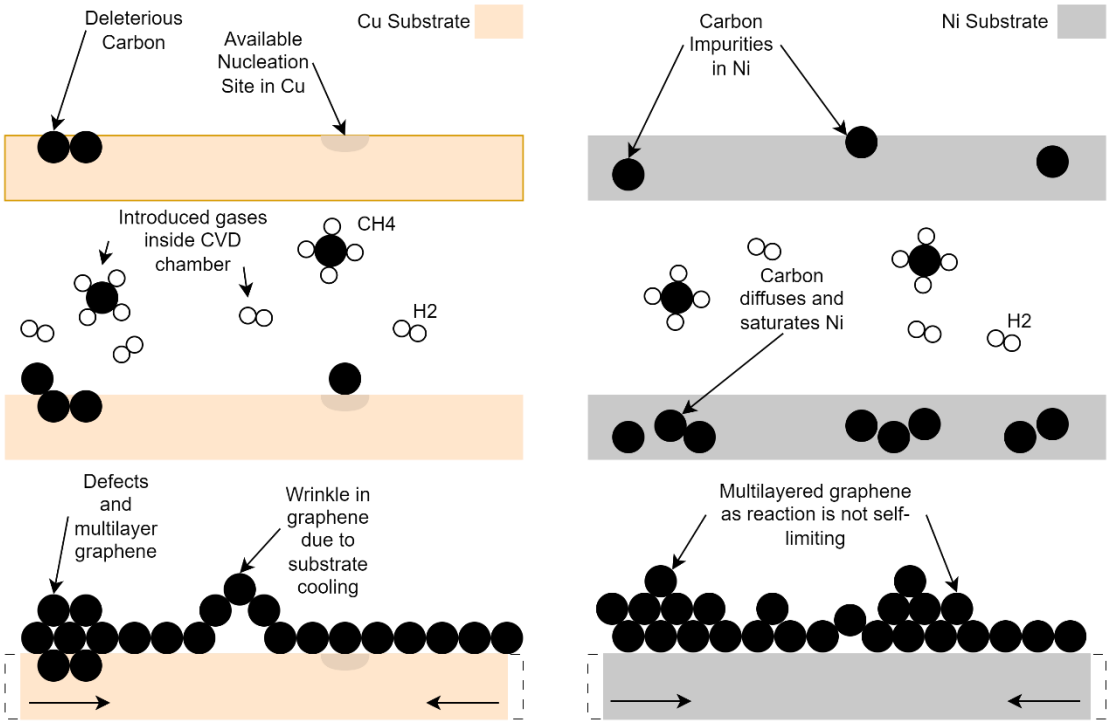
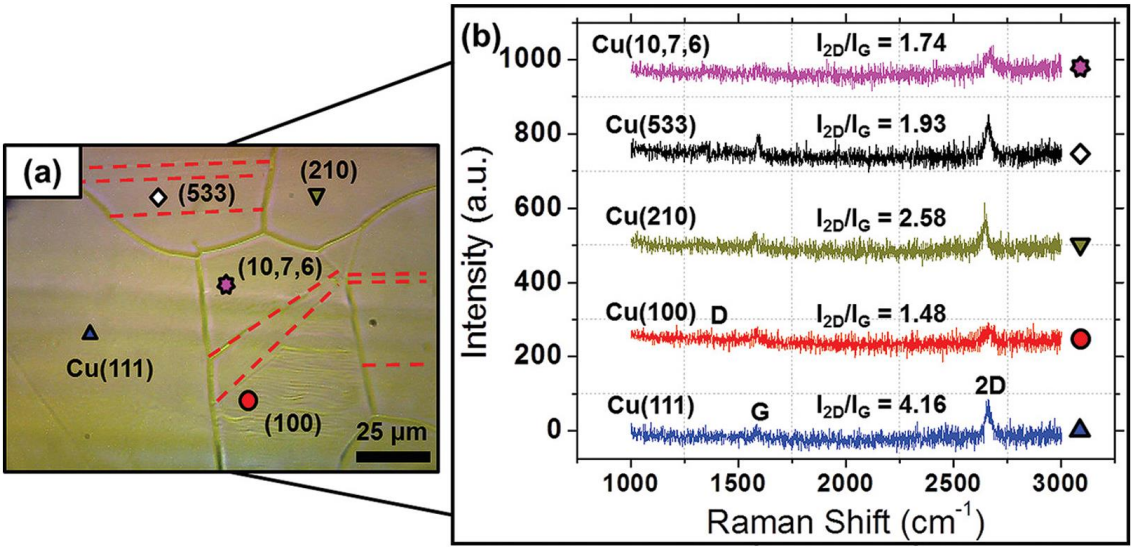


Figure 3 – Schematic representation of the different growth processes for CVD graphene in a Cu and Ni substrate.
(Left) CVD growth on Cu is a self-limiting process yielding mostly monolayer graphene, while on (Right) Ni, it relies on a saturation and precipitation/aggregation process.

Crystal facets of the metallic substrate can also play a role in the quality of the CVD-grown graphene, and it has been shown that specific orientations yield higher quality and faster growth. For example, Cu(111) crystals [45] have been shown to lead to higher-quality monolayer graphene sheets (Figure 4a). At the same time, graphene has been thought to induce a recrystallization of the Cu substrate (Figure 4b) into preferably Cu(100), shown by fast cooling CVD grown graphene on copper foils and comparing them to slow-cooled samples that exhibited larger grain Cu(111) formation (A. Y. Lu et al., 2012).



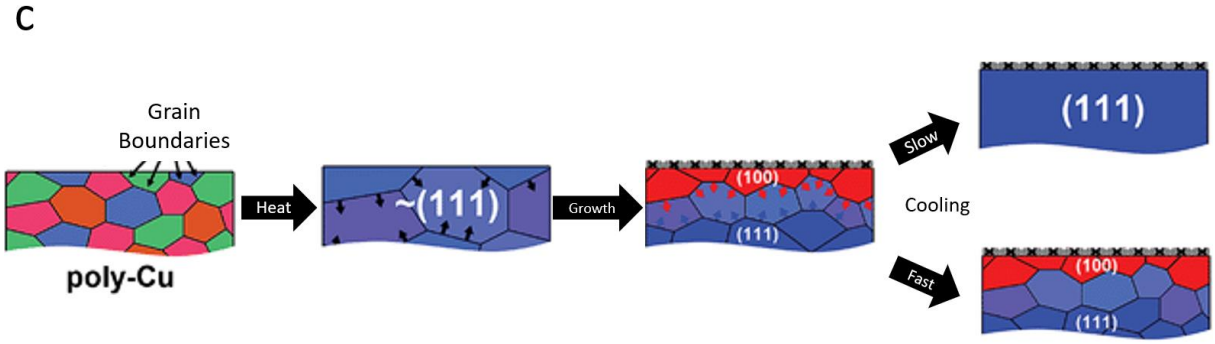


Figure 4 – Effect of Cu substrate crystallographic orientation on graphene quality and its evolution during CVD growth of graphene.
(a) Optical image of graphene grown on Cu substrate with different crystal facets and (b) the corresponding Raman spectrum. The I_{2D}/I_G ration on Cu(111) is higher, which indicates a better quality monolayer graphene sheet. (c) Schematic of the recrystallization process for Cu substrates in the CVD graphene growth process. Different colors represent different grain crystal orientations. Graphene induces a (100) recrystallization at the surface, shown by a tendency of small Cu(100) crystal facets to appear after fast cooling. In contrast, millimeter-sized Cu(111) crystals are formed upon slow cooling of the samples after the CVD growth process.

2.1.3 Graphene Transfer

Over the last decade [12], one of the biggest challenges in the large-scale use of graphene is the difficulty and cost associated with its transfer from its native substrate onto the substrate where one wants to utilize it. The transfer process is associated with decreasing graphene quality by introducing defects such as cracks, wrinkles, tears, or even doping the graphene. Although there have been efforts to manage to grow graphene directly on the target substrate [47], [48], [49], [50], such approaches are still very substrate-dependent and require optimization.

With CVD-grown graphene being one of the most popular techniques for graphene growth, different methods have been developed to transfer it from the metal catalyst onto the target substrate [12], [13]. One can categorize these techniques in a variety of ways. The most prominent over the years has been the wet transfer technique (Figure 5) involving the usage of a polymeric support layer spin-coated on top of the graphene, followed by the wet chemical etch of the metal catalyst, typically Cu, by leaving it afloat on a solution capable of dissolving copper, such as $FeCl_3$ [51]. This type of transfer technique is usually called wet transfer, as the transfer is done in a wet environment involving the metal etchant and another solution used to clean the graphene after the first etch, typically HCl and de-ionized (DI) water. Although commonly used, problems are associated with it, namely the possibility of etchant damage to the graphene and especially the inevitable residues left on its surface from either the etchant or the polymeric support [52]. Polymer residues from one of the most used polymeric supports, polymethyl methacrylate (PMMA), for instance, tend to change graphene's electrical properties by p-doping it [52], [53].

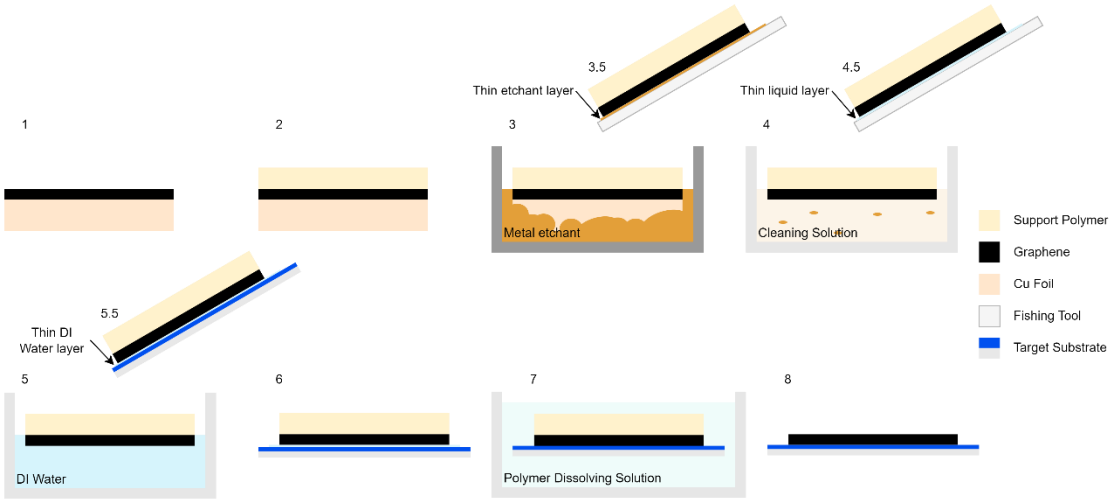


Figure 5 – Schematic of the wet transfer technique.
(1) After the CVD growth of the graphene on top of the metal catalyst, (2) a support polymer is spin-coated on top of the graphene, typically on the top side of the sample. (3) The polymer/graphene/metal stack is left afloat on a metal etchant solution until the substrate is completely etched away, (3.5) followed by the fishing of the polymer/graphene and careful transfer onto the next solution. (4) The sample is again left afloat in the following solution, responsible for cleaning possible metal etchant residues, (4.5) followed by another polymer/graphene stack fishing. (5) The stack is left afloat on DI water, ready for fishing with the target substrate. This way, one avoids unnecessary contact of the target substrate with other chemical solutions. (5.5) When fishing with the target substrate, one aligns the stack with the area where the graphene shall be transferred. A thin water layer remains under the graphene, creating a polymer/graphene/water/target substrate stack. (6) The sample is left to dry so the trapped water evaporates. The sample can dry at an angle so water escapes more efficiently. (7) After drying, the stack is immersed in a polymer-dissolving solution, so the only thing remaining on top of the target substrate is the graphene. (8) After cleaning the sample from the previous solution, the graphene has been transferred, and the fabrication process can resume.

Another option is to transfer the graphene without resorting to polymer support. These support-free transfer techniques from the metal catalyst onto the target substrate rely on achieving good physical contact between the two [54], [55] or a direct synthesis of the target substrate on top of the graphene/metal catalyst [56], followed by the typical etching of the metal.

As mentioned above, wet and support-free transfer techniques have one thing in common: one needs to dissolve the metal catalyst to achieve the "detachment" of the graphene and get the final result. As CVD-grown graphene on Cu foils has shown the most promising results, much work has been put into developing techniques capable of transferring the graphene directly from the growth substrate without the need for metal etchants, improving graphene's quality and dramatically lowering the associated costs. One of these techniques is called bubbling and consists of assembling a setup where a metal catalyst/graphene/support polymer stack and another electrode are immersed in an electrolyte and used as cathode and anode, respectively (Figure 6a). From here, a water electrolysis process is started, resulting in a formation of H_2 bubbles at the metal/graphene interface and a detachment (Figure 6c) of the graphene/support polymer stack, which is left afloat on the electrolyte [57], [58], [59]. This process

is faster than typical metal etching and allows for usage in metal substrates that are more inert and harder to etch, such as Ir, Ru, or Pt. It has also been proposed that this method does not rely on forming the H_2 bubbles but rather on the intercalation of electrolyte ions between the metal substrate and the graphene [60] (Figure 6b). As long as the ions in the electrolyte are not reduced upon contact with the cathode, intercalation is possible, and the graphene/support polymer stack is successfully delaminated. This was proved by applying a potential to the metal/graphene/support polymer stack while immersed in different electrolytes without applying any constant current and no bubble formation. Although promising and cheaper, this bubbling/ion intercalation technique suffers from inducing mechanical damage to the graphene sheet [57] and undesirably doping the material due to the usage of the support polymer and the contact between the graphene and electrolyte's ions [14].

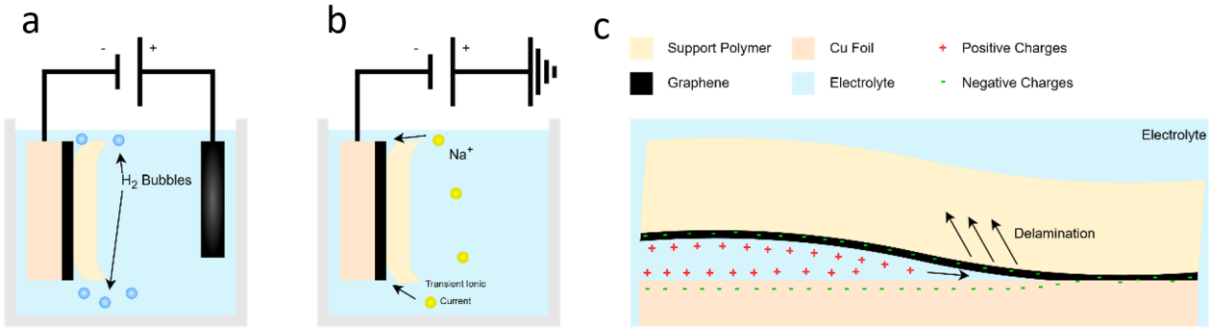


Figure 6 – Schematic of delamination of graphene by bubbling and ion intercalation.
(a) Schematic of the bubbling setup. The metal/graphene/polymer stack is connected to the negative voltage while the other electrode is connected to the positive voltage, functioning as a cathode and anode, respectively. Oxidation will occur at the anode and reduction at the cathode, with the formation of H_2 bubbles and intercalation of electrolyte ions that will detach the polymer/graphene stack. (b) The schematic of the setup utilized in [60]. Although no current passes through the system when it reaches the steady state, there is a transient movement of ions that intercalate between the metal and the graphene, effectively delaminating it. (c) Schematic of the delamination process. While an electrical connection between graphene and copper is maintained, both will be negatively charged and attract positive charges to their surfaces, effectively achieving delamination. This phenomenon works even if the charges are reversed.

As one of the primary sources of contaminants and doping of these transfer techniques resides in the usage of solutions, be they electrolytes or metal etchants, dry transfer methods have also been developed and demonstrate promising results. For dry transfer methods to be reliable, the adhesion energy between the metal catalyst and graphene should be lower than that between the graphene and the supporting layer. This can be achieved by, for example, utilizing metal catalysts for graphene growth that show smaller adhesion energies to graphene, as is the case of Ge [61], [62], allowing for direct dry transfer by utilizing only Van der Waals interaction forces to delaminate it. Unfortunately, Cu possesses an adhesion energy to graphene [63], [64], [65], which is much higher than typical Van der Waals interaction energies [66]. Approaches that utilize a material that possesses a bigger adhesion energy to graphene than that

of Cu after CVD graphene growth have been developed but are substrate dependent. The graphene, after delamination, is "permanently stuck" to this substrate material. For example, this can be achieved by utilizing a polyimide (PI) interlayer on the target substrate and then hot-pressing or laminating it onto the Cu/graphene stack, followed by peeling the Cu [67].

There is yet another route enabling the dry transfer and a direct release from the metal catalyst in the case of Cu growth substrates. It decouples the graphene from the Cu substrate by reducing its adhesion energy. It has long been known that while graphene is one-atom thin, impermeable to most elements, diffusion is possible at graphene crystals' edges and defects. The polycrystalline nature of most graphene sheets grown by CVD on Cu foils presents enough of these edges and defects for gases and water to intercalate and for an interesting process to take place [68]. Although graphene and Cu interface is stable, once water and oxygen manage to come into contact with the two, galvanic corrosion takes place and the graphene, the more noble material of the two, accepts electrons from Cu, in a process that culminates in the oxidation of the metal's surface and the intercalation of water. This galvanic corrosion process reduces the coupling of the two materials (Figure 7a). The chemical reaction taking place can be described as follows [69]:

- Cathode (Graphene) Reaction:

$$O_2 + 2H_2O + 4e^- \rightarrow 4OH^-$$

- Anode (Copper) Reaction:

$$Cu \rightarrow Cu^+ + e^-$$

- Oxide Formation:

$$2Cu^+ + 2OH^- \rightarrow Cu_2O + H_2O$$

This process starts at the graphene edges and defects and then extends laterally to other areas in a positive feedback loop [69], [70] (Figure 7a and Figure 8). The graphene at these sites is decoupled, and water and oxygen manage to intercalate further in the interface. The process repeats itself until the whole graphene surface is decoupled, resulting in a red shift of both graphene Raman G and 2D bands [71]

and the appearance of bands typical of Cu oxides and a visible change of the substrate's color [46], [69], [72] (Figure 7b).

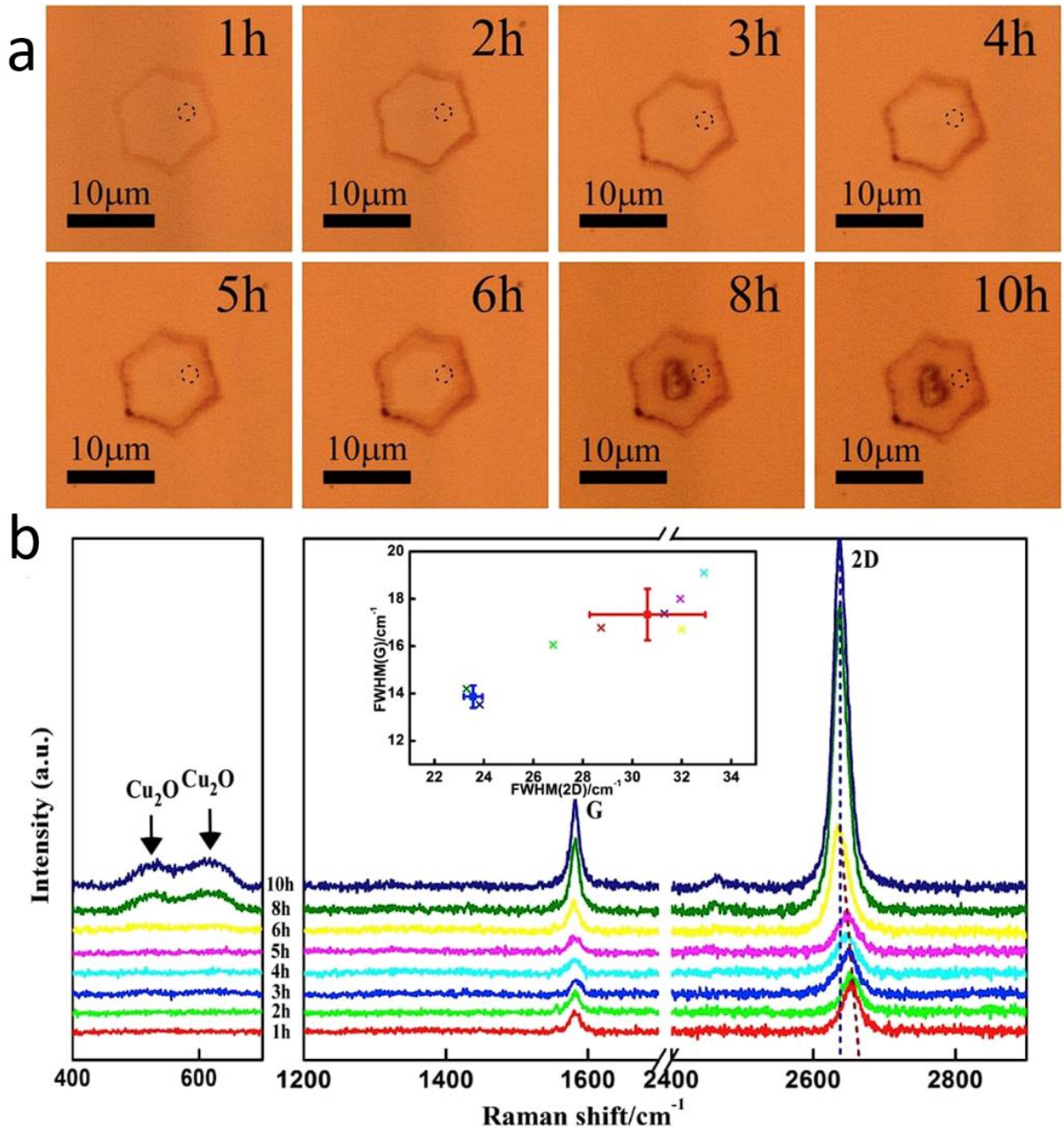


Figure 7 – Evolution of graphene under immersion in DI water.
(a) Optical images of a monolayer graphene crystal grown by CVD on Cu and its evolution after immersion in DI water from 1h to 10h. The oxidation begins at the edges and spreads towards the center. (b) Corresponding Raman signals from the dashed areas in (a). It is possible to notice the appearance of the Cu oxide peaks and the redshift in both the G and 2D peaks. [69]

This decoupling process can depend on the number of graphene layers and the crystallographic orientations of the Cu grains. It has been shown that bilayer graphene presents [73] better oxidation protection of the Cu surface than monolayer graphene or simply bare Cu when immersed in an electrolyte [68] or exposed to an ambient atmosphere [73]. A connection between the oxidation of the Cu growth

substrate and its crystallographic orientation has also been studied. In one study, it was found that Cu(100)/graphene interface was less reactive than Cu(111)/graphene, and thus, the latter is more prone to oxidation, contrary to what happens in bare Cu [73]. A different study assigned different "oxidation modes" to different crystallographic orientations of the graphene-covered Cu surface over 2 years of atmospheric air exposure to graphene while corroborating the theory that bilayer graphene shows better oxidation protection of the metal surface [74]. In this same study, the Cu/graphene stack was later reduced under H_2 annealing and re-oxidized with DI water immersion at 50 °C over 3 days, resulting in a faster oxidation of the Cu below mono and bilayer graphene (Figure 8).

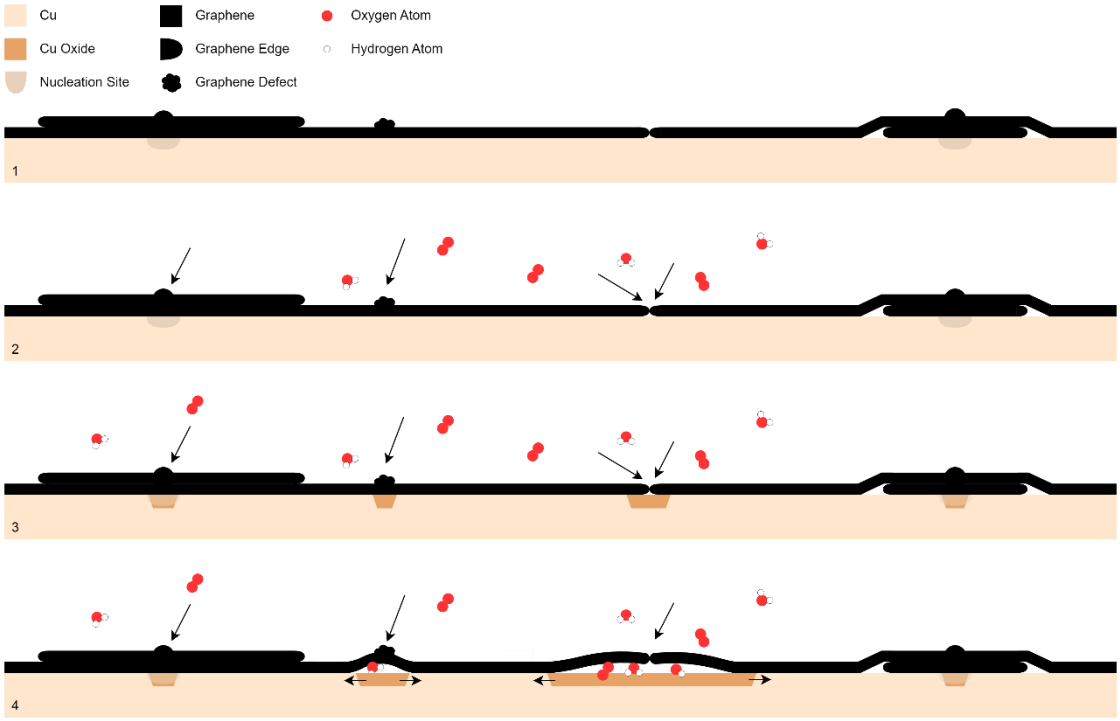


Figure 8 – Evolution of the graphene/Cu interface after exposure to oxygen and water. (1) After growth, nucleation sites, defects, and edges of graphene are spread along the sample. (2) Although graphene is impermeable to oxygen and water, its features allow for their diffusion. (3) Oxidation starts at these features as the oxygen and water reach the interface. (4) Decoupling of the graphene takes place, allowing oxygen and water to diffuse further and the oxidation spreads laterally. Notice how Cu covered in bilayer graphene does not get oxidized easily.

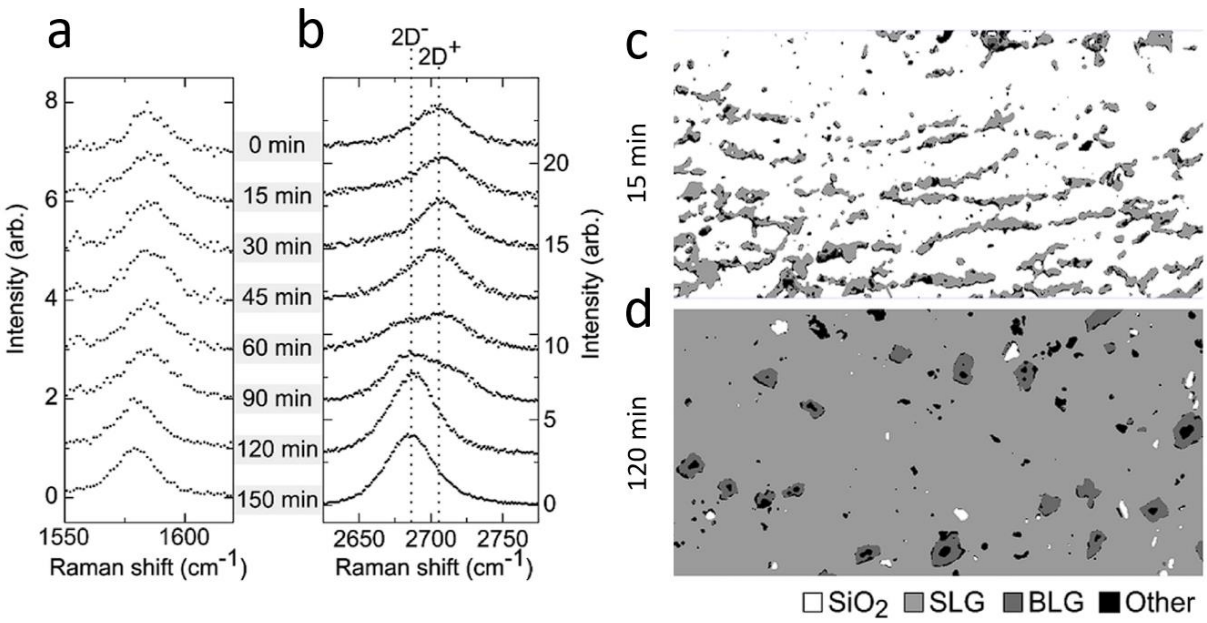


Figure 9 – Evolution of the (a) G and (b) 2D Raman peaks of CVD graphene on Cu after immersion in DI Water at 40° C.
The G peak gets red-shifted while the 2D peak splits into $2D^-$ and $2D^+$. The vanishing of the $2D^+$ peak and the appearance of $2D^-$ peak signal the decoupling of the graphene from the growth substrate. (c-d) Coverage images of graphene transferred by dry transfer onto SiO_2 utilizing PVA as a support polymer after different immersion periods in DI Water at 40° C. After 15 minutes of immersion (c) the graphene coverage is very poor. Still, after 120 minutes (d), the coverage is dramatically improved after the almost complete vanishing of the $2D^+$ peak (b) Adapted from [71].

Decoupling the graphene from the Cu substrate enables (Figure 9) the dry transfer of graphene with a broader range of support materials or target substrates. For example, one study utilized water vapor to induce the graphene decoupling from the Cu substrate and spin-coated polycarbonate on top of the graphene/Cu foil stack, followed by the peeling of the polycarbonate/graphene and subsequent transfer onto the SiO_2 target substrate by electrostatic bonding. The polymer was later dissolved leaving graphene on the target substrate. The Cu growth substrate managed to be reused without loss of material or loss of graphene quality [70]. Although not a dry transfer, another study utilized the decoupling mechanism to selectively etch the Cu oxide formed at the Cu/graphene interface. Polydimethylsiloxane was spin-coated on the decoupled sample, creating a Polydimethylsiloxane/graphene/Cu_2O/Cu stack, which was then immersed in an HCl solution, leading to the etching of the Cu_2O and release of the Polydimethylsiloxane/graphene. The remaining Cu substrate managed to be reused, and the process was repeated, with no apparent decrease in graphene quality [46]. The oxide formation can be sped up by immersion in hot DI water. This was used in another study where a Kapton tape/PMMA/graphene/Cu stack was immersed in DI water at 90°C for 2 hours, leading to the formation of an oxide layer, which allowed for the peeling of the Kapton tape/PMMA/graphene stack and subsequent transfer onto the

target substrate by contacting the two and dissolving the PMMA using acetone [75]. A recent study compared graphene obtained by a dry transfer technique to graphene samples transferred by wet transfer and bubbling. The technique comprised decoupling the CVD graphene from the Cu by immersion in DI water overnight and then laminating a commercial water-soluble polyvinyl alcohol (PVA) film utilizing a simple office laminator (Figure 10). Lamination was done at 110° C followed by a bake at the same temperature, and finally, the Cu substrate was peeled, leaving behind graphene on top of the PVA foil. A second lamination was employed to contact the PVA foil onto the target substrate and a second bake, both at 110° C. To conclude the transfer, the PVA/graphene/target substrate stack was immersed in DI water to dissolve the PVA. This inexpensive and practical technique was done in parallel and compared with the standard wet and bubbling transfers, yielding higher mobility, less doping, and overall higher quality of the graphene. The Cu foils were reused for 5 posterior growths, and the graphene quality did not deteriorate, showing a promising result that utilized fewer resources, was cheaper, more environmentally friendly, and could be scalable [14].

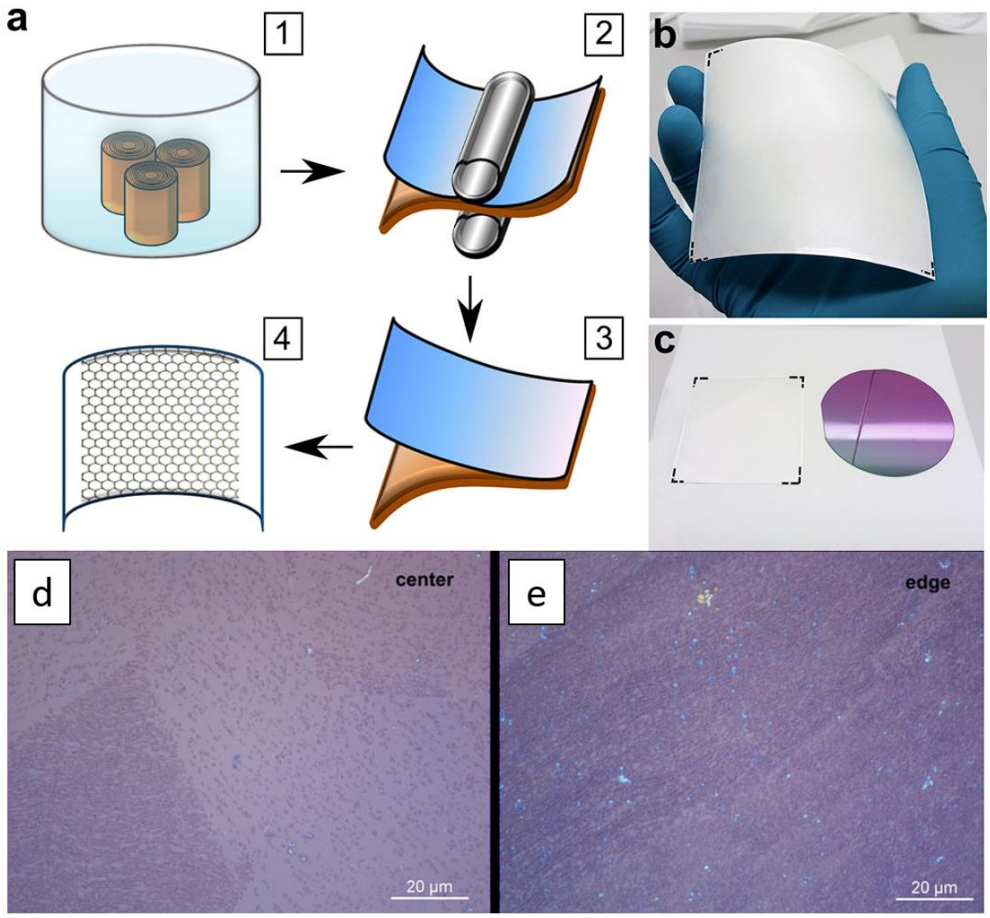


Figure 10 – The dry transfer of graphene with PVA lamination.
(a) The transfer process described in [14]. (1) The as-grown graphene on Cu foil is immersed in DI water overnight to promote the formation of an oxide layer in the graphene/Cu interface. (2) A PVA foil is hot laminated on top of the graphene/Cu at 110° C, followed by a short bake at the same temperature on a hot plate. (3) The

stack is then peeled, transferring the graphene onto the PVA foil, leaving behind the copper oxide and the Cu foil. (4) The graphene/PVA stack is then ready for handling and transfer onto another substrate. (b) Graphene transferred onto PVA. A darker square is noticeable in the center of the foil, corresponding to the graphene-covered area. (c) Graphene on PVA and corresponding target SiO2 wafer. (d,e) Optical images of dry transferred graphene by the described technique onto a wafer with pre-deposited 300 nm of SiO2. Graphene from the center and edge of the Cu foil corresponds to (d) and (e), respectively. One can notice some leftovers of the PVA support layer, visible as light blue dots. Adapted from [14].

Although there are various instances of dry or semi-dry transfer techniques, problems like cracks, tears, and transfer yield of the graphene still make them lag behind the standard wet transfer technique and call for improvement. Nevertheless, overcoming these problems could allow for the mass fabrication of graphene in a continuous process, e.g., roll-to-roll (Figure 11). This technique typically consists of a rolling mechanism where CVD-grown graphene on a roll of thin Cu foil is maintained under tension and laminated to a support layer that already contains the target substrate. From here, the detachment of the graphene from the Cu foil can be done by any of the above transfer techniques, be it wet chemical etch [76], bubbling [77], direct peeling by utilizing a high adhesion layer [15], [78], or even delamination by the oxidation of the Cu/graphene interface to decouple the graphene [79] (Figure 11). This type of transfer, coupled with a roll-to-roll CVD growth of graphene, would allow for continuous and inexpensive fabrication of graphene devices [78].

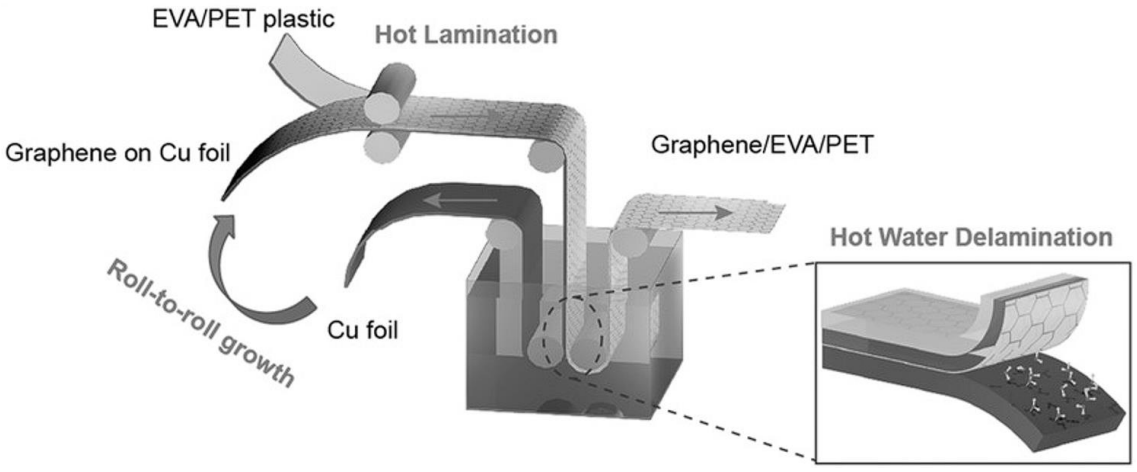


Figure 11 – Schematic of a graphene roll-to-roll transfer process based on hot water delamination. A roll of CVD graphene grown on Cu foil is left in an ambient atmosphere for one week after growth to oxidize the interface between the two. The roll is fed onto the setup, which is laminated to the ethylene vinyl acetate (EVA)/PET stack, followed by immersion in DI water at 50° C for 2 minutes. After that, the stack is delaminated in a dry environment and separated into Cu/Cu oxide and graphene/EVA/PET. [79]

2.1.4 Graphene Field-Effect Transistors

Graphene field-effect transistors (GFETs) are three-terminal devices that use graphene as the channel material, connecting the source and drain electrodes, between which a voltage (V_{ds}) is applied. A source-

gate voltage (V_{gs}) creates an electric field that modulates the source-drain current (I_{ds}) at constant V_{ds} by shifting in energy the graphene electron density of states relative to the Fermi level. Sweeping the V_{gs} voltage creates a characteristic GFET "V" shaped I_{ds}-V_{gs} transfer curve (Figure 12). The lowest current point occurs when the Fermi level is as close as possible to the Dirac point and corresponds to a net zero of charges in the channel at absolute zero, known as the charge neutrality point (CNP) (Figure 12a). Conduction at V_{gs} lower or higher than the CNP corresponds to holes or electrons as the majority charge carriers, respectively (Figure 12b). One of the transistor's most important figures of merit is their transconductance, $g_m = \frac{\delta I_{ds}}{\delta V_{gs}}|_{V_{ds}} \approx \mu \frac{W}{L} V_{ds} C_g$, with W and L the channel's width and length respectively and C_g the total gate capacitance, defined as the derivative of the I_{ds}-V_{gs} curve at a constant V_{ds}. In GFETs, g_m is very high due to graphene's high carrier mobility, and the same transistor exhibits two g_m, one for each branch of the transfer curve [80]. This property is unique to GFETs, as standard FETs exhibit either an electron or hole channel, but not both in the same device.

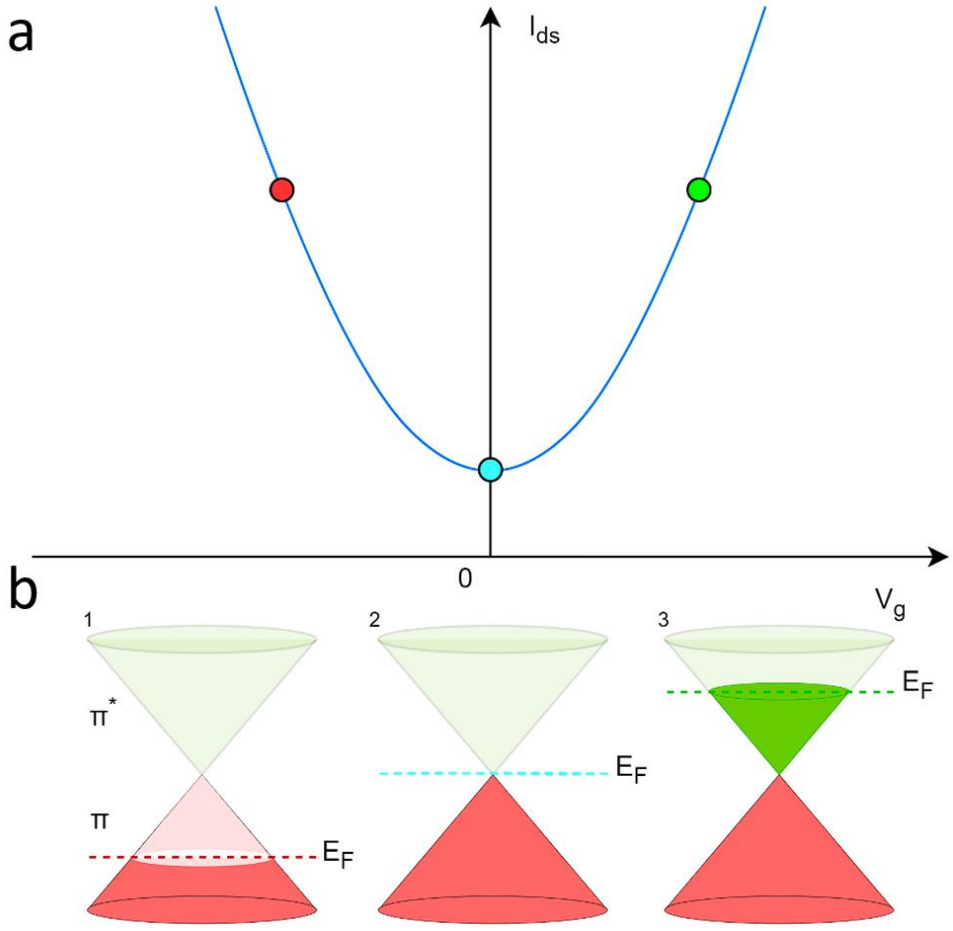


Figure 12 – GFET transfer curve and respective energy bands occupation.
(a) Example of a GFET transfer curve with undoped graphene. Red and green represent bands where holes (valence band) and electrons (conduction band) are responsible for conduction, respectively. The blue point represents the CNP, where the GFET conduction is lowest. (b) Schematic representation of graphene's π and π^* bands' occupation for different points in (a). The Fermi level is modulated by V_g, modifying graphene's

conductivity. When the Fermi level is inside the π band (1), or the π^* band (3), holes, or electrons, are responsible for conduction in the channel, respectively. When the Fermi level coincides with the CNP (2), pristine graphene does not conduct at absolute zero. Still, at finite temperatures, there is always a small electron occupation of states in the π^* band (and the corresponding holes in the π band), and a small current passes through the graphene channel.

Gating of the graphene can be achieved using top gate [81], bottom gate [82], or liquid gate [10] layouts (Figure 13). The first two require a solid dielectric to be placed and aligned between the graphene and the gate electrode. The top gate configuration covers the graphene channel, which is detrimental for applications like biosensing, where exposure of the transistor channel – a unique possibility associated with GFETs – is desired. In contrast, the bottom gate configuration typically possesses a more complex fabrication process. The liquid gate configuration achieves gating by applying an electrolyte (electrolyte-gate) in direct contact with the channel and the gate electrode, thus relaxing the alignment requirements in the other two configurations. The gate electrode in this configuration can be setup in a number of ways, including by immersing an external electrode or by incorporating it in the transistor's substrate (receded gate) [10], [11]. In electrolyte gate setups, a nanometer-sized space-charge electrical double layer (EDL) is formed at the graphene-electrolyte interface [83], achieving a high gate capacitance (≈10 $\mu F/cm^3$ higher than the other two configurations) that allows the GFET operation at low V_{gs} (< 1 V).

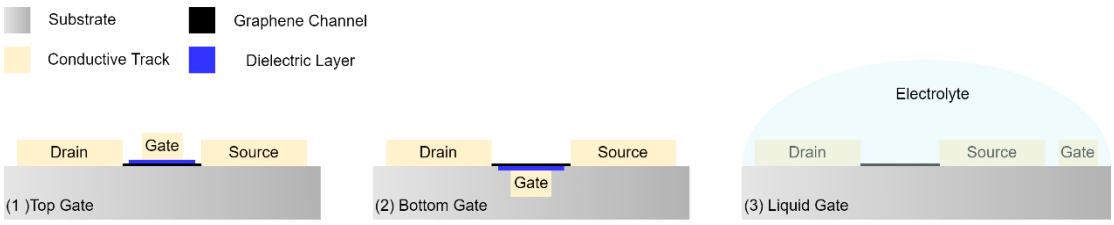


Figure 13 – Schematic of the top gate (1), bottom gate (2), and liquid gate (3) GFET configuration. It is necessary to add a dielectric layer between the gate electrode and graphene for top and bottom gate configurations. In liquid gate configurations, an insulating layer is self-assembled on top of the exposed graphene channel when a voltage is applied to the gate electrode. The gate electrode can be built into the substrate (receded gate) or externally placed inside the electrolyte.

2.1.5 GFET Biosensing

Graphene transistors present many benefits for biosensing, such as high signal-to-noise ratio (SNR), high surface-to-volume ratio with an area more than one order of magnitude higher than the surface area of any other nanomaterial used in biological systems [84], and sensitivity to charges in the device's channel vicinity. Furthermore, exposing the graphene channel to the analyte, which becomes possible in the

bottom-gate and liquid-gate configurations, enables for chemical modification of the material's surface for sensing applications.

In biosensing applications, liquid-gate GFETs are a promising tool as they provide a liquid interface between graphene and an electrolyte solution, which may contain molecules of interest, the target analyte (Figure 14). Because in the liquid-gate transistor the channel-electrolyte interface is part of the electrostatic gating system, the device's behavior will strongly depend on the properties of the electrolyte, be it its pH, ionic strength, or other polar or charged molecules in solution. For biosensing, i.e., to make the device sensitive to a single molecular target, the graphene must be functionalized to react only to specific targets (Figure 14c). The process to achieve such a goal is molecular immobilization on graphene of a biorecognition probe, typically using a linker molecule. Signal collection techniques vary, one of them being detecting a horizontal shift of the Dirac point/CNP in the I_{ds}-V_{gs} curve (Figure 14b). The shift occurs whenever there are local changes in charge distribution at the graphene-analyte interface, i.e., in the EDL. Functionalization of the graphene surface with the biorecognition probe adds receptors, which can be molecules with biological activity (DNA, RNA, aptamers, antibodies, enzymes, or proteins) with high target affinity and specificity so that only the target will react with the receptor (biorecognition). At the same time, other molecular species in the solution will not bind. Binding (Figure 14d) can effectively modify the GFET's properties by different mechanisms. It can, for example, enhance the electron transfer between the electrolyte and graphene or change the charge distribution in the channel vicinity, i.e., the interface capacitance. Since the interface, or better said, the EDL capacitance is crucial to the device's electrostatics, biorecognition events will change the GFET transfer curve, precisely the gate voltage corresponding to the CNP, which is easily detected experimentally [85] (Figure 14b).

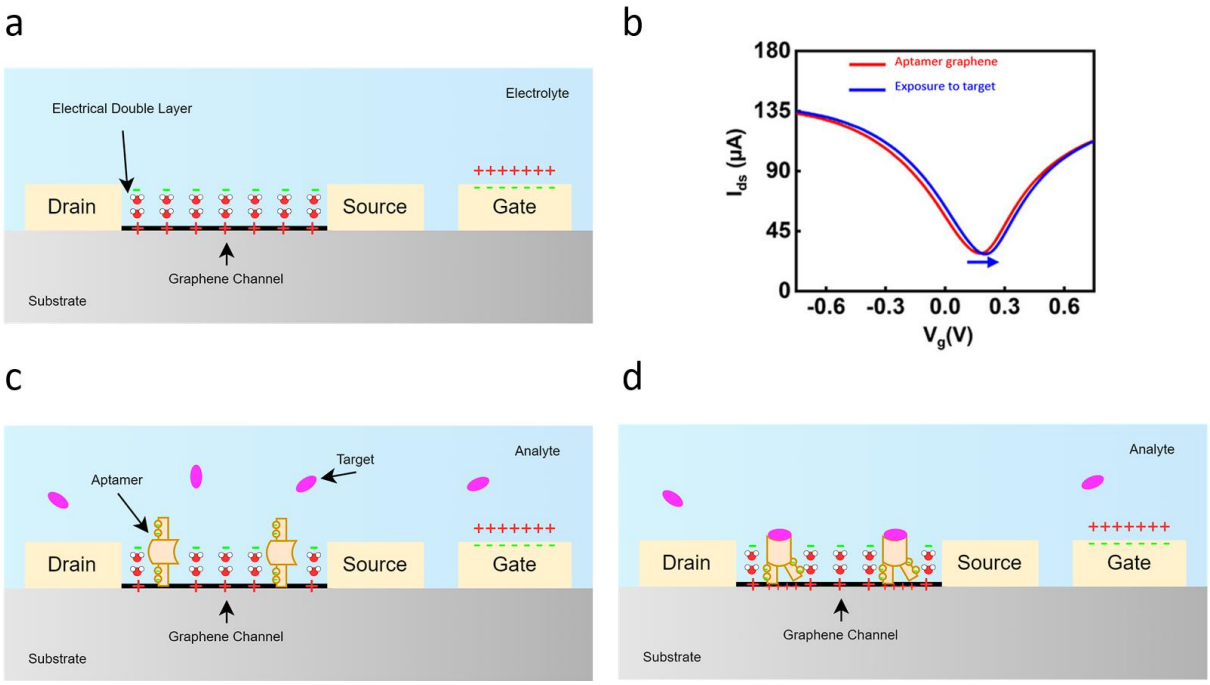


Figure 14 – Schematic of the arrangement of charged particles in a liquid gate transistor when a negative voltage is applied to the gate electrode in a bare graphene channel (a) and a functionalized channel before (c) and after (d) detection by an aptamer.

Positive ions are attracted to the gate electrode while negative ions are attracted to the graphene channel. (a) An electrical double layer of water molecules forms between the graphene and the negative ions at the graphene channel, effectively acting as a gate dielectric. (c) A functionalization process binds aptamers to the graphene channel. These long strands of DNA possess a charge distribution that can affect the doping of the graphene channel. (d) When a biorecognition event takes place, the aptamer changes its conformation, changing the distribution of charges in the graphene channel vicinity, bringing, negative particles closer to the graphene channel that add to the p-doping effect of the gate voltage. (b) The behavior of a functionalized GFET's I-V curve with aptamers when exposed to an analyte with targets. A right shift in the I_{ds}-V_{gs} curve occurs in the CNP, indicating p-type doping when a biorecognition event occurs for this specific case. Adapted from [11].

2.1.6 Flexible Devices

A multitude of graphene biosensing applications have been developed, ranging from healthcare [86], [87], food safety [88], and even gas sensors [53], capable of detecting small concentrations of target molecules. Incorporating these biosensors into flexible devices allows for the development of wearable [89] or even implantable [11] applications.

A wide variety of flexible substrates exist that one can utilize for the fabrication of GFETs, each with its properties (Table 1). Among polymeric substrates, PI is commonly chosen (Figure 15a,b) given its flexibility, robustness, biocompatibility, and high glass-transition point that allows for a broader range of fabrication processes. A wearable application of GFET biosensors in a PI substrate has been realized utilizing the liquid gate configuration, for example, for the detection of IL-6 inflammation biomarker on

[89] by recurring to functionalization of graphene with aptamers, short strands of DNA capable of high affinity and selectivity towards a target molecule. Showing a LOD of 10 pM, this device can detect small concentrations of the biomarker, comparable to devices on rigid substrates. This was achieved by wet transferring graphene onto a PI-printed PCB with pre-deposited 50 nm of SiO2 (Figure 15a), which is considered beneficial for increasing the transconductance and consistency of the devices. Interestingly, in a different study [90] to record action potentials of living cells, it was shown that GFETs fabricated on bare PI on Si wafers showed significantly higher transconductances than those fabricated on wafers with pre-deposited SiO_2 (Figure 17d), reaching 1.9 mS/V·■. The PI was spin-coated twice in order to reduce the surface roughness, achieving a 10 μm thick layer, which might have contributed to the enhanced performance of the transistors. GFETs on PI have also been utilized to detect mi-RNA (Figure 15c) by immobilizing DNA probes on graphene without the need for a linker or complicated functionalization process [91]. A LOD of 10 fM was reached and high selectivity was shown towards the specific mi-RNA associated with breast cancer. It was fabricated by wet transferring graphene onto the PI substrate and a subsequent patterning of Au electrodes by thermal evaporation.

Another important substrate utilized for the fabrication of flexible devices is the transparent and widely used polymer PET. GFET based biosensors have been fabricated on top of this substrate with promising results. For example, an olfactory detector was created on top of PET by utilizing GFETs based on plasma-treated bilayer graphene functionalized with an olfactory receptor. An impressive LOD of 0.04 fM for amyl butyrate, an odorant, was achieved in this liquid-gate flexible device. On [92], a top gate GFET based on a nano-mesh of graphene was fabricated on PET and functionalized with aptamers for the detection of the HER2 biomarker, important in the detection of breast cancer. The LOD reached 0.6 pM in real time detection by measuring changes in the transistor's drain current.

Other flexible substrates for graphene-based sensors have been utilized. In [88] a polyethylene naphthalate (PEN) substrate was utilized for the fabrication of liquid gate GFETs functionalized with aptamers for the detection of Hg in mussels. A LOD of 10 pM was achieved by monitoring the transconductance change with varying concentrations of Hg. Another distinct substrate, Mylar (a type of PET), was utilized in [93], for the fabrication of liquid gate GFETs. The graphene was functionalized for the detection of cytokines, achieving a LOD of 2.75 pM and 2.89 pM for TNF-alpha and IFN-gamma. The 2.5 μm thick flexible substrate allowed the device to conform to complex curved surfaces like the human skin.

Furthermore, it is important for flexible devices to withstand bending and multiple bending cycles with low performance degradation. In various studies, performance degradation is translated into small shifts

in the CNP and small decreases of I_{ds} [89], [94] (Figure 15c), or small increases in channel resistance [91].

The fabrication and configuration of these devices on flexible substrates is noteworthy. Several characteristics of graphene-based flexible devices are summarized in Table 1. Although there is a wide variety of applications, there is a clear tendency towards the usage of liquid-gate GFETs in biosensing, as it allows for a simpler fabrication process while maintaining a large exposure of the graphene to the analyte. Furthermore, the fabrication of the drain and source electrodes is typically done by thermal evaporation of Au and patterning by lift-off. The thermal evaporation allows for the usage of more delicate substrates. It also prevents damage to the graphene when the drain and source electrodes are deposited on top of the 2D material. At the same time, the lift-off spares it from exposure to more aggressive etchants that could modify it and avoid the problematic issue of etch stopping on 2D materials. There is also a clear tendency toward the usage of graphene wet transfer techniques on flexible substrates, presenting good reliability and providing good graphene coverage. However, they can hinder the scalability of device production if one aims to produce large-scale.

Table 1 – List of several flexible graphene biosensors and their characteristics.

Substrate	**Graphene Transfer**	**Configuration**	**Electrode Deposition/ Patterning**	**Detection Method**	**Functionalization**	**Target**	**LOD**	**REF**
PI	-	Liquid Gate (Integrated)	50 nm CVD SiO_2 and printed PCB electrodes before graphene transfer	Dirac point	Aptamer	IL-6 biomarker	10 pM	[89]
PI	Wet Transfer	Liquid Gate (External)	Au e-beam evaporation on graphene	Dirac point	DNA Probe (no linker)	mi-RNA	10 fM	[91]
PI	Bubbling	Liquid Gate (Integrated)	Au patterned before graphene transfer	Dirac point	Pyrene-1-boronic acid	Glucose	0.15 uM	[94]
Kapton	Inkjet printed	Back Gate	Inkjet printed silver	AC gain	Anti-norovirus antibody	Norovirus	0.1 ug/mL	[95]

	graphene ink		nanoparticle ink on graphene					
PET	Wet Transfer	Liquid Gate (External)	Au thermal evaporation on graphene	Current	Olfactory receptor	Amyl Butyrate	0.04 fM	[53]
PET	Wet Transfer	Liquid Gate (External)	Silver Paste on graphene	Dirac point	Glucose oxidase	Glucose	3.3 mM	[96]
PET	Wet Transfer	Top Gate	Au e-beam evaporation and lift-off on graphene	Current	Aptamer	HER-2	0.6 pM	[92]
PET	Wet Transfer and TRT	Resistor	Silver Paste on graphene	Current (non-GFET)	Lactate Oxidase Enzyme	Lactate	0.08 uM	[87]
PET	Wet Transfer	Resistor	Silver Paste on graphene	Current (non-GFET)	None	Ovarian Cancer Cells	-	[86]
PEN	Wet Transfer	Liquid Gate (External)	Au thermal evaporation on graphene	Transconductance	Aptamer	Hg	10 pM	[88]
Mylar	Wet Transfer	Liquid Gate (Integrated)	Au e-beam evaporation and lift-off on graphene	Dirac point and drain current (time-resolved)	Aptamer	TNF-α IFN-γ	2.75 pM 2.89 pM	[93]

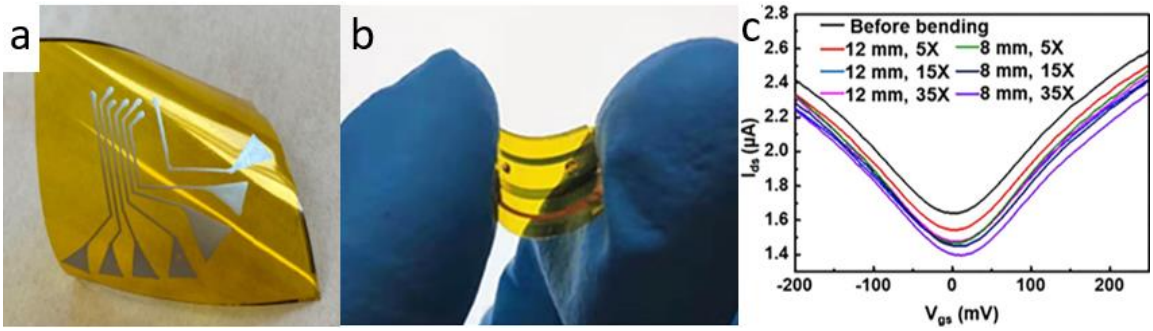


Figure 15 – GFET-based flexible sensors.
(a) Optical image of a flexible GFET-based sensor for IL-6 biomarker fabricated on PI with a LOD of 10 pM. The substrate was initially coated with 50 nm of SiO_2. Adapted from [89]. (b) Image of a flexible GFET-based sensor for MiRNA fabricated on PI with a LOD 10 pM. (c) Evolution of the transfer curve of the GFET in (b) after multiple bending cycles of 8 mm radius. (b),(c) Adapted from [91].

The fabrication and performances of the graphene-based biosensors on flexible devices has been showing promising results. The flexible nature and high sensitivity and selectivity of these devices is useful for NIs. Over the years the applications of graphene have been rising, paving the way for the development of graphene based NIs, addressed in the next section.

2.2 Graphene-based Neural Interfaces

Stimulating and recording brain activity is crucial in understanding the brain's functioning and treating underlying diseases. It can be achieved by designing devices capable of a high spatiotemporal resolution for prolonged periods. Therefore, NIs are devices capable of recording and modulating electrical or chemical brain activity, focusing on their biocompatibility, durability, and reliability. Designing these devices poses many challenges, mainly due to the nervous tissue response to foreign bodies [97]. Also, one of the critical elements of such devices is their flexibility, as mechanically matching the NI's properties to those of the tissue maximizes device longevity and minimizes mechanical damage to the surrounding tissue [98]. Different challenges arise depending on different modalities for recording or modulating brain activity. Graphene can help manage them.

2.2.1 The Neuron and Neurotransmitters

The human brain comprises roughly 86 billion neurons [1], [2] with various cellular sub-types that share the same basic structure. A neuron is a cell typically comprised of different cellular compartments including the dendrites, the soma, and the axon (Figure 16a), each possessing distinct functions and membrane properties. Dendrites are connected to different neurons and are responsible for receiving information input. They then connect to the soma, or cell body, where the nucleus is located. Finally, the axon is the neuron branch in charge of outputting information to other neurons. Each connection of an axon terminal to a dendrite is called a synapse, and each neuron can establish up to 5000 synapses with other neurons [99], [100].

Neurons communicate with each other via electrochemical signals. Within a neuron, the communication is electrical, propagating an electrochemical potential throughout the membrane (from the dendrites to the soma and then to the axon) via ionic channels that can regulate ionic flux across the membrane (Figure 16a inset). Communication between neurons is typically achieved through chemical signaling via molecular messengers called neurotransmitters (electrical communication between neurons is also possible through specialized connections called gap junctions, albeit less frequent). The release of chemical signals is commanded by the electrochemical potential propagated along the neuron reaching the synapse (Figure 16b). There is an interdependence between the two types of signals: electric signaling leads to release of neurotransmitters which induce a new electrical signal in another connected neuron, thus resulting in the transmission and processing of information between neurons.

Neurotransmitters commonly have an excitatory or inhibitory effect on the target neuron, which can promote or inhibit the activation of the neuron receiving these stimuli. They are released into the synaptic cleft, a gap between the neuron outputting information and the one receiving it, with a size ranging from 10-25 nm [101]. Neurotransmitters are released from the presynaptic neuron and then bind with specific molecular receptors in the postsynaptic neurons, inducing an electrical response [102].

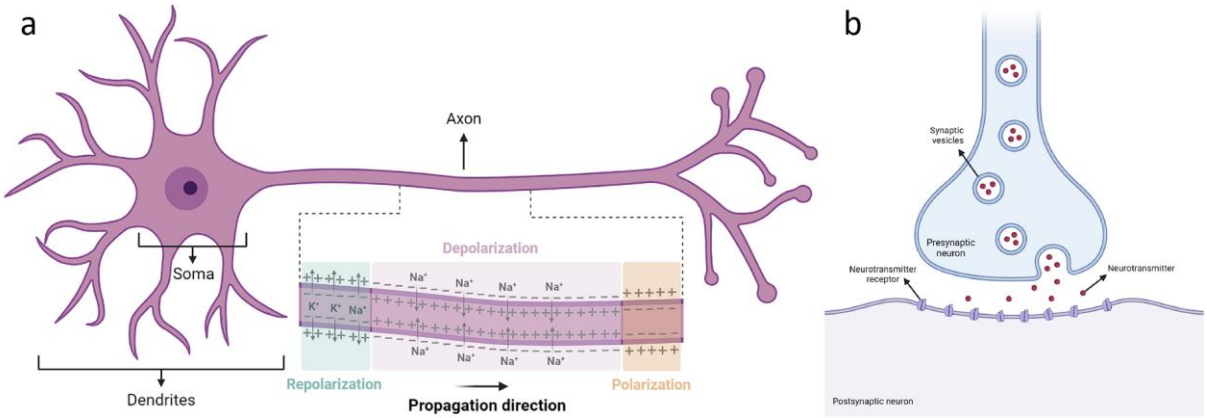


Figure 16 - Schematic representation of the neuron and the synapse.
(a) The neuron is typically comprised of the dendrites, soma, and the axon. (Inset) Propagation of an electrochemical signal along the axon. (b) At chemical synapses, neurotransmitters are released in very small quantities, being "sensed" by the postsynaptic neuron.

There are over one hundred known neurotransmitters and even more receptors. Neurotransmitters can be categorized depending on their molecular properties in groups such as monoamines, amino acids, purines, soluble gases, and peptides [102]. Although neurotransmitters' function might vary at the neuron level depending on different types of receptors at the dendrites, different roles can be addressed to each neurotransmitter at a bigger scale. One example is dopamine, a monoamine with great significance in the brain's function because it is involved in critical roles such as motor behavior and coordination, motivation, and learning. Dysfunctions of its levels or dynamics underlie several brain disorders, including Parkinson's Disease, Alzheimer's Disease, schizophrenia, attention deficit hyperactivity disorder, among others [103].

2.2.2 Neural Activity Recording

Brain activity is electrochemical, so interdependent electrical and chemical processes are taking place for the brain to function correctly. As such, monitoring brain activity can focus on detecting either.
Electrical recording techniques focus on detecting electrical potentials or currents due to electrical activity in the brain. These techniques vary in invasiveness and spatiotemporal resolution, typically inversely proportional. For example, electrical recording of brain activity is done mainly by using capacitive

electrodes near the target tissue or cells. Microelectrode arrays of metallic conductors on silicon substrates or brain mesh electronics [104] provide good spatiotemporal resolution in exchange for invasiveness, allowing electrical activity from dozens to hundreds of individual neurons in the brain [97]. Neural interfaces have utilized GFET configurations to perform successful electrical brain activity recordings [90], [105]. Taking advantage of the intrinsic amplification of the transistor configuration, based on the graphene electrical properties conferring high transconductance, operation at low gate biases up to 100 mV are possible. Implantable applications of these GFETs is enabled as the low biases do not pose a risk of damaging the biological tissue. GFET-based devices have been accomplished in PI on silicon [90] and bare PI [105], [106], [107], exhibiting transconductances higher than on other substrates (Figure 17). Like in other flexible GFET integrations, after repeated bending cycles, a slight decrease in transconductance and, thus, performance was detected [105] (Figure 17a,b). In one of the studies, the GFETs showed higher SNR than platinum (Pt) electrodes of similar size [107].

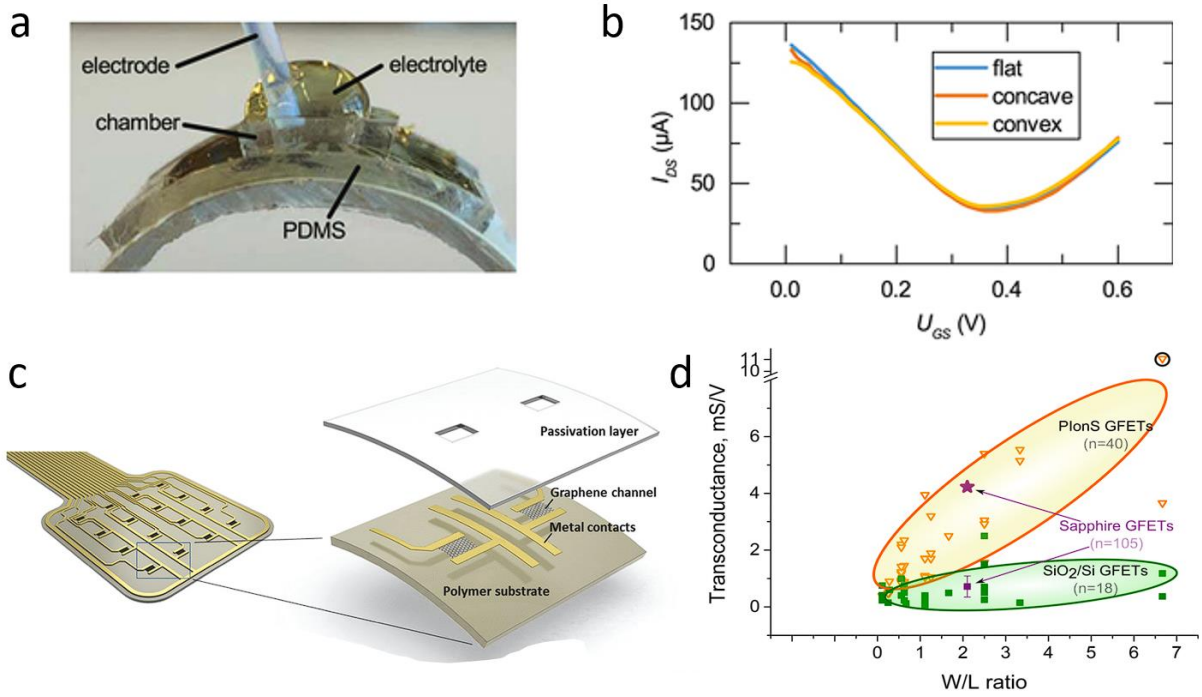


Figure 17 – GFET-based neural interfaces.
(a) Device with liquid gate GFETs fabricated on PI bent in a convex shape, immersed in electrolyte with the external gate electrode. [105] (b) Source-drain current of the device in (a) as a function of the applied gate voltage for flat (blue), concave (orange), and convex (yellow) bend conditions. It is possible to observe a negligible influence of the bend in the characteristic curve of the devices. [105] (c) Schematic of a liquid gate GFET array fabricated in [106]. The device was fabricated on top of a PI substrate. Conductive tracks were made of gold, and the graphene was transferred via wet transfer, followed by patterning. No gate electrode was integrated into the substrate, and an external gate electrode had to be utilized. (d) Comparison plot of channel area normalized transconductance versus the W/L ratio of the GFETs in [90]. GFETs fabricated on PI on silicon and SiO2 on Silicon are depicted by orange triangles and green squares, respectively. Colored areas denote the distribution of points for each type of GFET respectively. Purple points represent the GFETs fabricated on sapphire. The purple square refers to the GFETs fabricated in the study, and the purple star represents the best GFET fabricated at the

time of publication. The black circle denotes the best GFET in terms of normalized transconductance. GFETs fabricated on PI tend to provide a higher transconductance throughout the W/L ratio. Adapted from [90].

Recording of chemical activity in the brain is typically more complex than electrical. For example, neurotransmitters are released in very small quantities. A high sensitivity is crucial for probing their release and concentration in brain tissue. Furthermore, biological mediums as the brain are comprised of different molecules and cells and include many different neurotransmitters in one single area. Consequently, chemically similar molecules exist in the human brain and telling them apart can be challenging, as in the case of dopamine and levodopa. Sensor selectivity is thus necessary so measurements can be reliable.

Sampling of brain fluid can be a viable option for probing neurotransmitters concentration. Microdialysis, for example, relies on microfluidic channels implanted into the brain and can be used for neurochemical sensing. In [108], a Si microdialysis probe with a cross-section of only 45 μm×180 μm was fabricated. The probe was comprised of a microfluidic inlet and outlet terminating in a porous membrane at the sampling area. It managed to acquire samples from mice brains, later analyzed by liquid chromatography-mass spectrometry, revealing detection of 14 different neurotransmitters. Nevertheless, this kind of approach usually relies on external methods for analyzing the samples, which can be time consuming and not suitable for real-time monitoring.

Electrochemical methods allow for better temporal resolution and are utilized to detect electroactive molecules. Cyclic voltammetry is an example of a technique that detects redox reactions of the target molecules at electrodes when a varying voltage is applied. The voltage at the working electrode is swept forward and backward (resembling a triangular waveform), which creates a characteristic I-V curve for each molecule as the reactions occur. Fast-scanning cyclic voltammetry is a similar technique that can provide higher temporal resolution [109] by utilizing faster scanning potentials. These two techniques still fall short in selectivity compared to other emerging techniques. In [110] a fast-scanning cyclic voltammetry approach was utilized for detection of dopamine in living animals utilizing carbon fiber microelectrodes. A LOD of 0.96 nM was achieved in vitro, enabled by the developed sawhorse scanning potential, which contrasts with the typically used triangular waveform. A recent study [111] managed to fabricate an implantable array of glassy carbon microelectrodes with a PI substrate for simultaneous electrochemical detection of dopamine and serotonin. The device managed a LOD of 10-200 nM for both neurotransmitters by detection of different oxidation and reduction peaks of both molecular specimens.

Enhancing the selectivity of electrochemical sensors can be achieved by the utilization of molecules with high specificity. Enzymes have been immobilized on electrodes to promote selectivity towards

neurotransmitters. In [112], glutamate oxidase immobilized on an Au electrode was used to decompose glutamate, an abundant neurotransmitter. Electrons formed during the reaction between glutamate and the respective enzyme were measured to infer the neurotransmitter's concentration, reaching a LOD of 5 μm.

Aptamer-based sensors are also viable options for chemical sensing due to their high affinity and specificity [113] and can take different approaches [114], including the integration in GFETs [10]. This biorecognition method presents higher selectivity than cyclic voltammetry, although temporal resolution still lags. The implementation of aptamers for the simultaneous detection of dopamine and serotonin was achieved in [115]. In_2O_3 transistors were functionalized with dopamine and serotonin specific aptamers, which modulated the drawn current upon binding with the corresponding neurotransmitters. The achieved device was highly flexible due to the 1.4 μm thin PET substrate while at the same time presenting a LOD of 10 fM. Finally, a recent study [11] has accomplished an implantable GFET-based sensor functionalized with dopamine-specific aptamers (Figure 18), similar to [10], with 10 pM LOD of dopamine, an upper limit of 100 μM, and high selectivity. It was fabricated on a 76 μm thick flexible PI substrate via wet transfer of CVD-grown graphene and magnetron sputtering of gold (Au) contacts and later implanted in mice. Demonstration of detection *in vitro*, *ex vivo*, and *in vivo* was possible, with the latter being pharmacologically evoked via a microfluidic connection to the implantation site, although not part of the device. It utilized the modulation of the graphene drain-source current due to the binding of the aptamers to dopamine to infer its concentration. This study has proven the viability of GFET biosensors on flexible substrates for implantable neural interfaces for neurochemical recordings.

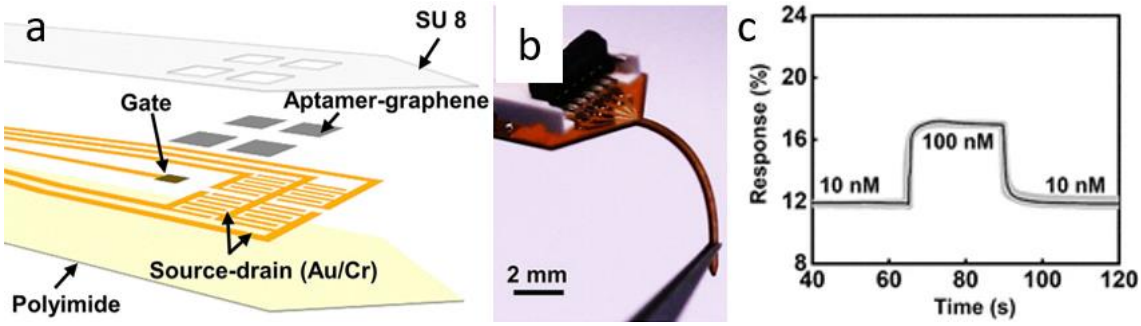


Figure 18 – Implantable and flexible GFET neurotransmitter sensor.
(a) Schematic illustration of the implantable and flexible GFET aptamer-based sensor for dopamine. SU 8 was utilized as a passivation layer, exposing only the graphene channels. Chromium (Cr) was used as a seed layer for the Au tracks. (b) Optical image of the implantable device on a 76 μm PI substrate, with a total weight of 31 mg. (c) Time-resolved response of the device to different dopamine concentrations in vitro. The response is defined as the variation in drain-source current, ΔI_{ds}, divided by the initial current, I_0, before the addition of dopamine. The measured on and off times were 2.09 s and 5.38 s, respectively. (a), (b), (c) Adapted from [11].

2.2.3 Neural Activity Modulation

One can achieve brain activity modulation by various techniques. Pharmacological modulation is based on utilizing drugs to modulate brain activity. This is complicated due to the blood-brain barrier impermeability to most substances. Thus, techniques for directly delivering the drugs to the target area have been developed. These usually rely on microfluidic channels inserted into the brain, managing to contact the target area and release the drugs directly [116]. For example, in [117], a microdialysis probe was fabricated with push-pull microfluidic channels for both drug delivery to the brain and sampling of fluid (Figure 19a). Successful stimulation of tissue was achieved, confirmed by measuring electric signals with iridium electrodes after delivering KCl onto the tissue.

Magnetic methods can also be utilized. They utilize electromagnetic induction to influence the firing of nearby neurons by generating electric currents inside the brain. It allows for non-invasive modulation as the induction effect can occur at a distance without needing a physical connection, albeit neurons cannot be targeted individually [118]. In [119], a submillimeter sized inductor was utilized to demonstrate magnetic stimulation of tissue in mice with higher targetability. It was fabricated by utilizing a commercial surface-mount device coil and attaching it to insulated copper wires for powering. The magnetic induction device was implanted in the dorsal cochlear nucleus of mice, and stimulation was verified by placing recording electrodes at the inferior collicus – both brain regions part of the auditory pathway of mice. A more recent study [120] managed to microfabricate implantable Cu microsolenoids only 80 μm × 40 μm in footprint and coated in Parylene-C for biocompatibility (Figure 19b). They managed to induce stimulation ex vivo, in acute transgenic mice brain slices, verified by calcium imaging.

Using ultra-sounds has also proven effective in modulating brain activity non-invasively. This technique focuses ultra-sounds in small brain areas and can achieve excitatory or inhibitory brain activity behavior [121]. In [122] a focused ultrasound transducer was utilized for brain activity stimulation, tracked by simultaneous functional magnetic resonance imaging. The experiments were completely non-invasive, and no damage was done to the alive animal test specimen. High spatial resolution was achieved in [123] by utilizing a dual setup of focused ultrasound transducers. The sonic beams were aligned to focus the ultrasounds on a small brain region, achieving a focal volume of only 0.52 μm^3, capable of stimulating the habenula of mice. Micron-sized ultrasound transducers have also been fabricated in [124]. The fabrication process entailed the usage of a piezoelectric layer and patterned electrodes by microfabrication techniques, achieving a transducer membrane of only 500 μm of with and 55 μm thickness (Figure 19c). Although not used for stimulating brain cells, the small footprint of the device managed to stimulate cells in vitro with high spatial resolution, verified by calcium imaging.

Electrodes have been extensively used to apply sufficient voltage to specific brain regions and modulate activity. These techniques are more invasive, requiring proximity between the electrode and the target brain area. Electrodes have been utilized in humans, for example, to treat conditions such as epilepsy. Deep brain electric stimulation with electrodes aided in reducing the frequency of seizures [125]. To minimize invasiveness, transcranial electrode arrays have also been utilized for brain stimulation, as in [126]. By activating different combinations of electrodes, the applied electric fields were sculpted to target specific brain regions of the motor cortex of mice. The array of electrodes was fabricated utilizing standard flex-PCB technology. Graphene has also been utilized to fabricate electrodes for brain stimulation. In [127], graphene fiber electrodes were achieved by reducing suspensions of graphene oxide. The electrodes were then utilized for brain stimulation with simultaneous functional magnetic resonance imaging. The graphene fiber electrodes produced little imaging artifacts compared to metal ones.

Light can also be utilized to modulate brain activity; the next section will be dedicated to it.

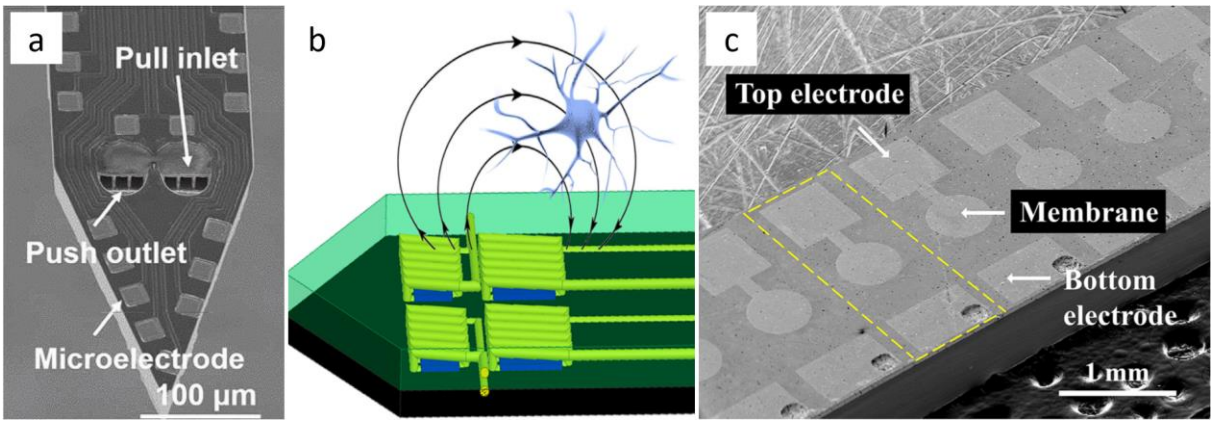


Figure 19 – Devices for brain activity modulation by microdialysis, magnetic induction and ultrasounds. (a) SEM image of microdialysis probe in [117], with visible microfluidic channels inlet and outlet, as well as built-in recording microelectrodes. (b) 3D Schematic of microfabricated probe with microsolenoids in [120]. The applied magnetic field stimulates nearby neurons by inducting a current. (c) Angled SEM image of the array of microfabricated ultrasound transducers in [124]. The dashed yellow rectangle delimits a single transducer. The electrodes deliver the necessary voltage to oscillate each membrane.

2.2.4 Optogenetics

Optical brain stimulation uses photons delivered in a specific wavelength to targeted brain areas containing modified light-sensitive neurons. This modality of brain stimulation is called optogenetics and is made possible by expressing microbial light-sensitive proteins called opsins in target cells. Chlamydomonas reinhardtii Channelrhodopsin-2 (ChR2) and Natronomonas pharaonis halorhodopsin (NpHR) are two of the most significant opsins. ChR2 is a non-selective cation channel that, when expressed in the membrane of a neuron, can excite it if hit by blue light with a wavelength near 470 nm.

NpHR is a chloride ion pump that can inhibit the firing of a targeted neuron when hit by yellow light with a wavelength near 580 nm [128], [129] (Figure 20a). Expression of these proteins in neurons is mainly achieved by genetically manipulating the organism or by viral gene delivery, utilizing viral vectors encoding the opsins. These opsins have fast kinetics, allowing for selective modulation of brain activity. Compared with other stimulation methods, optogenetics offers high targetability of specific neuron sub-types via genetic manipulation and allows for easier integration in multimodal devices that utilize electrical transduction. Nevertheless, its use in humans raises concerns due to ethical matters with respect to willingly introducing genes encoding opsins into neurons. However, in a recent study, optogenetics was used in the human retina to restore vision in a blind patient for the first time [130].

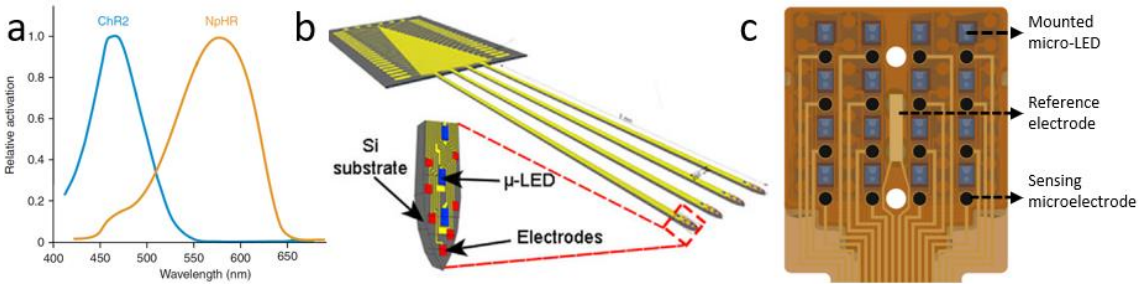


Figure 20 – Opsin responses and μLED integration in NIs.
(a) Response of ChR2 and NpHR to light of different wavelengths. They present distinct peaks which allow for individual activation of each opsin. Adapted from [129]. (b) Monolithic integration of μLEDs in a silicon probe. Each μLED can output 60 nW of power [131]. Gallium nitride was used for blue light emission. Adapted from [132]. (c) Schematic of a neural interface with 16 mounted μLED arrays on a PI substrate. Each μLED has dimensions of 220 μm * 270 μm * 50 μm. Adapted from [7].

Methods for delivering light to the brain vary, but studies typically use strategies including fiber optics [133], [134], waveguides [135], mounted [7] (Figure 16c), or built-in [131] (Figure 20b) μLEDs depending on the application and type of neural interface [136]. Fiber optics were the first to be utilized and stand out for their simplicity and bulkiness. This approach fails to provide a high density of light-delivering sites, as one optical fiber is usually needed per site, although multicore tapered fibers have been developed [133]. Also, integration with other recording modalities requires complicated handling techniques [132], [137]. Waveguides, on the other hand, can deliver light to multiple sites without compromising devices' dimensions [138]. They are easier to integrate with other modalities as they can be accomplished with standard microfabrication techniques [139]. Like fiber optics, waveguides require an external light source, such as a solid-state laser or a high-intensity LED, implying a physical connection to the outside of the brain. However, some applications have been developed where LEDs or laser diodes are used as light sources built into the device, but still placed outside the brain [134]. Contrarily, μLEDs bring the advantage of not needing an external light source and present low power consumption. They

enable multi-site light delivery with individually addressable μLED arrays [140]. However, built-in ones are difficult to fabricate and require substrate-dependent optimization, and mounted types suffer from complex assembly techniques. In the built-in μLED versions in [131], an Si substrate was utilized for the fabrication of the device. Multiple layers of different materials were deposited and lithographically patterned, making fabrication complex. Furthermore, the efficiency of the μLEDs was very small, with only 1.1% of the inputted power reaching the neurons in the form of light. Authors state that utilizing sapphire substrates could increase the efficiency of the device, emphasizing the substrate-dependent optimization needed. In [7], the mount-type μLEDs were assembled by creating an SU-8 slot where the glue was deposited so the component would stay in place. The amount of glue was critical as too much glue would overflow and damage the device, and too little would not fixate the component. Later, the μLED was wired and bonded to the rest of the substrate, and the connections were covered with silicone. This resulted in a bulky assembly unsuited for deeper brain implantation. Also, having the light source close to the delivery site, although enabling high light intensity, poses a risk of damaging the tissue due to the heat generated by the μLED operation [8].

In this type of applications where optical stimulation is used, transparency of the utilized materials is essential to prevent the creation of photoelectric artifacts or even improve light transmission [141]. Graphene is a promising material for use in transparent neural interfaces and has been utilized to fabricate transparent electrodes proven to provide high transmittance [142] (Figure 21). Light-induced artifacts can also be suppressed by utilizing graphene as a conductive electrode [143] (Figure 21c). However, lower-quality graphene can produce unexpected artifacts due to defects or residues from the fabrication process.

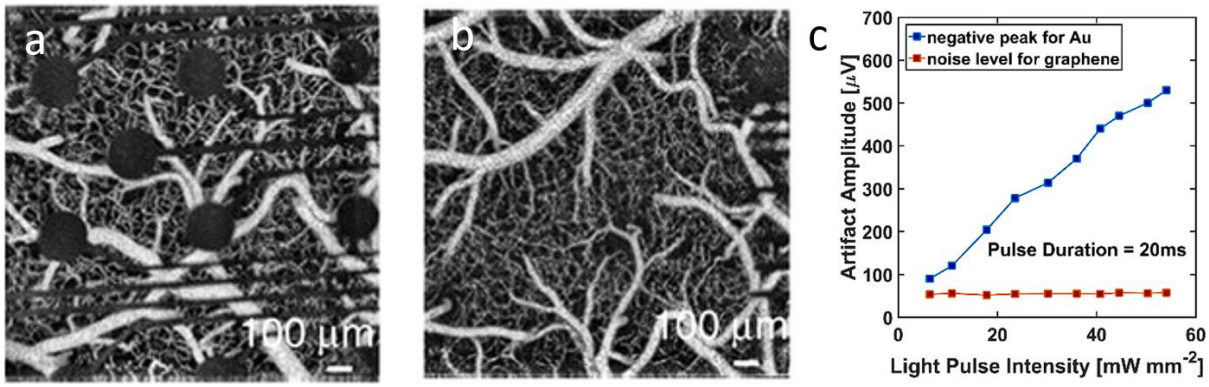


Figure 21 – Graphene electrode's optical and electrical advantages.
(a,b) Maximum intensity projection of optical coherence tomography angiogram showing cortical vasculature through a platinum micro-electrocorticography device (a) and a similar device utilizing graphene electrodes (b), fabricated on Parylene-C substrate. Adapted from [142]. (c) Artifact amplitude as a function of irradiated light pulse intensity for gold microelectrodes (blue) and graphene microelectrodes (red). The artifacts are negligible for the graphene electrodes [143].

3. MATERIALS AND METHODS

3.1 General Methods

3.1.1 Optical Microscopy

Optical microscope (OM) images were acquired in two different types of OMs. Images taken inside the cleanroom utilized a Nikon Eclipse L200N equipped with 1x, 2.5x, 5x, 10x, 50x, and 100x zoom lenses and a motorized stage. The motorized stage was used to perform scanning of large images where different images were acquired at adjacent locations and stitched by software. Images taken outside the cleanroom utilized a Motic PSM-1000 microscope equipped with 10x, 50x, and 100x zoom lenses and a mechanical stage.

3.2 Wafer Fabrication

3.2.1 Plasma-Enhanced Chemical Vapor Deposition of SiO_2

An SPTS CVD MPX plasma-enhanced chemical vapor deposition (PECVD) system (Figure 22) was utilized to deposit SiO_2 conformally on Si wafers. A 500 nm SiO_2 thin film was deposited at 300°C and 30 W power plasma, in a vacuum pressure of 900 mTorr, with 1420 sccm N_2O, 10 sccm SiH_4 and 392 sccm N_2 flows, for 10 minutes and 37 seconds.

Figure 22 – Utilized SPTS CVD MPX system.

3.2.2 Spin Coating of Polyimide

A spin-coating procedure was done to achieve PI layers. A Polos Spin200i system was utilized to spin-coat PI2611 (HD Microsystems) (Figure 23). This precursor comprises polyamic acid precursors dissolved in a n-methyl-2-pyrrolidone-based solvent carrier. The PI precursor was stored at -20°C and left at room temperature for 12h before spin-coating. The process for creating a PI layer can be divided into four steps: adhesion promoter application, PI precursor spin-coat, soft-bake, and curing, described in more detail below:

1. To promote adhesion between the PI and the underlying substrate, the VM-651 (HD Microsystems) adhesion promoter was diluted in H_2O to form a 0.1% (V/V) solution. The wafer, already placed in the spin-coater, aligned, and fixed onto the vacuum holder, was covered with the adhesion promoter solution while static and left for 20 seconds. A spin dry procedure followed with a 3-second ramp and 30 seconds at 3000 rpm speed to remove the solution.
2. Without removing the wafer from the spin-coater, the PI precursor was manually dispensed at the center of the wafer. The precursor was left idle for 30 seconds, followed by a 3-second ramp and 30 seconds at 500 rpm, for spreading it on the wafer. Finally, to achieve the desired thickness of the precursor, the spin-coating process continued with a 6-second ramp from 500 rpm to 3712 rpm, and this speed was maintained for 30 seconds.
3. The soft-bake procedure starts by pre-heating a hotplate to 70°C and baking the wafer for 180 seconds, followed by a slow ramp of 2-4°C up to 170°C, where the temperature is maintained for another 180 seconds.
4. The final curing took place in a Memmert UFE400 furnace with a 2-hour ramp from room temperature up to 250°C. This temperature was held for 14 hours to fully convert the precursor into PI and evaporate the solvent carrier.

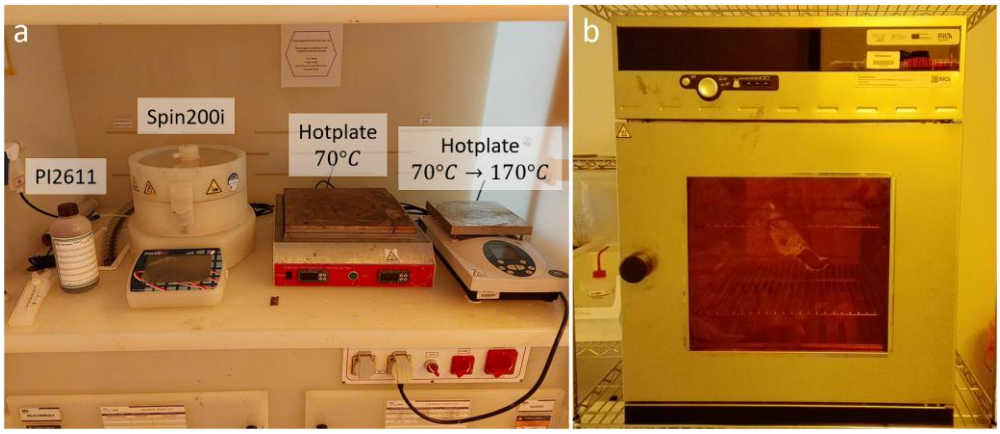


Figure 23 – Utilized setup for spin-coating of the PI film.
(a) Setup located in the fume hood. Two different hotplates are utilized for the different soft-bake moments. (b) Utilized furnace for the curing of the spin-coated PI films.

3.2.3 Lithographic Patterning

The lithography procedure was done to create a pattern in photoresists. Patterns were defined by digital drawings created in AutoCAD 2023 and exported as a *.dxf file (DXF is a Drawing Exchange Format). The utilized photoresist was the positive photoresist AZ 1505 (MicroChemicals), and the utilized developer was the AZ400K (MicroChemicals) in 1:4 proportion. The spin-coating and development of photoresists was done in a SUSS Microtek Gamma Cluster system, which is an automated spin-coater and developer. The utilized lithography system was the Heidelberg Instruments DWL 2000, a high-resolution, laser-based maskless optical lithography system capable of achieving features as small as 700 nm and writing on 200 mm wafers (Figure 24).

The lithographic patterning process consists of three steps: spin-coating of the photoresist, exposure, and development, detailed below:

1. The spin-coater of the Gamma Cluster is utilized to dispense AZ1505 photoresist on the wafer and achieve a thickness of either 600 nm or 1035 nm by utilizing 3500 rpm or 1000 rpm for 30 seconds, respectively, followed by a soft bake at 100° C for 60 seconds.
2. According to the defined drawings, the wafer with the spin-coated photoresist is placed in the DWL 2000 for exposure. Using alignment marks, an alignment procedure is performed for lithography on top of already patterned layers. The focus position and laser intensity are regulated according to the defined parameters updated monthly by the cleanroom technicians.
3. The already-exposed wafer is placed in the Gamma Cluster once again to develop the photoresist in AZ400K developer. The developing time depends on the thickness of the photoresist. As such,

either 60 seconds or 120 seconds are utilized for 600 nm and 1035 nm thicknesses, respectively. The wafer is then washed with DI water and spin-dried.

Figure 24 – Systems utilized in photolithographic processes.
(Left) Utilized SUSS Microtec Gamma Cluster system for spin-coating of photoresists of different thicknesses,
(Right) Utilized Heidelberg DWL 2000 system for lithography patterning of the photoresist.

3.2.4 Material Sputtering Tools Kenosistec and Timaris

Two different physical vapor deposition (PVD) systems were utilized for material sputtering. The Kenosistec Sputtering system was utilized for the sputtering of Cr and Au layers, consisting of a UHV deposition chamber with 11 magnetrons in confocal geometry (although only one was utilized), allowing for co-deposition of materials on wafers of up to 200 mm in diameter. Before the sputtering onto the target wafer, a deposition of the materials was done on a dummy wafer to clean the target. First, the deposition of Au was always preceded by a deposition of a Cr layer to improve adhesion. The sputtering time was varied to achieve different layers' thickness.

The Singulus Timaris Four-Target-Module was utilized for the sputtering of AlSiCu alloy in UHV, with the aid of a single magnetron. The sputtering time was varied to achieve the desired thickness of AlSiCu layer and a soft pre-etch was performed to aid in the adhesion.

3.2.5 Reactive Ion Etching

For dry etching of the PI films, a Reactive Ion Etching (RIE) STPS APS system was utilized. The etching was achieved under a 25 mTorr atmosphere, with 20 sccm CF_4 and 80 sccm O_2 flows, and a plasma created by a 13.56 MHz coil and platen with 1200 W and 70 W of power applied, respectively. The etching was done in steps, to allow for topography measurements described in section 3.2.8 to control the etched depth.

3.2.6 Selective SiO_2 Dry Etching

The selective etching of SiO_2 was accomplished in a SPTS Primaxx system by employing multiple cycles of a stabilization, etch and pump sequence. The sequence starts by stabilizing the atmosphere at a flow of 1425 sccm of N_2, together with 210 sccm of ethanol flow for 2 minutes, followed by 10 minutes under this same flow plus 190 sccm of HF. The atmosphere is then evacuated for 30 seconds, and the cycle repeats three times.

3.2.7 Film Thickness Interferometer Measurements

For the measurement of transparent thin films, an OPM Nanocalc UV-NIS system was used. Prior to any measurement, the system was calibrated and aligned to each wafer. The system worked by fitting the interferometer data to achieve an estimate of the film's thickness, after defining the rough structure of the wafer's layers in the software. Measurements were done in pre-set points to achieve a map of the thickness, t, as a function of the position, in a total of 21 points. A value for the uniformity of the film was calculated, N_{unif}, dependent on the average thickness, $t_{average}$, and maximum and minimum measured thicknesses, t_{max} and t_{min}, respectively, as expressed in Equation (1).

$$N_{unif} = \frac{\left|t_{average} - \max\left(\left|t_{average} - t_{\min}\right|, \left|t_{average} - t_{max}\right|\right)\right|}{t_{average}} \times 100\ (\%) \qquad \text{Equation (1)}$$

3.2.8 Mechanical Profilometer Measurements

A KLA Tencor P-16+ contact profilometer system was used to perform profile measurements. The wafers were mounted in a motorized stage and held in place by a vacuum chuck. The scanning tip was then

lowered until it touched the wafer to “focus” the instrument. The motorized stage moved the wafer to the desired position to begin measurements. Sections of 500 μm were analyzed at a sampling rate of 200 Hz, while applying 2 mg force, with a scanning speed of 100 μm/s.

3.2.9 Scanning Electron Microscopy

For scanning electron microscope (SEM) image acquisition a FEI NovaNanoSEM system was utilized, prepared to accommodate 200 mm diameter wafers. The electron accelerating voltage was set to 2 kV and two different detectors, Everhart-Thornley Detector (ETD) and Through-Lens Detector (TLD), were used for magnifications smaller or bigger than 1000x, respectively.

3.2.10 Transmittance Measurements

A PerkinElmer LAMBDA 950 UV-VIS-NIR Spectrophotometer was used for transmittance measurements of PI thin film (Figure 25a). The system was first calibrated by acquiring a baseline curve for correction purposes. The samples were then mounted onto the device’s support (Figure 25b), and the transmittance measurements were done in 1 nm light wavelength decrements from 800 nm down to 250 nm.

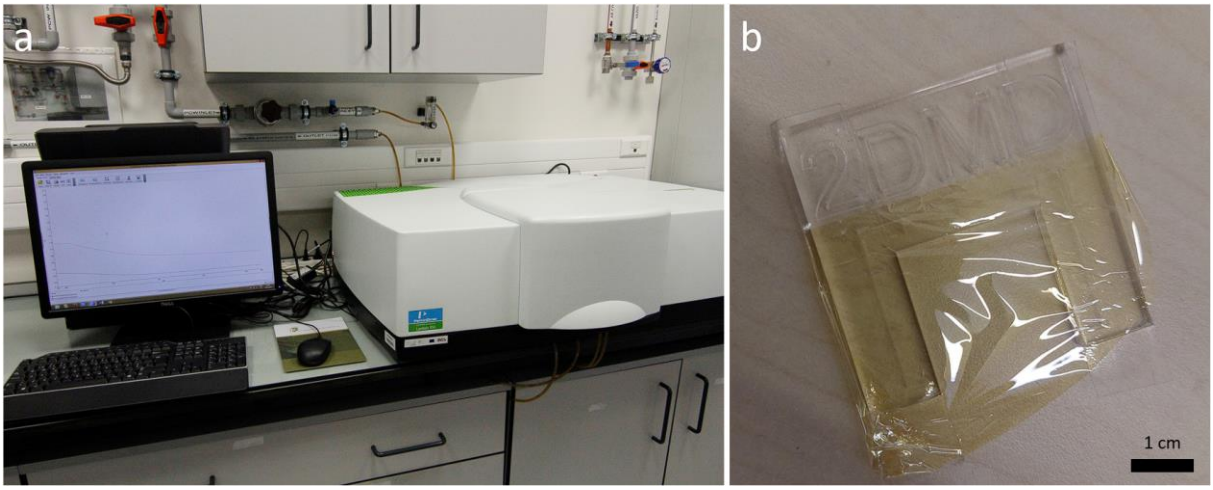


Figure 25 – Transmittance measurement setup.
(a) Utilized system setup for the acquisition of transmittance data. (b) Mounted PI film on the custom-made support for the measurements.

3.3 μLED Mounting

3.3.1 μLEDs

Two types of flip chip μLEDs, the LA HB12FP1 and the LA UB06FP2 (Light Avenue), were utilized. Their main characteristics are shown in Table 2.

Table 2 - Main characteristics of the utilized μLEDs.

μLED	**LA HB12FP1**	**LA UB06FP2**
Chip Size (μm)	$150 \pm 30 \times 300 \pm 30$	$89 \pm 20 \times 150 \pm 20$
Chip Height (μm)	80 ± 20	80 ± 15
Bond Pad Size (μm)	$75 \pm 15 \times 100 \pm 15$	$37 \pm 10 \times 53 \pm 10$
Forward Voltage	3.2 V @ 20 mA	2.6 V @ 1 mA
Radiant Power	20 mW @ 20 mA	15 mcd @ 1 mA

The LEDs are packaged in blue tape with contacts facing away from the glue. They were moved from the package manually by utilizing a tweezer and placed near the mounting site, aligned with the desired features. In the case of the smaller μLEDs, LA UB06FP2, an intermediate step was necessary between removing the device from the package and onto the mounting site as glue residues from the blue tape were left on its surface and complicated handling. This intermediate step was the immersion of the μLEDs in a droplet of isopropanol (IPA) that would remove these residues. After evaporation of the liquid, easier handling with tweezers onto the mounting site was possible.

3.3.2 Stamping, Picking and Placing

For mounting the μLEDs on the substrate with conductive glue, a wire-bonder TPT HB 16 with pick-and-place capability was utilized, with the aid of custom tips for stamping, picking, and placing. The conductive glue utilized was the Ablestik ABP 8037 TI (Loctite), which is an adhesive filled with silver particles that grants conductivity and is heat cured. It was maintained at -20°C and left to thaw for at least 1 hour before use. The utilized custom tips were ordered from SPT Roth Ltd, one for stamping (Figure 26c) and one for picking and placing the μLEDs (Figure 26d).

In the case of small chips, an appropriate holder of the TBT HP 16 was utilized (Figure 26a), although in the case of full wafers a custom holder was assembled in acrylic (Figure 26b). First, the stamping tip was assembled in position (Figure 26c) and a drop of conductive glue was dispensed near the mounting site,

for the stamping of the glue onto the pads. Only after this step, the first tip was replaced by the pick-and-place tip and the vacuum tube connected to its top end (Figure 26d). The µLEDs were then placed near the mounting site and manually aligned with tweezers, followed by the pick-and-place procedure.

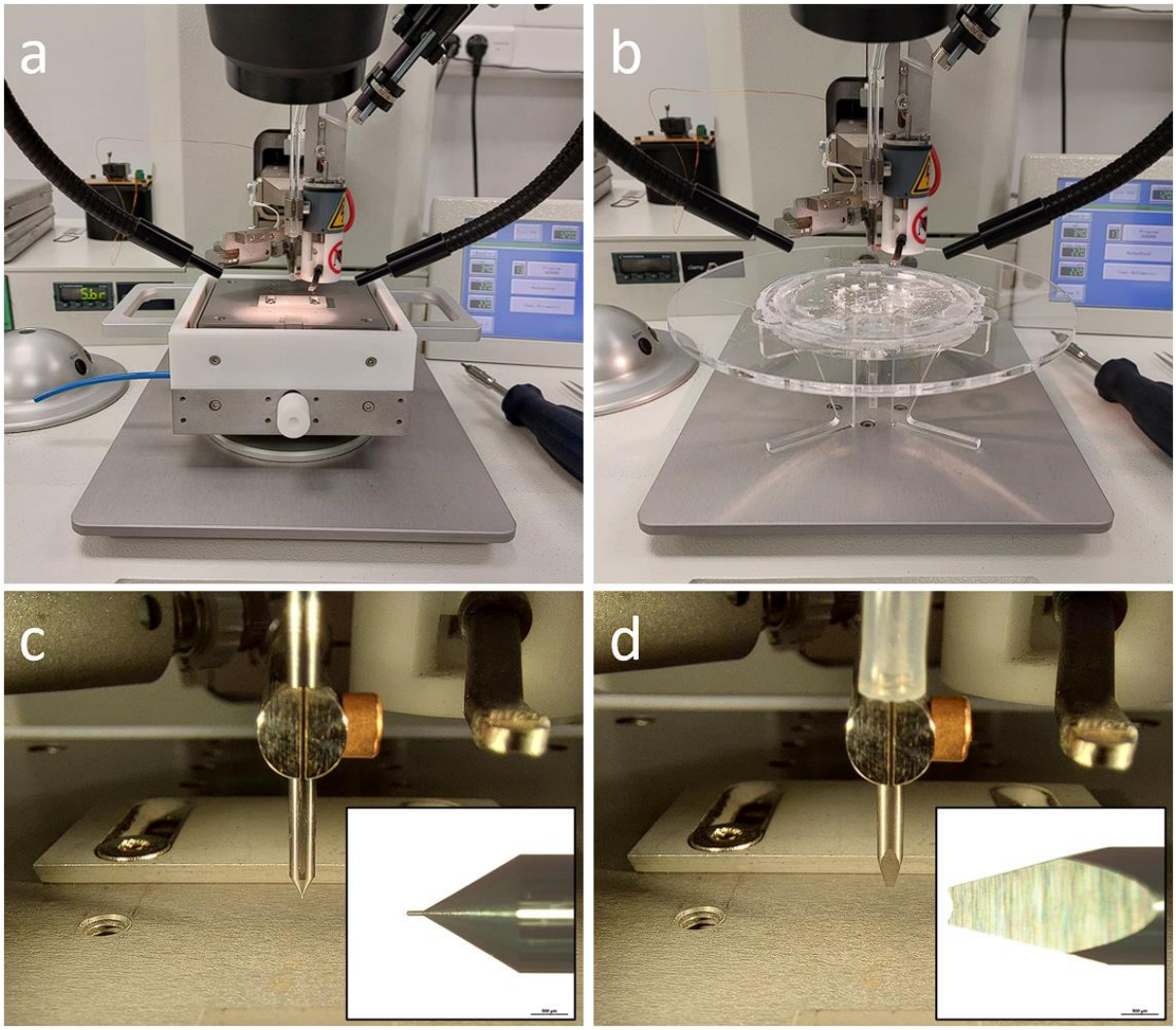


Figure 26 – System utilized for stamping and pick-and-place procedures.
(a) Chip holder for operation in the TPT HB 16. (b) Custom acrylic wafer holder. (c) Stamping tip mounted on the TPT HB 16. (Inset) Profile OM image of the stamping tip. (d) Pick-and-place tip mounted on the TPT HB 16. At the top the vacuum tube connection is observable. (Inset) Profile OM image of the pick-and-place tip.

3.3.3 Transparent UV-Cured Adhesive

The UV-glue utilized for dispensing on top of already-mounted µLEDs was 8424 UV (IQ BOND) and was applied by utilizing a custom-made tip in the TPT HB 16 system. High intensity UV light was used for curing the glue for 5 seconds.

3.3.4 Soldering μLEDs to Wafer

To mount the μLEDs via soldering, solder paste 4860P (MG Chemicals) was first utilized. It is a Sn63/Pb37 solder paste of Type 3, meaning it is comprised of particles between 25 μm and 45 μm. The recommended temperature for soldering reaches 225°C. By utilizing tweezers and a microscope, solder particles were placed on top of the μLEDs' electrodes and Au tracks of the fabricated wafers, followed by heating on a hotplate.

To expose the samples to lower temperatures, Sn42/Bi57.6/Ag0.4 solid core solder wire (Chipquik) was also used. It was scrapped against a glass slide to achieve small pieces, adequately sized about the tracks where mounting was expected. This solder could be used at temperatures lower than 150°C, with its melting point at 138°C. It was applied both in bare Au tracks and in Au tracks covered by electroplated Ni.

3.3.5 Ni Electroplating

To test the compatibility of soldering to a wafer with a Ni layer, a custom electroplating setup was devised (Figure 27) to achieve a Ni layer on top of the already present Au tracks on the wafer without needing a more complicated process.

For this, a NiCl electrode in contact with a $NiSO_4$ solution with an undisclosed concentration was utilized as the electrolyte to create an electrolytic cell. An external power supply was utilized to provide the driving force for the reaction to occur, with a -4 V voltage being applied to the Au tracks where one wanted to deposit the Ni, while the anode was connected to ground. With a marker, a region on top of the wafer was delimited and a drop of the electrolyte solution was placed in the middle. Due to the hydrophobic nature of the marker's ink, the droplet would stay in place. The negative voltage was applied at the Au tracks, outside of the droplet zone and the ground was connected to the electrode touching the droplet. The electroplating took place for approximately a minute.

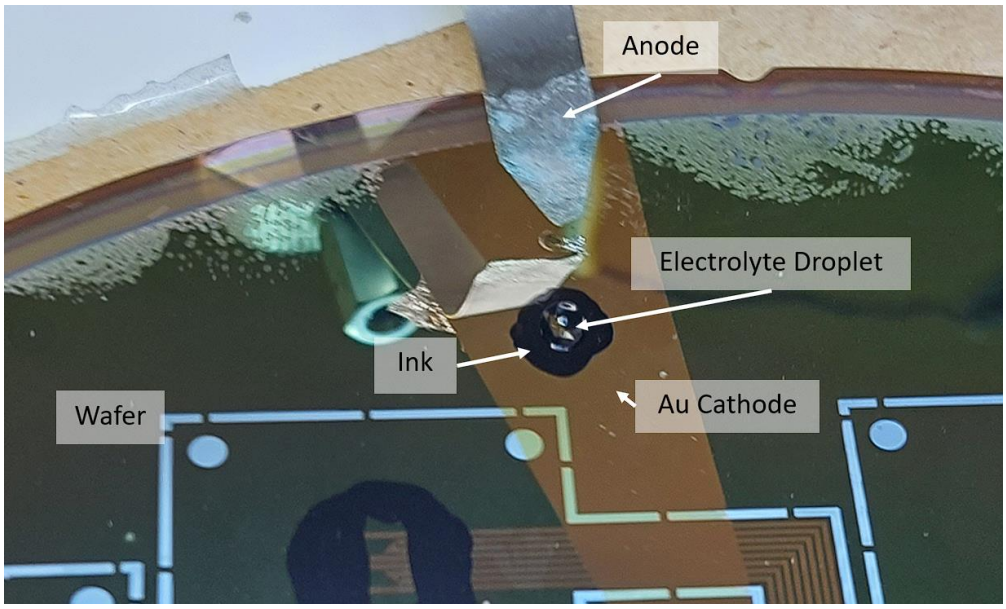


Figure 27 – Utilized electroplating setup.
To start the electroplating, the cathode is connected to the negative voltage of the power supply, whilst the anode is connected to the positive one while in touch with the electrolyte. Notice how the ink prevents the droplet from spreading.

3.3.6 µLED I-V Curve Acquisition and Optical Power Measurements

The setup comprised a Keythley 2400 for power supply and voltage measurement, a Thor Labs S121C photodiode power sensor, a Thor Labs PM101 power meter, and Thor Labs Optical Power Monitor software for optical power measurements (Figure 28b).

Two micromanipulator tips connected to the power supply were in electrical contact with the tracks connected to the µLED electrodes. The sensor was connected to a computer with the required software installed and configured for 450 nm wavelength light. To align the photodiode power sensor to the µLEDs, these were first powered with a current of 20 mA. The sensor was moved in plane until the measured power output was maximum for that given current, meaning correct alignment was achieved. As the µLEDs were mounted on a wafer and the circuit was subject to Au track's resistance, R_{Track}, and contact resistance, $R_{Contact}$, between the device and the tracks, these needed to be considered, as denoted in Figure 28a. The I-V and the Optical-Power-I point present in the datasheet (TABLE) for $I = 20\,mA$ was utilized. Initially, the power supply was utilized as current source and set to $I = 20\,mA$, and it was assumed that the voltage between the µLED's pads was $V_{LED} = 3.2\,V$. The resulting voltage present at the two ends of the circuit was then used to calculate the resistance associated with $R_{Total} = 2(R_{Track} + R_{Contact})$. Different voltages were then applied to the circuit's ends, the current was

measured and V_{LED} was calculated considering R_{Total}. For each of these points, the measured optical power, $P_{Optical}$, was registered.

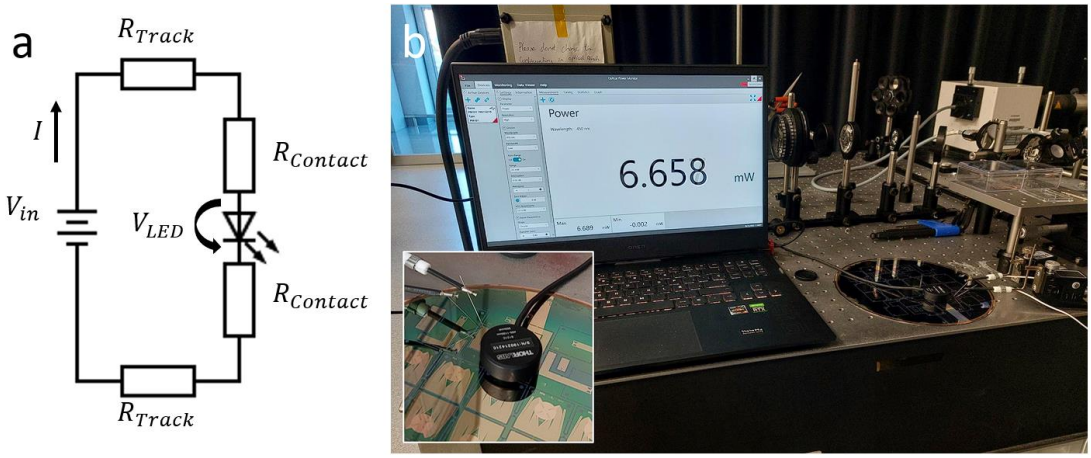


Figure 28 – Setup for μLED related measurements.
(a) Schematic of the circuit comprised of the μLED, the Au track and contact associated resistances, and the voltage source. For the initial measurement, the voltage source was substituted by a current source. (b) Utilized setup for simultaneous measurement of I, V_{LED}, and $P_{Optical}$. The photodiode was aligned with the μLED by moving the former in-plane until the measured $P_{Optical}$ was maximized. (Inset) The micromanipulator's tips were in contact with the Au tracks connected to the μLED away from the photodiode and thus, a significant track resistance was associated.

3.4 Graphene Dry Transfer

3.4.1 CVD Graphene Growth

Continuous graphene samples were grown by 2D Materials and Devices' researchers at INL facilities in an EasyTube ET 3000 CVD system made by CVD Corp., USA.

Two types of continuous graphene samples were prepared, differing only in the pre-CVD process. The first type (OxGr) of samples consisted of mostly monolayer continuous graphene with few nucleation sites while the second type (noOxGr) possessed a high number of regions of multilayer (>1 layer) graphene with a large density of nucleation sites. Both were grown on 25 μm thick Cu (99.99+% purity) foils with varying sizes and chemically treated by immersion in a dilute solution of $FeCl_3$ and HCl to remove surface impurities and reduce rugosities. The OxGr samples had the Cu foil pre-oxidized on a hotplate at 250° C for 20 minutes to create a Cu oxide surface (Figure 29) and reduce nucleation sites during graphene growth while the noOxGr samples did not. Graphene growth followed on these Cu foils by placing them inside a three-zone quartz tube furnace. The growth process started by evacuating the chamber to approximately 10 mTorr and then filling it with 250-sccm Ar and 170-sccm H gas mixture. Once the growth temperature and pressure were reached, the carbon precursor was introduced into the chamber (1.25 sccm CH_4). Graphene growth was carried out at 1040 °C and 6 Torr for 1 hour on both sides of the copper foil.

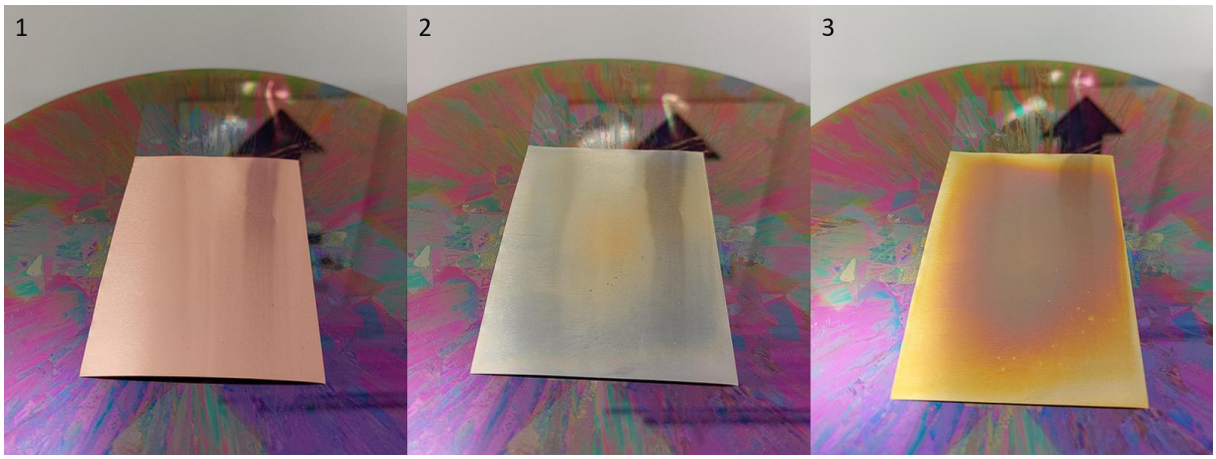


Figure 29 – Appearance of the 25 μm thick Cu foil before (1), after 5 minutes (2) and after 20 minutes (3) of being heated on a hotplate at 200° C.

3.4.2 Wet Transfer

Graphene wet transfer was achieved similarly for both types of OxGr and noOxGr samples. It followed a similar process to the one depicted in (Figure 5). First, PMMA was spin-coated on top of the as-grown graphene/Cu samples and let to dry overnight. To prepare for the etching of the substrate, the backside of the sample is etched for 1 minute in an O_2 plasma to remove graphene grown on this side that would prevent the etchant to come into contact with the Cu. Next, the PMMA/graphene/Cu stack was left afloat on a 0.5M $FeCl_3$ solution for 2 hours until all the metal was dissolved, with only PMMA/graphene remaining. The stack was then scooped with a fishing tool, comprised of an Si wafer, and moved onto a container with DI water for 5 minutes, followed by a second scoop and transfer onto an HCl 2% (w/v) solution for 20 minutes to remove leftovers from the first etching solution. The operation is repeated twice, each utilizing fresh DI water to reduce contamination of the target substrate. After scooping the graphene onto the target substrate, the PMMA/graphene/substrate stack was then left to dry at an angle overnight, as a thin DI water layer remained intercalated between the graphene and the substrate. Leaving the stack at an angle eases the water removal by gravity. The final step was the removal of the support PMMA layer by immersing the stack in acetone for 2 hours, followed by immersion in IPA to remove the solvent's leftovers, and finally, the remaining graphene/substrate stack was blow-dried by N_2 gas flow.

3.4.3 Water Intercalation

The simplest approach utilized to induce oxidation of the graphene interface was water intercalation. This was mainly achieved by immersion of the graphene/Cu samples in DI water containers at room temperature. The containers were covered to protect them from airborne particles or contaminants, for a varying period. Occasionally, the DI water was heated to 50° C. An alternative method was also utilized, based on water vapor saturation. The graphene/Cu samples were left inside a tin and placed inside a furnace at 50° C for varying time intervals. The tin had DI water and the graphene/Cu samples were placed on top of a platform to keep them dry (Figure 30). A lid was used to cover the tin and a cloth placed at the bottom of the lid so condensed water would not precipitate on top of the Cu/graphene.

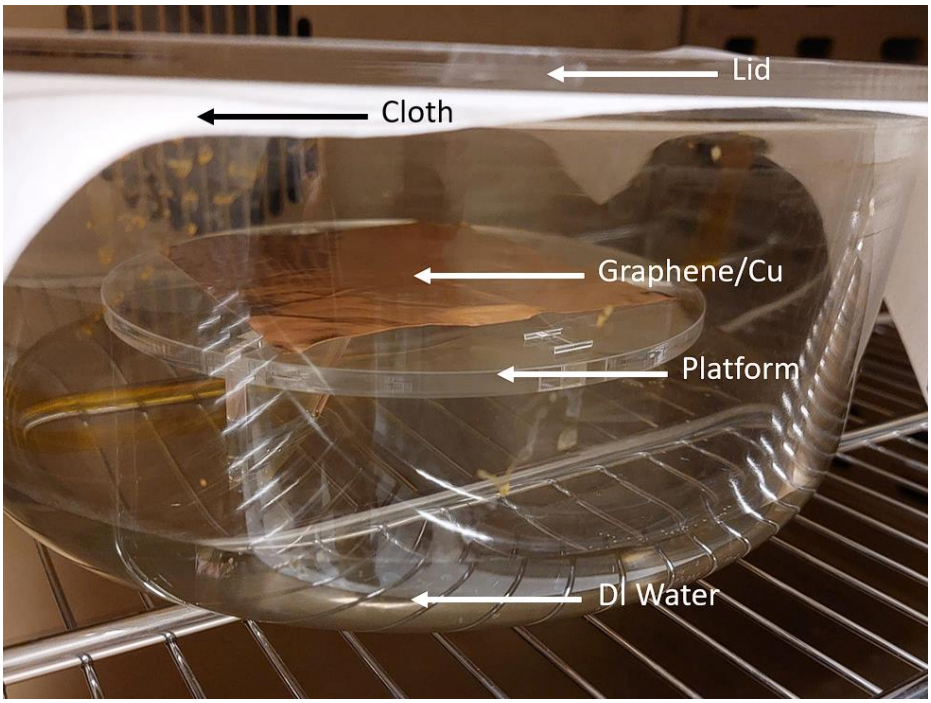


Figure 30 - Utilized setup to achieve water vapor oxidation inside the furnace.
The lid and platform were custom made in 5 mm thick acrylic.

3.4.4 Laminator Approach

Blank water transfer printing foils were purchased from Stardust Colors and consisted of a 25 μm thick PVA sheet attached to a white support paper. The utilized laminator was the commercially available Akiles Pro-lam photo 6.

The lamination process is depicted in Figure 31. First, after the utilization of a decoupling process, the graphene/Cu samples were placed on top of the PVA foil (with the support film) with the graphene and the PVA facing each other, and the stack was placed on top of a thin flat surface (Figure 31.1). The PVA foil could also be taped onto the flat surface as heating may cause it to deform and detach unintentionally. Next, the stack was enclosed in parchment paper and laminated at the desired temperature (Figure 31.2). Parchment paper was used to avoid PVA sticking to the laminator's rolls. Immediately after lamination the stack was placed on top of a hotplate for about a minute at the desired temperature. A flat weight was placed on top of it to ensure good adhesion between the PVA and graphene, while also avoiding deformation of the PVA foil, and improve contact between the stack and the hotplate for homogenous heat transfer (Figure 31.3). After cooling down the sample with the weight on top of it, the Cu foil was peeled from the PVA foil and a darker patch was visible on top of the polymer, hinting towards a successful transfer (Figure 31.4). After picking the target substrate, the graphene/PVA was laid on it with the graphene contacting its surface and again enclosed in parchment paper followed by lamination at the

desired temperature (Figure 31.5). If this substrate was rigid, there was no need for a thin flat surface, otherwise, a process similar to Figure 31.1 can be executed. Again, similarly to Figure 31.3, the stack was baked on a hotplate at the desired temperature for about one minute while a flat weight applied pressure on it (Figure 31.6). Next, the weight was removed, the support film was carefully peeled while the stack was still on the hotplate, and the sample was maintained at the hotplate for another minute at the same temperature (Figure 31.7). Peeling while hot ensures easier detachment of the support film. Finally, the last step was to immerse the PVA/graphene/target substrate in DI water to dissolve the PVA overnight (Figure 31.8). To clean the sample, ethanol, IPA and water were used to rinse it followed by blow dry with an air gun.

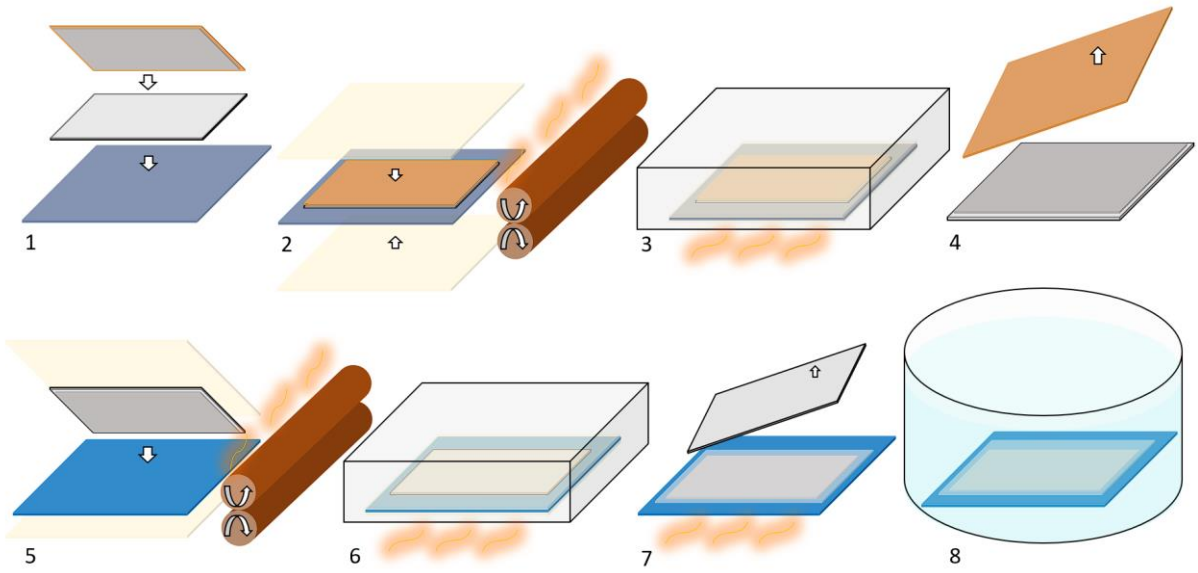


Figure 31 – Schematic of the graphene dry transfer with the laminator approach.
(1) The graphene/Cu is placed on top of the PVA foil, and a rigid thin flat surface is used to maintain the stack flat. (2) Parchment paper is used to enclose the stack followed by hot lamination. (3) A hot bake is done on top of a hotplate while a flat weight applies pressure to ensure good physical contact and even heat transfer. (4) After the bake, the sample is let to cool down and the Cu is ready to be peeled off and the graphene is successfully transferred onto the PVA/support film. (5) The graphene/PVA/support film is placed on top of the desired substrate and enclosed in parchment paper followed by lamination. (6) Again, a bake on top of a hotplate is done while a flat weight applies pressure. (7) The peeling of the support film is done still on top of the hotplate followed by some more time of baking. (8) Finally, the sample is immersed in DI water to dissolve the PVA and finish the transfer.

3.4.5 Spin Coated PVA Supported Transfer

One other option to the use and lamination of PVA foils onto graphene/Cu was the direct spin-coating of PVA on top of the graphene while still on the growth substrate. This was achieved by first preparing a 9% (w/w) solution of PVA by adding 9 g of PVA pellets to 91 mL of DI water at 90° C. The solid PVA was gradually added to the water under stirring and left overnight to completely dissolve the polymer. Then,

the graphene/Cu was placed on a support substrate and fixated with Kapton tape while ensuring its flatness. It was then placed and aligned on the spin-coater Polos SPIN150i and held by vacuum followed by the manual dispensing of the PVA solution until the whole sample was covered. The spin-coating procedure then started, being comprised of a first spreading step of 30s where the spin-coater reached 300 rpm after 2 seconds followed by another step of 30s where the spin-coater reached 750 rpm after 4 seconds. The spin-coated PVA was then cured in one of two ways:

- Curing at room temperature over a period.
- Curing at 120° C over 2 minutes on a hotplate.

After curing, the PVA was peeled off the copper, carrying the graphene with it, leaving behind the Cu growth substrate (Figure 32a). The peeling started at one of the edges and then slowly and carefully progressed towards the remaining areas.

Transfer onto the target substrate happened in one of two ways. The first is lamination utilizing the same process in (Figure 31.5-8) without the removal of PVA's support film step, as there is no support film. The second process involved the wetting of the target substrate with IPA followed by carefully lying the PVA/graphene stack on the wet surface with the graphene facing down (Figure 32b). By surface tension forces, the stack gradually flattened and adhered to the substrate. Leaving the PVA/graphene/IPA/target substrate at room temperature resulted in an evaporation of the IPA. Drying at an angle helped IPA flow from under the graphene and evaporate, similarly to water removal step in the wet transfer. Finally, after around 1 hour, the stack became PVA/graphene/target substrate (Figure 32c) and was then immersed in DI water to dissolve the PVA. In the end, the graphene/target substrate were rinsed with ethanol, IPA and DI water followed by a blow dry to clean the sample.

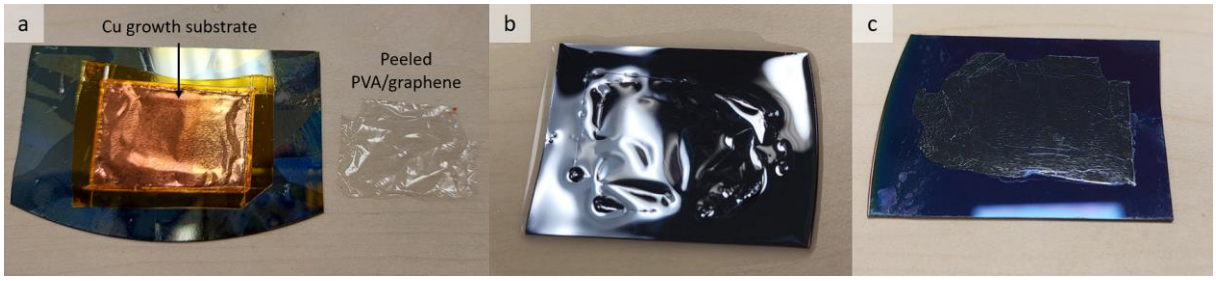


Figure 32 – Transfer process with spin-coated PVA.
(a) Image of a peeled PVA/graphene sample and the corresponding target substrate. (b) PVA/graphene sample in (a) placed on top of the IPA-wetted target substrate surface. The graphene is facing the IPA. (c) Sample in (b) after 30 minutes of exposure to room temperature. Some wrinkles can be observed, as the substrate was not let drying at an angle.

3.4.6 H_2 Intercalation

To intercalate H_2 molecules in the graphene/Cu interface a Roth and Rau Microsystems MicroSys 400 was utilized. After growing graphene on Cu foils by the already described CVD process, the intercalation process was started by evacuating the chamber followed by heating up to 250° C. At that point, H_2 was released onto the chamber to achieve an atmosphere of 10 mbar that was held for 3 hours. The chamber was then once again evacuated and let to cool down to 100° C, where it was vented to atmospheric pressure, finalizing the process. After this, a water immersion process followed as described section 3.4.3.

3.4.7 Raman spectroscopy

Raman shift measurements and associated Raman images were taken in a WITec Alpha300M+ with a 532 nm wavelength laser and a motorized stage. The laser was set to 2 mW on all samples and a grating of 600 mm^{-1} for spectra acquisition was used. Each spectrum was obtained by integrating the Stokes shift signal over 0.5 s and averaging over 10 acquisitions.

Measurements were done to evaluate graphene's most prominent peaks, being the D, G and 2D (or G') at around 1350 cm^{-1}, 1580 cm^{-1} and 2700 cm^{-1}, respectively. For every measurement the focus was adjusted until the 2D graphene's Raman peak was maximized to ensure optimal laser focusing onto the sample and efficiently compare different locations' spectra.

3.4.8 Graphene Resistance Measurements

Resistance measurements were achieved by utilizing a Keithley 2400. Two-point and four-point resistance measurements were done by utilizing either two micromanipulators with attached conducting tips or a home-made 4-point setup, respectively. The instrument's configuration was changed according to each type of measurement. In some instances, a multimeter was utilized for more rough estimates of graphene sheets' resistance.

3.4.9 X-Ray Diffraction

X-Ray Diffraction (XRD) measurements were performed on a PANalytical X'PERT PRO MRD. The X-Ray source was a copper anode, with a major line $K\alpha = 0.154$ nm. Different samples of the same Cu foil after CVD graphene growth, decoupling by interface oxidation and transfer were mounted on a glass substrate

and then fixated on the machine (Figure 33a). The device is composed of a detector, a sample holder, and an X-Ray Source.

The two utilized protocols were the Theta-2Theta (T2T) measurements and Pole Figure (PF) measurements. Prior to any measurement, alignment of the setup was necessary after sample fixation. First, the sample was lowered in z in order to leave the a clear path between the X-ray source and the detector and a scan around $2\theta = 0$ was performed to center the detector around the maximum intensity, meaning the source and detector were aligned, to correct the offset. Next, a scan in z was performed and a step signal was acquired, where the middle of the slope corresponded to the desired position where the sample was aligned with the detector. Then, with 2θ and z already in the desired alignment, a scan around $\omega = 0$ was performed to find the value in which a greater intensity is detected, indicating an aligned sample and allowing for offset correction. Finally, a similar scan in χ was also performed with the same goal. These alignments in z, ω, and χ were iteratively done to progressively align the sample to a greater extent.

With alignemt procedures complete, T2T measurements were performed. These measurements consisted in scanning different values of θ to find the peaks corresponding to each crystallographic plane parallel to the sample's surface, associated to a value of d (Figure 33b). In the present equipment, the T2T was done by scanning ω and 2θ in such a way that $2\omega = 2\theta$, and thus ω and θ are equivalent. Varying ranges of scans where done in order to acquire more precise measurements of desired peaks, namely the peak associated with (111) crystallographic plane, close to $\theta = 43.3º$.

For PF measurements, the peak around which the procedure would be done was selected. So, in PF measurements, after the setting of the the θ and 2θ angles to the desired peak, a scan was performed in χ and φ, and information was obtained as a function of these two variables. In each measurement, after sample alignment as already described, φ and χ were scanned in 2.5° increments in the ranges of $[0°, 360°[$ and $[0°, 85°]$, resulting in 144 and 35 discrete steps for each parameter, respectively, and a total of 5040 detected (φ, χ) intensity data points for each sample. These were plotted utilizing standard stereographic projections of the intensity points onto the equatorial plane of the sphere defined by the scanning of φ and χ. The relationship between φ and χ and the corresponding polar coordinates of the pole figure can be given by Equation (2) and Equation (3), where ρ and ϑ denote the radius and angle of polar coordinates, respectively, and R is the maximum radius of the projection.

$$\vartheta = \varphi \qquad \text{Equation (2)}$$

$$\rho = R \times \tan\frac{\chi}{2}$$ Equation (3)

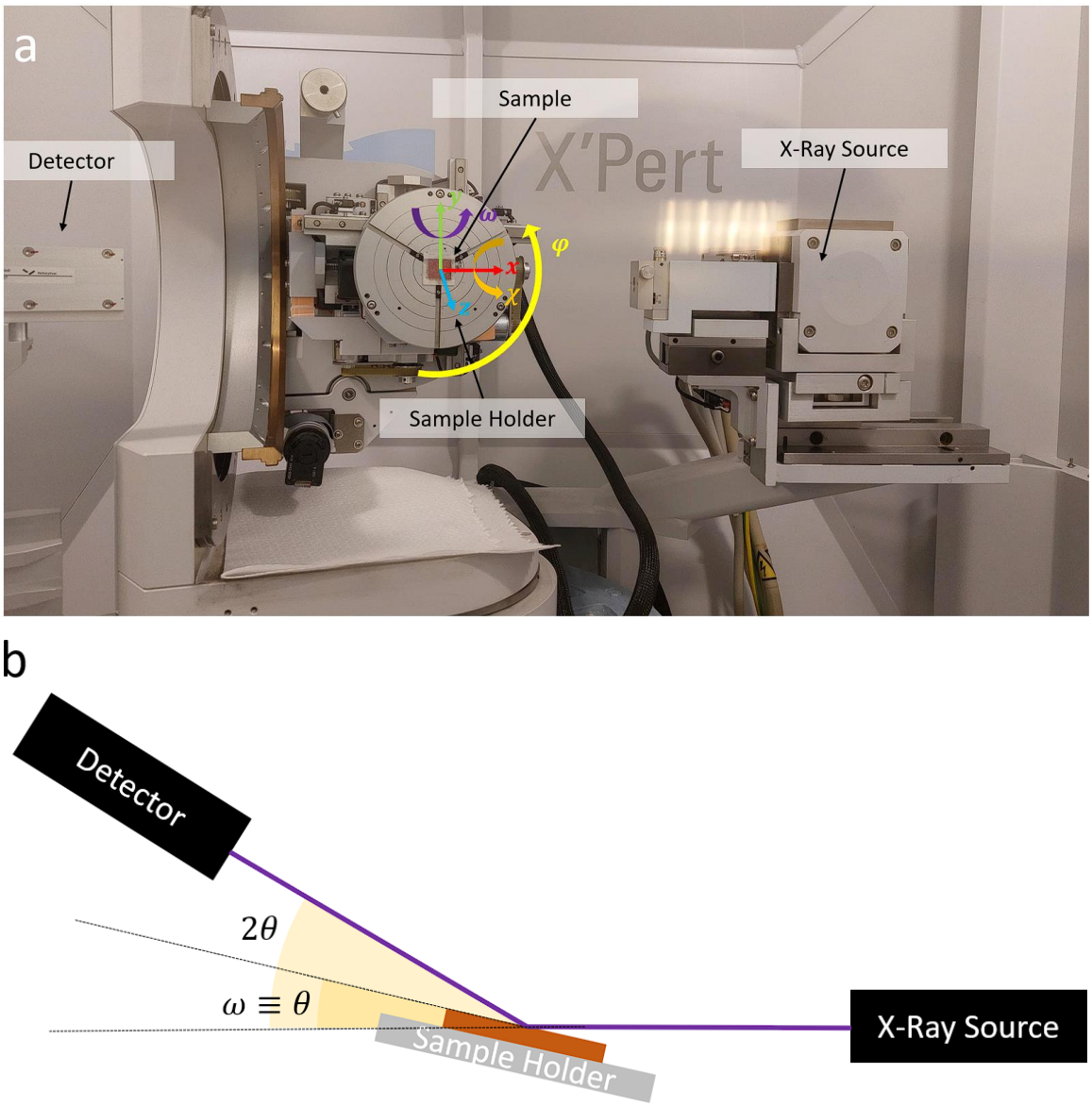


Figure 33 – Setup for XRD measurement.
(a) Utilized setup for the XRD measurements. In the picture there is depicted the sample's reference frame and the associated axis of rotation for each parameter. (b) Bottom view schematic of a T2T measurement. As the X-Ray source is fixed, ω has a similar role to θ.

4. Device Development

The device design and fabrication in this thesis was part of the NeuralGRAB project which aims to develop a novel neural interface for in vivo neurochemical detection. A graphene multi-transistor chip fabricated on top of a Si wafer for electrolyte gated GFET detection of neurotransmitters had been developed previously to this dissertation work [10]. One of NeuralGRAB's goals is to establish a fabrication process for GFETs on a flexible substrate and to integrate μLEDs capable of optical stimulation of transgenic mice brain tissue, working towards an implantable neural interface for neurotransmitter detection and optogenetic stimulation. Thus, the device developed in this work contributes to that goal.

The previously developed device on a Si/SiO_2 rigid substrate is an electrolyte-gated GFET array, with each transistor comprised of Au drain and source contacts connecting to a graphene channel and a receded Au gate. The graphene was wet transferred onto the wafer after the Au contacts were patterned, followed by the graphene channel lithographic patterning. All the device's sensing surface is passivated with a multiple stack of SiO_2 and Si_3N_4 apart from the graphene channel and the gate, which will remain exposed to the electrolyte. The rigid device possesses two transistor groups of 16 GFETs, each with individual drains and common sources and two gate terminals, totaling 40 connections (Figure 34). After fabrication on the Si wafer, individual chips are diced and then mounted on a PCB, where each of the 40 connections is wire bonded to the PCB. The PCB can then be plugged into a custom acquisition platform that allows for modulation and reading the GFETs' response. The data acquisition is done by biasing the GFETs at a given drain-source voltage and then sweeping the gate voltage while recording the current passing between the source and the drain. This enables plotting of the I-V curve of the GFET and tracking the Dirac point, which can be used for biosensing, as described in section 2.1.5. The sensor is capable of achieving a LOD of 1 aM and provide a selectivity against chemically similar molecules.
The selectivity and sensitivity towards the desired neurotransmitters are achieved by a functionalization process, which is described in appendix I, exposing the device to different solutions that change the GFET I-V curve (tracked via the acquisition platform). The desired samples can then be analyzed by being brought in contact with the GFETs in a liquid environment.

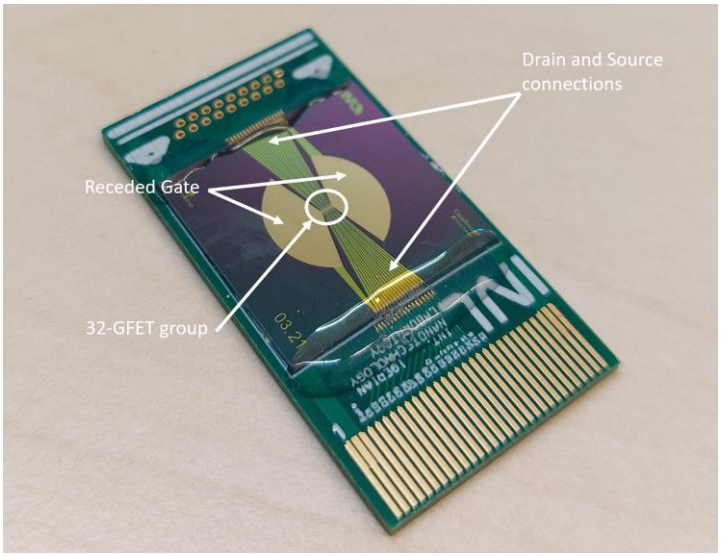


Figure 34 – Electrolyte-gated GFET array biosensor previously developed in the NeuralGRAB project. Courtesy of Mafalda Abrantes (unpublished results).

The new device developed in this dissertation aimed to succeed to the rigid one, adopting the same GFET-based architecture, but in a flexible substrate, capable of performing ex vivo neurotransmitter detection. The device developed in this thesis should integrate μLEDs to allow for optical stimulation of genetically modified brain tissue. Because the devices should be flexible, a flexible substrate is required. Achieving these goals paves the way for the future implantable device, since the developments on the flexible substrate fabrication can then be easily adapted and scaled to a smaller size device that can be implanted in the brain.

As the new device succeeds to the old one, it was essential to maintain enough similarities between the two to allow for performance comparison for validation purposes. As such, changing the device's variables was minimized. To achieve this, the new device was developed to minimize layout differences and allow for operation utilizing the same acquisition platform. There were also other limiting factors on the development that narrowed design possibilities. The limited time frame for the development of this project meant that exploring new fabrication techniques not commonly performed at INL was risky, and established techniques would render faster and more reliable results, so they were preferred. The project had already acquired LA HB12FP1 μLEDs, and thus the design also had to revolve around their geometry, mechanical and electrical properties, namely their size and operation current.

The fabrication of GFETs requires micro-fabrication techniques, as their features are in the order of the micron, and thus lithography is essential. The tracks required to power the μLEDs are in the orders of hundreds of microns but still require micro-fabrication techniques. These would allow for GFETs and μLEDs homogeneous integration in the same chip but considering the μLEDs' thickness this option was

a no-go. The μLEDs' thickness is 3 orders of magnitude higher (tens of microns) than that of the remaining features (tens of nanometers). This gives rise to a problem, as the surface of the device should be as flat as possible to ensure good contact between the neurotransmitter sample and GFET sensor.

With all these limitations in mind, a three-part device design was devised (Figure 35). Each of these parts would have its purpose, and each would deal with its specific design challenges. The three parts are the GFET array, the Spacer, and the μLED array.

As the name implies, the GFET array comprises all the GFETs in a flexible substrate. This is the top layer with the finest features and is the only one requiring graphene. The μLED layer accommodates the μLEDs and tracks suited to power them, and represents the bottom layer. By isolating this layer from the rest, one can physically separate the more delicate GFET array from the μLED layer, of which the assembly process is in principle more residues prone and confine the higher voltages and currents required for μLED operation. The remaining layer, the Spacer layer, is required to match the μLEDs and the top layer that have features with very different thickness. The Spacer layer has pre-patterned holes and a thickness slightly greater than that of the μLEDs so that when assembled on top of the μLED layers, one can achieve a flatter surface that can then accommodate the assembly of the GFET array.

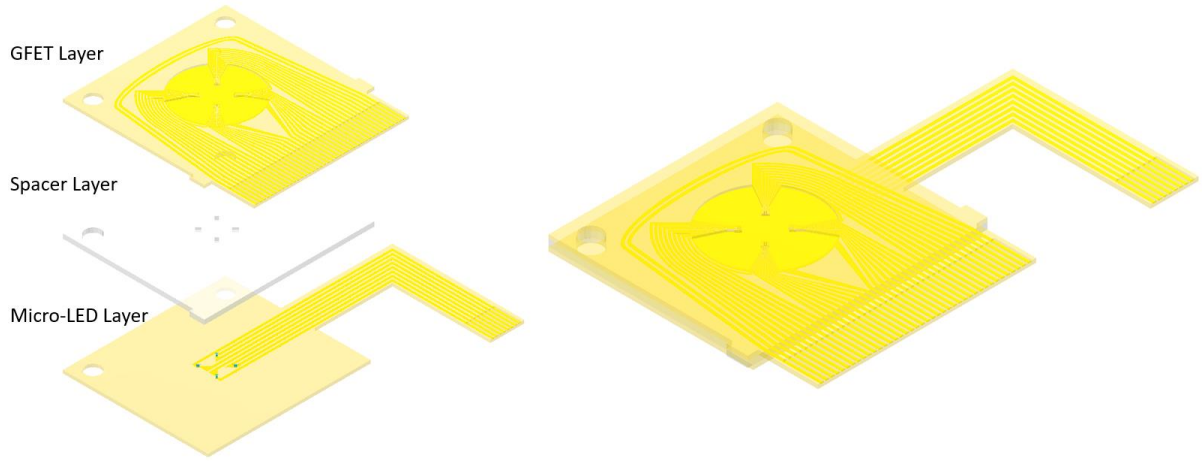


Figure 35 – Schematic of the three different layers (left) that, after assembly, would comprise the whole device (right).
Vertical dimensions are not to scale, as real thicknesses are too small.

With each layer's roles defined, the device's functionality led to various design considerations. Assembly of the device's successive layers can be tricky, and thus, alignment holes were open in every layer to facilitate it, similarly to the device in [7]. Furthermore, a reliable zero-insertion force (ZIF) connector connecting to the data acquisition platform was proposed ensuring a stable signal flow to and from the control electronics, [11], [106], [142], [144], [145]. A standard 500 μm pitch connection layout utilized in many ZIF connections was suggested. Also, as the circuitry powering the GFETs and the μLEDs was in

different layers, utilizing two different ZIF connections distant enough from each other was adopted. This has the advantage of isolating circuitry where the current would never surpass 1 μA from circuitry where the current could reach 10 mA, as is the case for the GFET and μLED layers, respectively, preventing crosstalk between conducting lines. Finally, the chip's size, similar to the rigid chip, was chosen for future experiments to accommodate a whole mouse brain slice, for possible ex vivo experiments.

These general remarks about the device and its context set the basis for the design and development of the remaining parts. Its development started with sketching a fabrication process and defining a suitable layout, which was partially tested in two wafers. Also, the integration of μLEDs was explored (see section 5), and a dedicated wafer for its development was fabricated, with a fabrication process very similar to the device's wafer (see appendix II and III, respectively), used to validate some fabrication steps. The wafers fabrication process will be addressed in the following sub-section. A brief description of the spacer layer is provided in appendix IV.

4.1 Layout and Fabrication Process Design

Designing the chip's fabrication process and layout required considering multiple aspects. The GFET array and μLED layer, requiring microfabrication techniques, were done on top of Si wafers, making them easier to process with standard techniques. The Spacer layer, due to its comparatively high thickness, would be unsuited to microfabrication processes and its process is discussed in appendix IV. Before any layout definition, the materials and fabrication process sketch were first defined. The main aspects considered during this process were as follows:

- GFETs: these had to maintain the same morphology and working mechanism as the previous rigid device. Au tracks should be deposited before the graphene, or in other words, the graphene should contact the drain and sources from above. Also, the gate electrode should be made of Au and as large as possible.
- Flexible and Transparent Substrate: the device should be flexible, so it is imperative to use a flexible substrate like PI or PET (see Table 1). Furthermore, the GFET array will be stacked on top of the μLEDs layer, meaning it will have to transmit the wavelength in which the μLEDs emit light. Key aspects also considered are that this substrate should be biocompatible and withstand the fabrication process, namely high temperatures, as many processes cause the heating of the

wafer. It should also be able to withstand the functionalization process, which entails chemically aggressive solvents like dimethylformamide (see appendix I).

- Device Releasing: fine features require lithographic processes commonly done on Si wafers. Fabrication is possible on top of these wafers by depositing the desired substrate on them and executing all the processes. This then requires the release of the fabricated devices from the Si wafer, a process of its own.

These considerations led to the proposed device structure and a sketch of the fabrication process steps in Figure 36. The fabrication will start with depositing a sacrificial SiO_2 layer (Figure 36.1) to release the device in the final step (Figure 36.9). The spin-coating of PI will follow, as it is a biocompatible and transparent film, capable of withstanding temperatures above 300° C and dimethylformamide exposure (Figure 36.2). Patterning of conducting tracks follows, utilizing a thin Cr layer to improve adhesion between the PI and the Au (Figure 36.3). The next step will be transferring and patterning the graphene and completing the transistors (Figure 36.4). To ensure the device passivation, first, a Ni-stopping layer will be patterned in every area where one wants to open vias on the passivation layer (Figure 36.5). This layer prevents the via-opening process from damaging the device's structures, such as the graphene or the Au tracks. A second PI layer will be spin-coated to ensure device passivation (Figure 36.6). As the utilized PI is not photosensitive and thus not photolithographically patternable, a sacrificial layer of AlSiCu will be patterned on top of the PI passivation layer (Figure 36.7). The AlSiCu sacrificial layer will act as a mask and allow for etching the PI only on AlSiCu unprotected areas. These unprotected areas are the openings of the device's vias and the defined cutouts of the GFETs' and µLEDs' layers. After the etch, the AlSiCu and stopping layer will be removed, leaving the device with open vias and defined cutouts (Figure 36.8). To finalize the fabrication, the device will be released, which is done by selective etching of the SiO2 sacrificial layer deposited in the first step (Figure 36.9). A more detailed representation of the proposed fabrication process can be seen in appendix V.

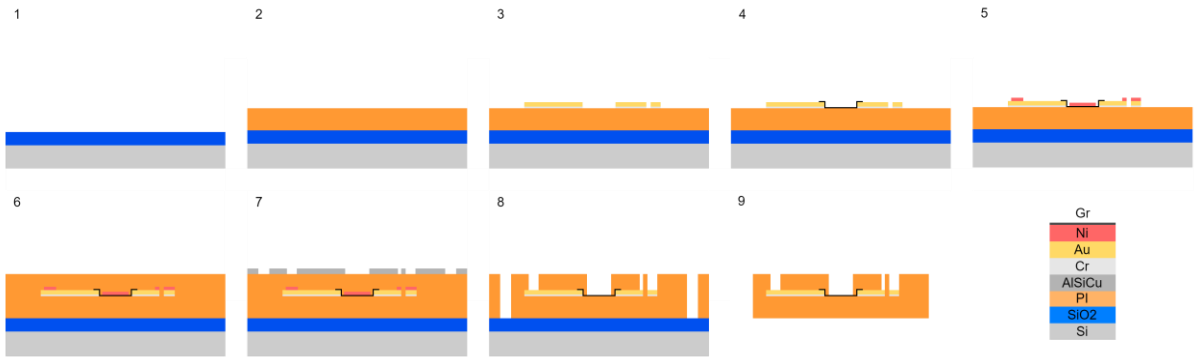


Figure 36 – Schematic of the different steps necessary for the device fabrication.

(1) SiO_2 sacrificial layer. (2) Spin-coating of PI. (3) Patterning of Au/Cr tracks. (4) Graphene transfer and patterning. (5) Patterning of stopping layer. (6) Spin-coating of the PI passivation layer. (7) Patterning of AlSiCu sacrificial layer. (8) Etching of vias and device cutouts. (9) Device release.

After sketching the fabrication steps of the device, the device's layout was readily defined, as depicted in Figure 37. Both the GFET array and the µLEDs layer were designed considering the same fabrication steps and thus share the same layers, except the layer corresponding to the graphene patterning, as the µLEDs layer does not possess any graphene regions.

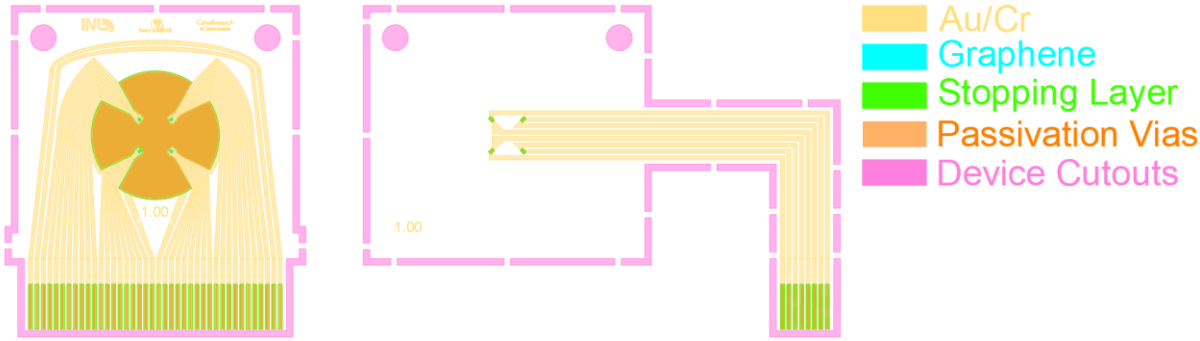


Figure 37 – Overview of (Left) the designed GFET array layout and (Right) the designed µLEDs Layer.

The GFET array layout presents 32 GFETs, each 75 µm in width and 25 μm in length, arranged in 4 groups of 8 transistors each, with individual drains. Only two source tracks connect to 16 transistors on either the device's left or right side. A giant gate electrode is present at the center of the device, which is 1 cm in diameter, with two redundant tracks for contacts. The chip also has two tracks going around the devices, which will connect to the ground to create a ground plane that can contribute to reducing possible noise or capacitive interferences. All the tracks then connect to the bottom of the device where a 500 µm pitch ZIF connector layout was adopted, totaling 40 connections.

The device's radially symmetric shape maintains the transistors in similar conditions, namely the distance to the gate electrode. GFETs in the rigid device were all significantly close to the gate area, as it was possible to connect the tracks to different sides of the chip. In the present case, all the tracks must converge to the ZIF connection side, which limits possible arrangements and increases tracks' resistances. Furthermore, the transistor arrangement in each group is done to maximize the density of devices, similarly to the rigid device, while at the same time restricting each group of 8 transistors to the area directly above the µLEDs.

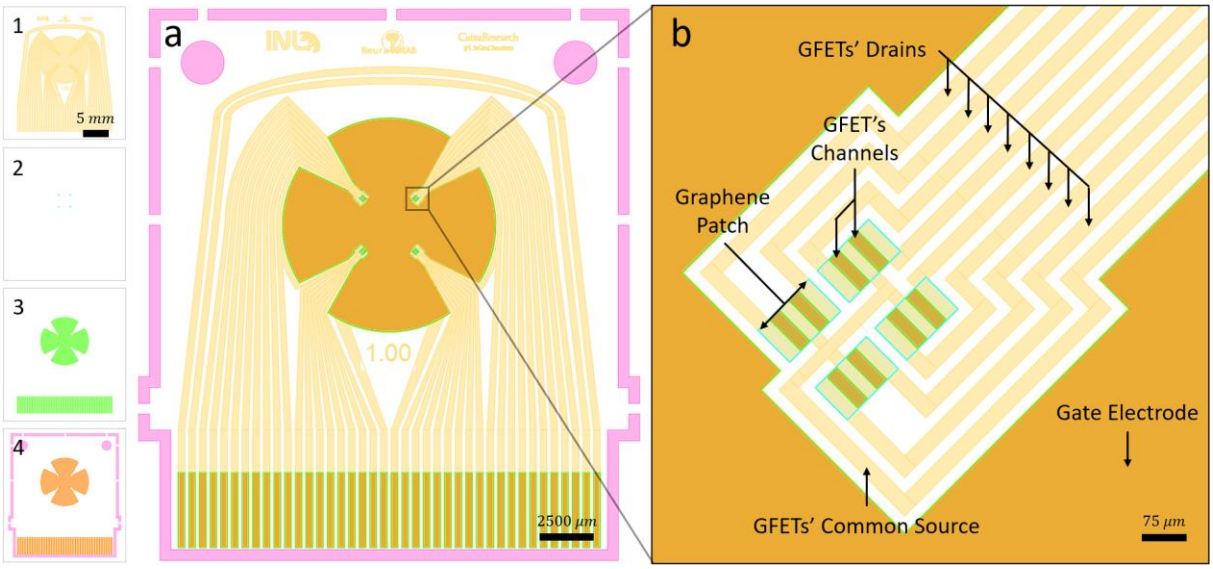


Figure 38 – Layout of the GFET array, following the same color code as Figure 37.
(a) The layout of a single GFET array presenting all of the utilized layers. The insets represent the different layers isolated by fabrication step. (1) Au/Cr tracks patterning. (2) Graphene patterning. (3) Stopping Layer patterning. (4) Passivation Vias opening and Device Cutouts patterning. (b) Detail of one of the 4 groups of 8 transistors. Each graphene patch creates two GFET's channels.

The µLEDs layer possesses the same layers as the GFET array except for the graphene one. The layout is simpler, since each device has two-terminals only, with 8 tracks leading in pairs to the vias where the µLEDs will be mounted. Each of the vias for the mounting of the µLEDs presents a size slightly wider than the LA HB12FP1's footprint, with 250 µm × 400 µm in area, exposing two small parts of the Au tracks which work as electrodes, comprised of an area of 75 µm × 100 µm each. These connections form a tail, ending in a standard 500 µm pitch ZIF connection layout.

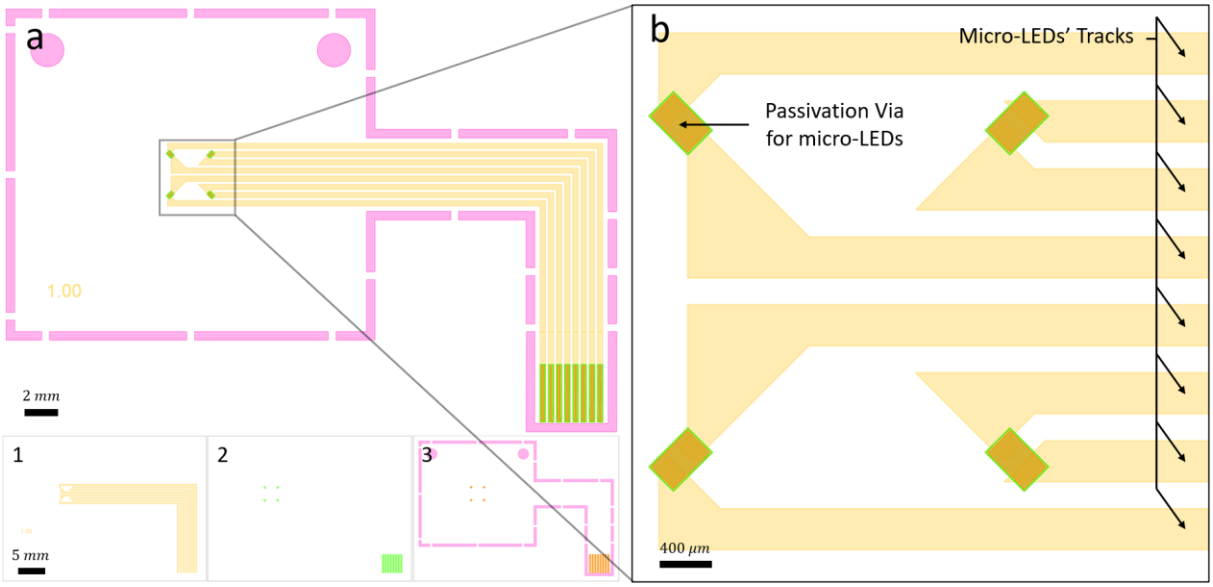


Figure 39 - Layout of the µLEDs Layer, following the same color code as Figure 37.

(a) The layout of a single μLEDs Layer presenting all of the utilized layers. The insets represent the different layers isolated by fabrication step. (1) Au/Cr tracks patterning. (2) Stopping Layer patterning. (4) Passivation Vias opening and Device Cutouts patterning. (b) Detail of the area where the mounting of the μLEDs takes place. There is a total of 4 vias for 4 μLEDs, which when aligned to the GFET array, coincide with the 4 transistor groups.

These two layers layouts were arranged in a single drawing for fabrication on a 200 mm diameter Si wafer (Figure 40a). A total of 12 pairs of layers were arranged, and in the remaining clear areas of the wafer two simple designs with electrodes sized for μLED mounting were placed for testing purposes if needed, highlighted in Figure 40c. Also, alignment marks were placed at the center, left and right margins of the wafer, highlighted in the inset of Figure 40a, and 4 zones for process control were located at 4 different spots (Figure 40b).

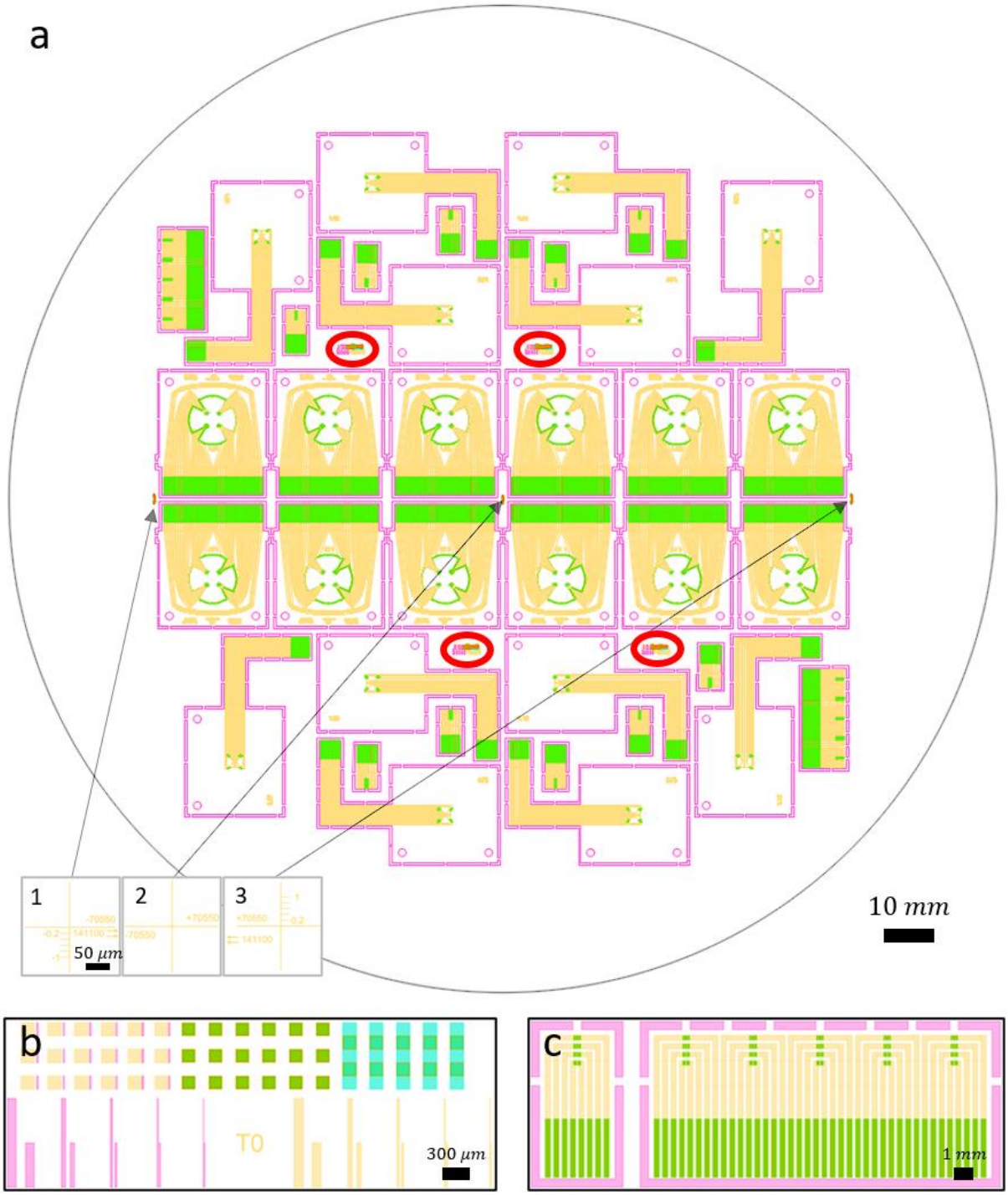


Figure 40 – Device wafer layout. (a) Wafer sized arranged layout.
The grey circle denotes the wafer's limits. In total, 12 GFET arrays and 12 μLEDs Layers were displaced among the wafer. (Inset) Detail of the alignment marks placed on the wafer for alignment during lithography processes. (b) Detail of one of the test zones placed in the red circles marked in (a). (c) Close-up of the small devices for μLED mounting testing.

After the full definition of the layout, wafer fabrication started according to the fabrication process defined.

Before starting the fabrication some of the steps were tested in dummy wafers to assess their viability

and validate their usage on the device wafer. These tests aimed to validate the graphene transfer onto PI, its release and the PI's transmittance, and will be addressed in the following sections.

4.1.1 Graphene Transfer onto Polyimide Test

Before this dissertation project, graphene had only been transferred onto SiO_2 substrates in the context of the NeuralGRAB project. Thus, a first test to assess the wet transfer of graphene onto PI was performed (Figure 41).

An Si wafer was spin-coated with 15 μm of PI (see section 3.2.2), without any layer for release. Prior to the graphene transfer, PI treatment in HCl was performed on a portion of the wafer (Figure 41b). According to [146], the immersion of PI films in 10% HCl solution for 5 minutes would increase the adhesion of the graphene onto this substrate by slightly modifying the surface chemistry, improving the overall transfer quality. The graphene was then transferred via wet transfer process in such a way that roughly half of the graphene patch was placed on the untreated area while the other half was placed on the treated one. The procedure was performed successfully, in a similar fashion to the process described in Figure 5 and section 3.4.2.

After this process, two-point resistance measurements were taken (Figure 41b.3) both on the treated and untreated side, showing no evident differences between the graphene transfer quality, and thus, the HCl treatment was discarded. Moreover, the wet transfer process onto PI occurred similarly to the transfer of graphene onto SiO_2 substrates, showing that the transfer could be done directly onto the spin-coated PI surface, as reported in the literature [11], [91], [94] (summarized in Table 1 of section 2.1.6).

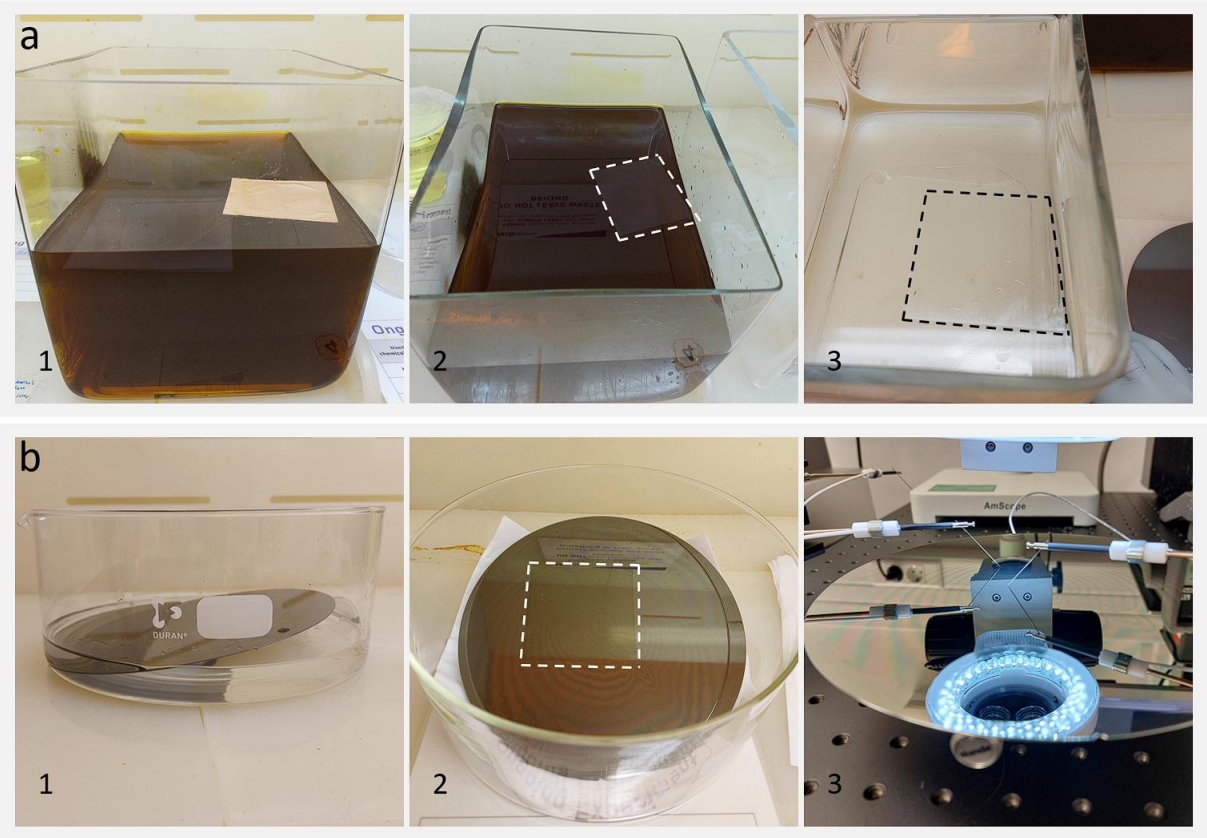


Figure 41 – Process of graphene transfer and chemical treatment on PI.
Graphene patches are highlighted by dashed lines. (a) Transfer process of the utilized graphene. (1) PMMA-coated graphene on Cu foil right after being left floating on $FeCl_3$. (2) PMMA-coated graphene floating $FeCl_3$ after Cu etch. (3) PMMA-coated graphene floating on DI water prior to transfer onto PI wafer. (b) Steps of the test on the PI wafer. (1) Setup for immersion of the PI wafer in HCl 10% for 5 minutes. (2) PI wafer after fishing of the PMMA-coated graphene in (a)(3) visible as a dark patch. (3) Two-point measurement setup on the graphene patch after removal of the PMMA.

4.1.2 Polyimide Release from Wafer Test

To test the release process of the PI from the Si wafer by utilizing a SiO_2 sacrificial layer, another dedicated wafer was prepared. A sacrificial layer of 500 nm of SiO_2 was deposited by PECVD (see section 3.2.1) on a Si wafer, followed by spin-coating of 4 µm thick PI (Figure 42a,b, and section 3.2.2). A portion of the wafer was cleaved and a dry etch of the SiO_2 took place (Figure 42c, and section 3.2.6). The PI film was partially released, and wrinkles formed on its surface. By peeling the thin film with a tweezer, the PI thin film was fully released, indicating a successful process suitable for usage in the wafer fabrication. One should point out that the efficacy of this process is attributable to the fact that PI films show significant permeability to the utilized gas etchant, accelerating the etch process. If this was not the case, the etching of the oxide could only take place laterally, hindering or slowing the process.

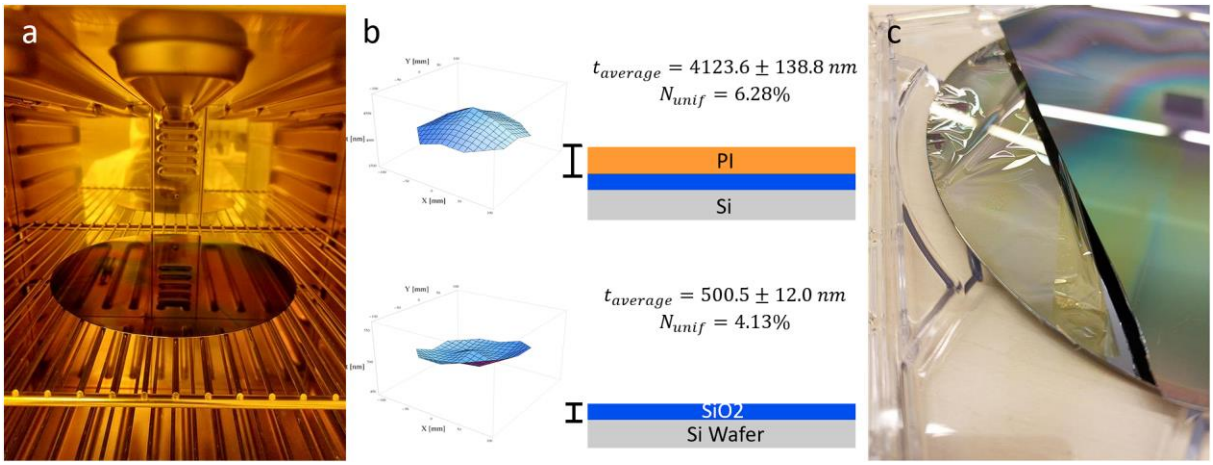


Figure 42 – PI wafer before and after the release process.
(a) Wafer after the spin-coating of PI inside the furnace for curing. (b) Obtained thickness measurements by optical profilometry of the SiO_2 sacrificial layer and respective schematic (bottom) and of the PI spin-coated layer (top) (c) Cleaved and released portion of the wafer next to the remaining unreleased one. The PI film got released and wrinkled as it was no longer attached to the SiO_2 substrate which got etched.

As the release of the device is one of the last steps, the whole device will be exposed to this process. This raised questions as to what effects the exposure to the dry etch process will bring. To explore this, small patches of graphene were dry transferred onto 6×6 mm^2 $Si/SiO_2/PI$ stack chips, followed by execution of the dry etch process of the oxide sacrificial layer (Figure 43). To test the effects of the process, two-point resistance measurements were taken before and after the dry etch. The results can be observed in Table 3. Two out of the six samples were non conducting before the exposure to the process, attributed to an unsuccessful transfer process. Interestingly, the resistance measurements of the remaining samples show that the graphene on average halved its resistance after the dry etching process. It is known that HF exposure can help in cleaning inorganic oxide residues [61], as is the case of Cu oxides, which can explain this decrease in resistance. Furthermore, fluorination of graphene during this process is unlikely, as although exposing it to an aqueous solution of HF can successfully achieve its fluorination [147], [148], exposure to HF gas for up to 17 hours has been shown not to alter its properties [148].

Table 3 - Two-point resistance measurements before and after exposure to dry etch process.

Sample Number	**Resistance Prior to Exposure ($k\Omega$)**	**Resistance After Exposure ($k\Omega$)**
1	73	29
2	-	-
3	44	21
4	-	-
5	39	26

6	42	21

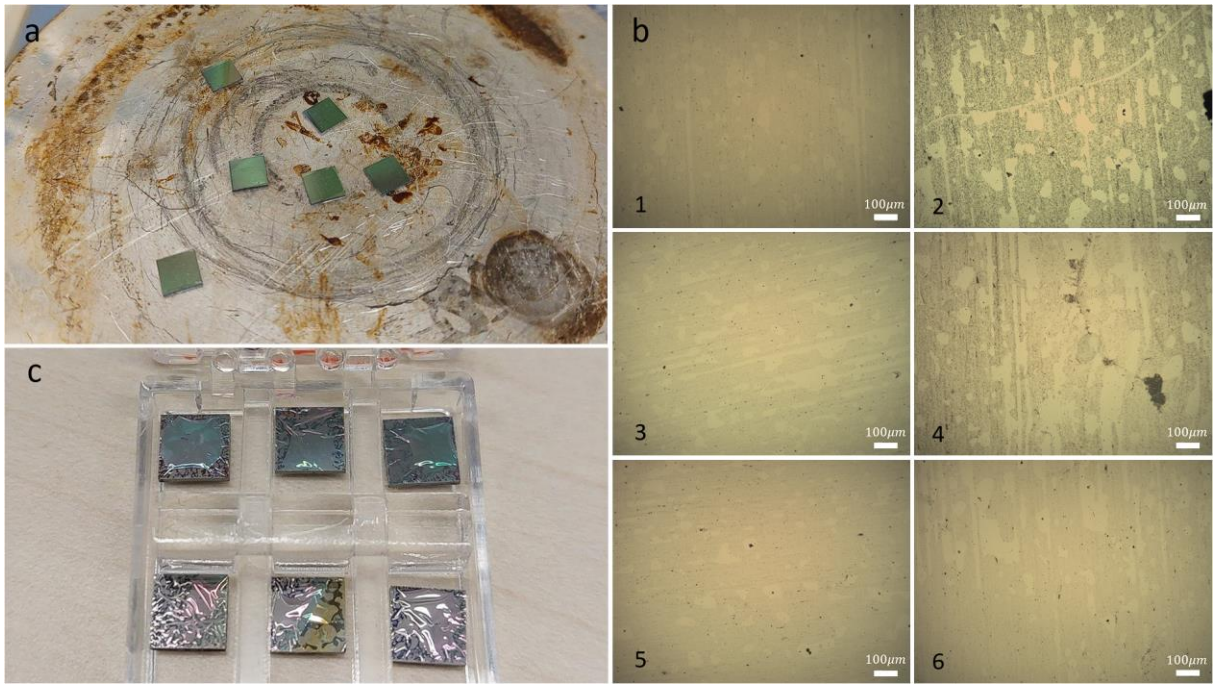


Figure 43 – PI Wafer chips with transferred graphene before and after exposure to the dry etch process. (a) Six small graphene patches were transferred on a Si/SiO2/PI chip with a PVA support polymer. (b) OM images of the transferred graphene after removal of the PVA and before the etch process. The scale accounts for the 100 μm (c) Appearance of the chips after exposure to the dry etching treatment. The wrinkling shows that the sacrificial SiO_2 layer got etched and the PI partially released. The wrinkled surface complicated the acquisition of OM images.

4.1.3 Polyimide Transmittance Measurement

The device layout and structure place the μLEDs below a PI film of 3.5 μm. Although PI is deemed transparent, it shows an orange tint, meaning its transparency decreases for smaller wavelengths of visible light. This can pose a problem as the utilized LA HB12FP1 μLEDs emit light with a central wavelength of 450 nm. To address this, UV-Vis measurements were performed on the released 3.5 μm thick PI films. For comparison, PI Kapton HN (DuPont) films of 25 μm and 75 μm thick also had their transmittance measured. Furthermore, as graphene will be present on top of the PI film in the end device, one more 75 μm thick sample was covered with graphene. The results can be observed in the plot of Figure 44. The thin film released from the wafer presented the highest transmittance out of all the samples at the 450 nm wavelength, with around 75%. The remaining samples are unsuitable for usage in the top layer of the device as they present near-zero transmittance of 450 nm wavelength light, rendering the μLEDs useless. Although the thin PI film of PI2611 only presents 75% of transmitted light,

it is acceptable for usage in the device because the optical output of the device can be increased to account for this reduction in transmission across the PI film.

It is also noteworthy that although the thickest PI film of 75 µm coated with graphene presented lower transmittance than the uncoated one, the difference is minimal (below 3%). This means that graphene, as expected, has little effect on the layer's transparency.

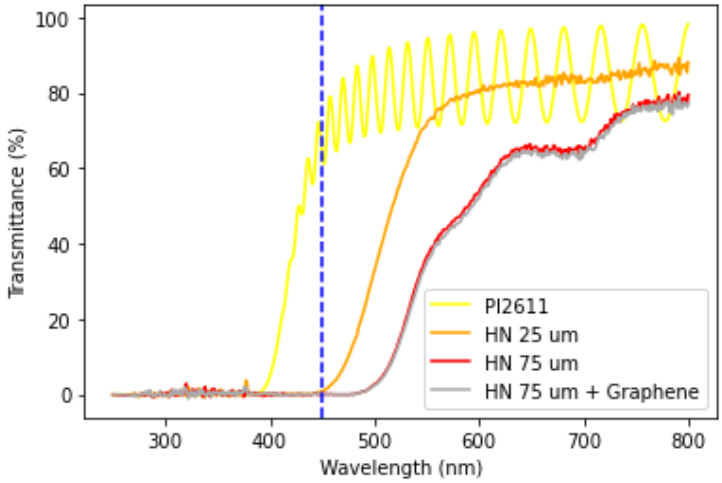


Figure 44 – Plot of the transmittance measurements acquired on the UV-Vis for the four samples. The dashed vertical line indicates the central wavelength of 450 nm at which the utilized LA HB12FP1 µLEDs emit light.

4.1.4 Polyimide Passivation and Via Opening on Au Tracks Test

The PI passivation and vias procedure was tested on a custom wafer for µLED mounting testing, and the entire fabrication process can be found in appendix II. In this wafer, the layer utilized for passivation of the Au tracks was PI, and vias were open on top of these tracks in the required areas. The summarized process for PI passivation and via opening on Au tracks is depicted in Figure 45a. With already patterned Au tracks with Cr as an adhesion layer on top of a PI substrate, the wafer was spin-coated with another 3.5 µm of PI, effectively passivating the whole wafer. For AlSiCu patterning by lift-off, spin-coating of photoresist was the next step, followed by exposure and development to create the intended pattern (see section 3.2.3). Deposition of 100 nm of AlSiCu (see section 3.2.4) on top of the wafer was then performed. Finally, the lift-off process was done by immersing the wafer in acetone with the simultaneous application of ultrasounds. From here, the wafer was now ready to open the vias. By utilizing RIE and a $CF_4 + O_2$ atmosphere, the PI was etched at a fast rate of around 500 µm/min. In comparison, the AlSiCu was barely attacked at an etch rate lower than 5 nm/min, effectively opening vias only where the PI was exposed. Once the Au tracks were reached, the etch rate of those areas again decreased, signaling that the etching could be stopped, although a slight over-etch was done. Care was needed in this step as the

Au layer thickness was only 40 nm and it is stated in the literature that the etch rate of Au under these conditions is around 8 nm/min [149]. After this process, the AlSiCu was removed by wet etching utilizing an Al etchant.

After the process the vias were successfully opened. In Figure 45b-d it is noticeable the evolution of the etching of the PI. Before reaching any Au track, the etch rate was similar everywhere except at the AlSiCu covered area. When reaching the Au track, the etch rate abruptly decreased. The small over etch was done for two reasons: to remove PI residues that could be present on the Au track areas, and the etch rate was not homogeneous throughout the whole wafer area, as typically it is weaker near the wafer edges, thus requiring more etch time. By comparing images before and after opening the vias in Figure 45e,f the difference in coloration of the visible tracks was noticeable due to the partial etching of the surface of the Au tracks. By utilizing a higher magnification and after removing the AlSiCu sacrificial layer, the roughness of the surface and PI residues became evident, meaning the over-etch was not enough to mitigate this issue. This emphasizes the need for a stopping layer. By utilizing a stopping layer, the whole Au thickness would be preserved, and the PI residues would be removed at the same time as the stopping layer removal.

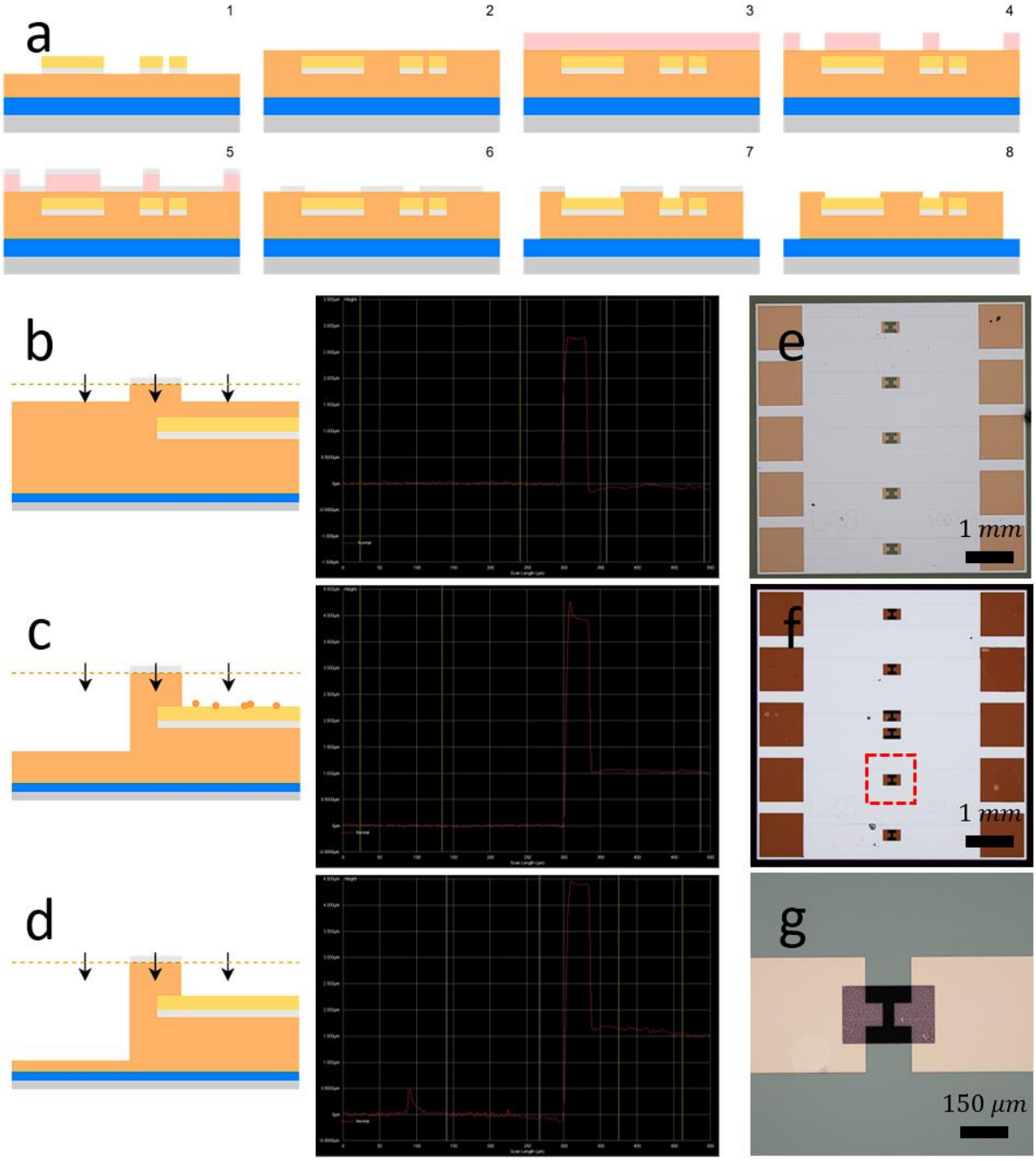


Figure 45 – Designed process and results from PI passivation and vias opening.
(a) Schematic of the process for the PI passivation and via opening starting with an already patterned Au/Cr layer on PI (a), followed by spin-coating of PI passivation layer (2), the lithographic process of photoresist spin-coating (3), exposure and development (4), sputtering of AlSiCu (5) and lift-off (6), to allow for the RIE of the PI to open the vias (7) and ending with the etching of the AlSiCu (8). (b),(c),(d) Schematic and respective plot of the measured topography of the wafer during the RIE process for PI vias opening after a total of 5 min (b), 7.5 min (c) and 9 min (d) of etch. (e) OM image of an area of the wafer before the RIE to etch the PI passivation. (f) OM image of a similar area to (e) after the RIE. (g) Detail of the area delimited by the dashed contour in (f) after removing the AlSiCu sacrificial layer, showing the residues of PI left on top of the exposed Au tracks.

4.2 Device Wafer Fabrication

The sketched fabrication process in Figure 36 was partially validated by the tests in sections 4.1.2, 4.1.3, and 4.1.4. The following sections addresses the device wafer fabrication. Each of the designated steps of fabrication are discussed in an in-depth manner, providing the context of each wafer fabrication step and the obtained result.

4.2.1 SiO_2 Release Layer Deposition

The deposition of the SiO_2 layer was done in a PECVD system (section 3.2.1). A total of 500 nm was deposited on top of a new Si wafer. This layer is indispensable for release of the final flexible device; without it, the device would remain permanently attached to the fabrication substrate and not be flexible. After the oxide deposition, interferometer measurements were executed to evaluate the thickness and uniformity of the wafer (Figure 46). It presented good uniformity with a value of 3.36%.

$$t_{average} = 495.4 \pm 9.9\ nm$$
$$N_{unif} = 3.36\%$$

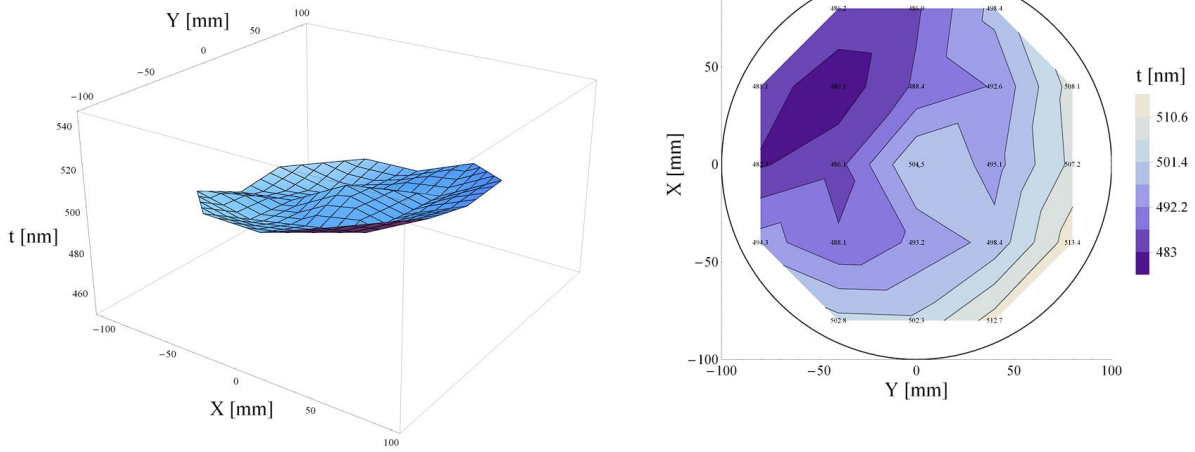


Figure 46 – Map of the thickness of the deposited SiO_2 deposited layer.
An average thickness of 495.4 nm is achieved, with a uniformity of 3.36%, an acceptable value.

4.2.2 Spin Coating of Polyimide Substrate

Spin-coating of the PI (see section 3.2.2) took place after the SiO_2 deposition. A film of about 3.5 µm in thickness was achieved (Figure 47) with good uniformity (4.42%). Some defects, such as bubbles or comet-like structures, were visible on top of the wafer. The bubbles occur during the spin-coating and curing stages due to a deficient application of the PI precursor (see section 3.2.2). The comet-like structures form due to the presence of particles on top of the wafer before the application of the PI

precursor. These defects, mainly bubbles, can render smaller features on the device useless as they make the surface locally defective with unpredictable topography. Nevertheless, the spin-coated PI layer presented good uniformity, and the number of defects was not significant enough to justify the repetition of this step.

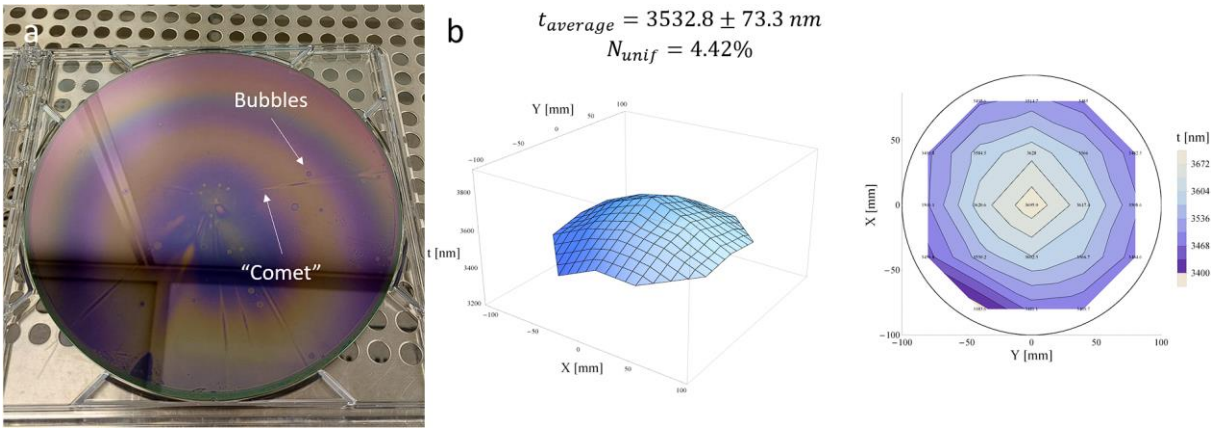


Figure 47 – First PI spin-coating on the device wafer wafer.
(a) Image of the device wafer after the spin-coating of PI. Defects are visible on its surface. (b) Interferometer measurements of the spin-coated PI substrate layer of the device wafer.

4.2.3 Patterning of Conductive Tracks

The conductive tracks were made of Au to resemble the rigid devices. In its case, for improved adhesion of the Au onto the SiO_2 substrate, a skinny Cr layer is used, which is also well suited for usage in the case of the device wafer, as it presents an excellent adhesion improvement on PI substrates [150] in comparison with bare Au. Also, in the case of the rigid device, the patterning of the tracks was done by ion-milling, which, by tunning the angle at which the wafer is about the beam, could achieve a smooth edge that would prevent graphene cracking after the transfer at the drain/source and channel connection [51]. Ion-milling is based on bombarding the surface of the wafer with ions, slowly etching it. This process is unsuitable for the device wafer as it could damage the PI surface and complicate the graphene transfer process, benefiting from a smooth, flat substrate surface. To circumvent this problem, a different patterning technique was adopted. In the literature, GFET devices with graphene on top of drain and source contacts also utilize lift-off as their patterning technique with successful results [11]. In the case of the device wafer, this process was also adopted (see section 3.2.4).

The process for patterning the wafer is depicted in Figure 48a. The photoresist was first spun with a thickness of 1035 nm and then soaked in tetramethylammonium hydroxide (TMAH) to harden its surface. The photoresist is then exposed (see section 3.2.3) to the pattern in Figure 38a.1 and developed to reveal the exposed pattern (Figure 48c). In principle, the soaking process hardens the photoresist surface, which

is slightly less attacked by the developer than the deeper part of the photoresist. A structure with an inverted slope is created, as depicted in Figure 48b. This shape prevents metal from being deposited on the sidewalls of the photoresist thus promoting well-defined edges. The sputtering of the Au/Cr tracks followed. First, 10 nm of Cr was deposited, followed by 100 nm of Au, covering the whole wafer (Figure 48d). Finally, the removal of the photoresist in acetone and ultrasounds took place, lifting off the excess deposited metal and revealing the intended pattern (Figure 48e).

Mechanical profilometer measurements hinted that the metal possessed rough edges, meaning the soaking in TMAH in the lift-off process was unsuccessful. The spikes seen at the edges might have also been an artifact from the measurement, and to confirm this, measurements were made in opposite directions in the exact location. From observation of the plots in Figure 48f, it is possible to conclude that although artifacts were present, there was also a spike at the edges of the metal tracks. This could complicate the step of graphene transfer, which was the next step in the fabrication process, addressed in the next section.

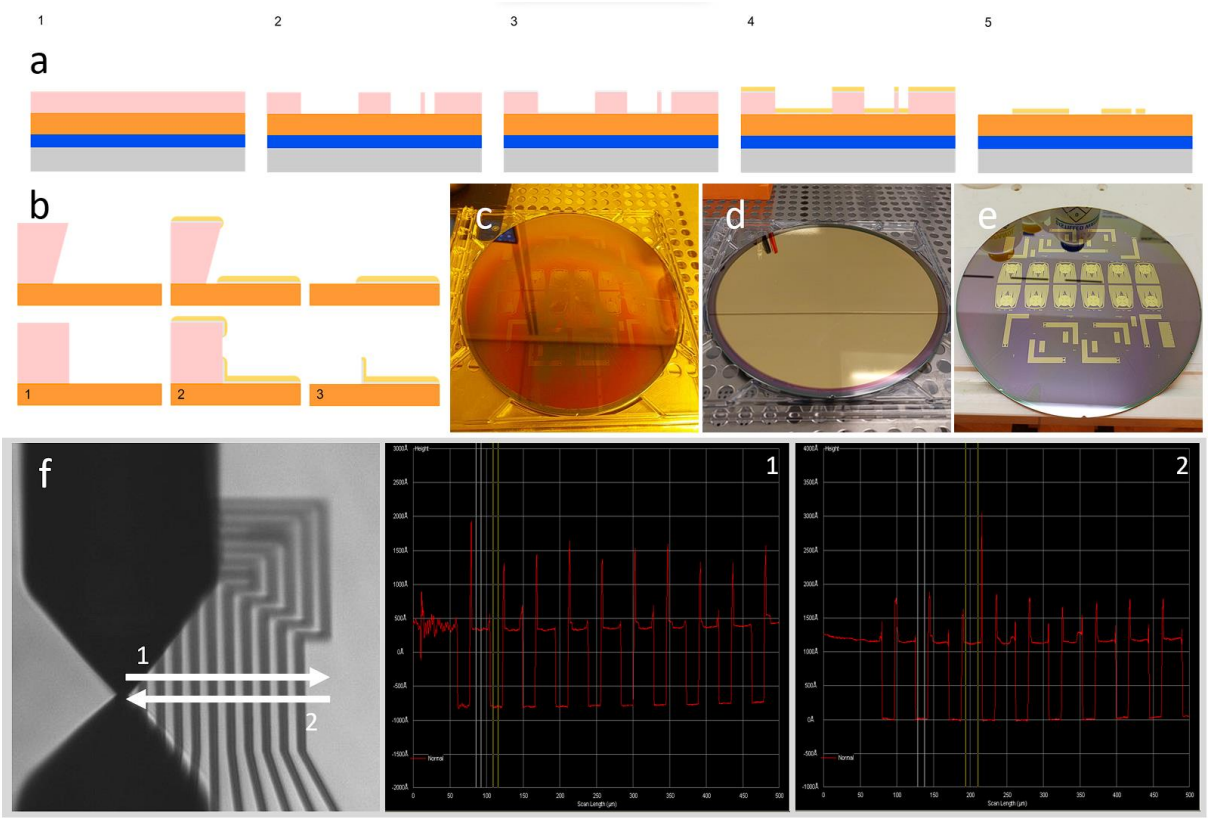


Figure 48 – Process of patterning of Au tracks on the PI substrate.
(a) Schematic of the patterning process of the Au tracks with Cr adhesion layer by lift-off. First, there is the spin-coating of the photoresist (1), followed by its exposure and development (2), and the subsequent sputtering of Cr (3) and then Au (4), ending with the removal of the photoresist in acetone to lift-off the excess metal (5). (b) Comparison of the effect of the soaking with TMAH (upper) versus no soaking (bottom) before the exposure and development of photoresist. (1) The soaking results in an inclined wall of the photoresist (2) that prevents the formation of vertical edges that survive the lift-off process (3). (c),(d),(e) Device wafer at the steps (a)(2), (a)(4)

and (a)(5), respectively. (f) Captured image of the contact profilometer measurement and an indication of the taken paths forward (1) and backward (2). Tall spikes are noticeable at the metal edges corresponding to the top portions of the graphs.

4.2.4 Graphene Wet Transfer

The next step was graphene wet transfer onto the patterned tracks. A standard wet transfer (see section 3.4.2) of OxGr resumed onto the patterned tracks. After the removal of the PMMA support polymer in acetone, the transfer was complete. The graphene patch covered 3 devices, as visible in Figure 49a, before the PMMA removal. Microscope images show that the transfer produced a lot of residues, and the graphene got torn in multiple places. In Figure 49b,c,d the extent of the residues is visible from a smaller to a larger scale. Dark brown residues indicate leftovers of $FeCl_3$ used in the etching of the graphene native substrate and indicate poor cleaning of the graphene during the transfer process.

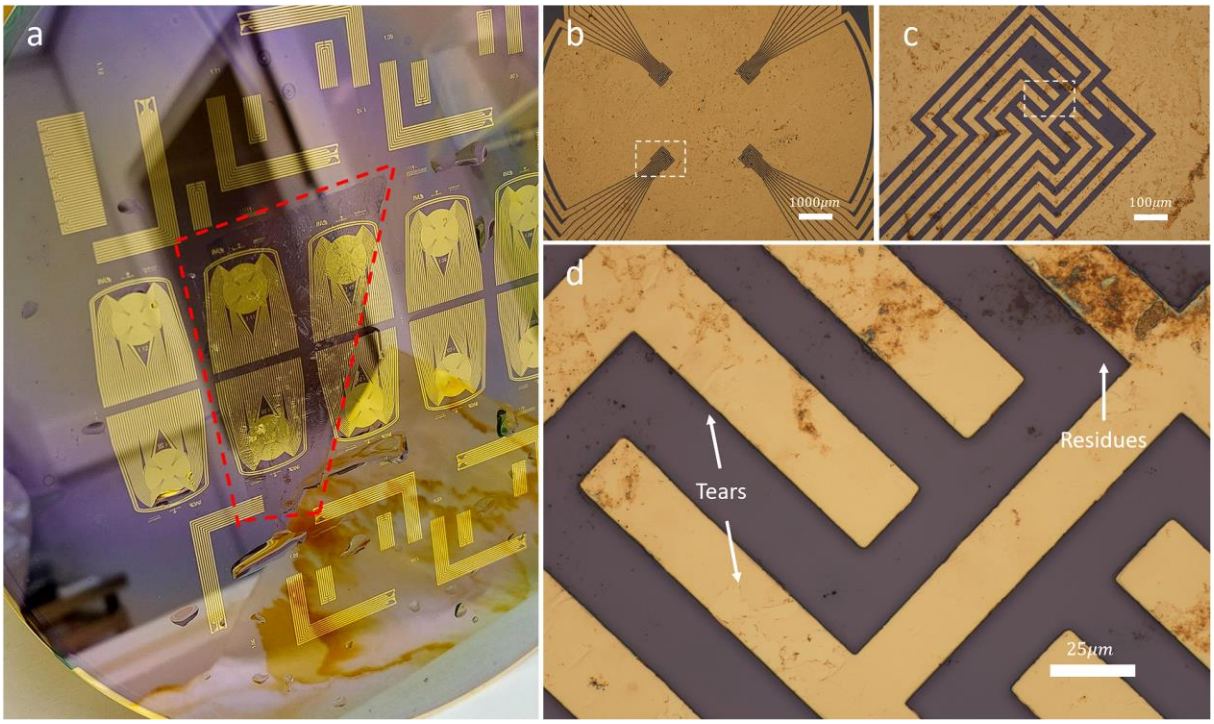


Figure 49 – Graphene transfer onto the device wafer.
(a) Graphene patch transferred onto the device wafer before removing the support PMMA marked by a dashed line contour. (b) OM image of one of the devices after the PMMA removal. A lot of residues are visible at this scale. (c) OM image of the area marked by a dashed contour in (b). The area presents itself as densely packed with residues. (c) OM image of the area marked by a dashed contour in (c). Graphene cracks and tears are visible. Residues are also spread across the GFETs' to-be channel area.

Furthermore, the visible cracks in Figure 49d are spread randomly and could affect the correct functioning of the to-be-fabricated GFETs if these defects are present in their channels. To address this possibility,

SEM images of the devices were acquired (Figure 50). The Au tracks resemble the lighter areas, while the PI substrate is dark. Differences in the Au track's tonality are due to either the presence or absence of graphene, presenting darker or lighter colors. Round smudges with a 3D appearance amidst the PI substrate are artifacts due to the charging of the scanned area. This happens when the scanned area has poor conductivity, and given this fact, one can understand whether the graphene is covering the PI substrate. Dark areas with a "flat" appearance are graphene-covered and are thus conductive, while the "3D smudged" areas are absent of graphene and thus present charging artifacts. This phenomenon can be used to interpret these images and evaluate the coverage and integrity of the graphene on the PI substrate that will be used as channels of the GFETs. In the case of Figure 50a, the channel areas presented acceptable graphene coverage at this scale. It is worth noting that the SEM presents as a powerful tool to assess the quality of the transferred graphene onto this substrate, as it is challenging to distinguish graphene-covered areas from non-covered ones by simple OM images, as noticeable in Figure 50b by looking at the PI areas. By increasing the magnification of the SEM, it is possible to observe that the suspected edges created on the Au tracks from the lift-off process are indeed present. Figure 50 (c) and (d) show that these edges are fracturing graphene, compromising the continuity between the Au tracks and the graphene channel. It is also possible to observe that the graphene sometimes got suspended and under tension, leaving it in a very fragile state, where even surface tension of liquids could fracture it. This made it unsuitable to resume fabrication under these conditions, and intermediate steps would be necessary before transferring more graphene onto the wafer. Unfortunately, it was impossible to do so during the time course of this dissertation work, and the fabrication halted in this step.

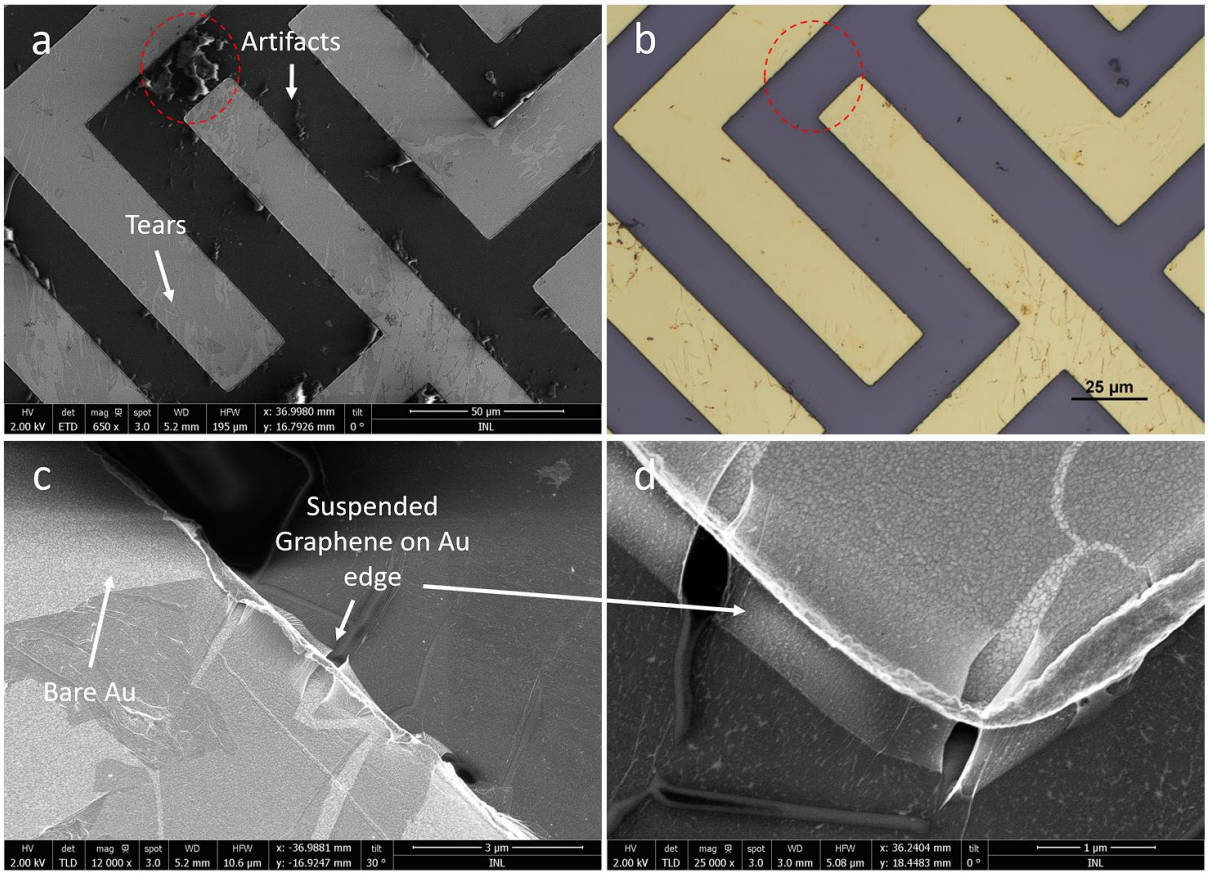


Figure 50 – Assessment of the graphene transfer onto the device wafer.
(a) SEM image of a transistor area where tears and cracks on the graphene are noticeable compared to (b) OM images of the same area. The dashed circle denotes an area where no cracks or tears are visible in the OM but are evident under the SEM. (c),(d) SEM images of different Au edge regions where transferred graphene got suspended and torn by the edges created in the lift-off patterning of the tracks.

4.3 Concluding Remarks on Device Development

Although the fabrication of the device wafer was not completed, the results confirmed different aspects of the designed fabrication process and highlighted critical key points that must be considered.

The choice of materials proved effective, as the Au tracks presented good adhesion to the polyimide substrate by using the Cr interlayer. Nevertheless, the deposition and patterning methods utilized would require further tuning. The spin-coating of the PI should be modified to reduce the number of defects that can compromise whole devices, and the patterning of the Au tracks should be made by other methods, for example, wet etching, to avoid the formation of edge spikes that can later tear graphene. The state of the Au tracks conditions the fabrication process, and an etch of the spiked edges would be necessary.

The transfer of graphene achieved was too dirty for the standards of the approach utilized, with an unusual number of residues being transferred onto the substrate. This entails that special care should be taken when preparing the etching solutions of the Cu foil during the wet transfer. Furthermore, the utilized

polymer, PMMA, can also compromise the transfer with large amounts of residues, as shown in appendix VI, which highlights another critical point for the successfulness of the process.

Regarding the fabrication steps that were not accomplished, none of them appear to be limiting. Graphene patterning is relatively straightforward by utilizing a photolithography process for patterning a photoresist and later etching of the exposed areas by O_2 plasma. This would, in principle, damage the surface of the PI in the exposed regions, which is not critical as the GFET channels with graphene would be protected and the integrity of the underlying PI substrates maintained. Furthermore, the following deposition of the stopping layer has already been tried [51] by sputtering of either Cu or Ni, albeit in rigid substrates. At this step, one can recognize that the increased porosity of PI and the sputtering technique for deposition of the stopping layers could induce damage to the graphene. Still, testing would be essential to assess this possibility. If not successful, different stopping layers would need to be tested or different deposition methods employed (for example, evaporation, although not available at the INL facility). The remaining passivation with PI and opening of the vias should, in principle, occur smoothly as there would be no substantial differences from the test done in the custom wafer for μLED mounting (appendix II), except for the existence of the stopping layer, which would improve the overall quality of the process. A possible complication would entail the chemical modification of the stopping layer due to the usage of the CF_4+O_2 chemistry in the plasma and complicate the layer removal in the etchant, and testing would be necessary to address this possibility. Finally, the release of the devices would follow the mentioned tests, which should be adequate and achieve the full release of the fabricated devices.

Overall, the work in this section contributed to implementing the GFETs on the PI and showed significant signs that the fabrication process could occur, albeit further tuning and testing are necessary. It was highlighted that patterning procedures of the gold tracks are important to achieve a successful wet transfer. Furthermore, a technique for via opening on polyimide passivation layers was established, and the resistance of graphene to the release process of the devices confirmed. These results thus facilitate the integration of the graphene-based neurochemical sensor on flexible and transparent polyimide.

5. μLED MOUNTING

Brain activity modulation with optogenetics requires light to be delivered to the desired tissue. The NI designed in this work aimed to accomplish this by integrating optical stimulators in the flexible device. By utilizing flip-chip μLEDs (LA HB12FP1 and LA UB06FP2), fabrication process was simplified, as a fabrication process for the μLEDs did not need to be developed. Nevertheless, mounting these μLEDs on the flexible substrate is challenging. The small size of the components complicates handling and the reduced footprint of the target electrodes on the wafer makes alignment procedures difficult. Furthermore, attaching the μLEDs while maintaining reliable electrical contacts required optimization, and thus different approaches were explored. The tried approaches can be divided into two groups, being the soldering approach and the stamping/pick-and-place approach, with the latter providing the best results. To further test the stamping/pick-and-place, the same procedure was applied to the smaller footprint μLEDs (LA UB06FP2), which enables smaller devices to be fabricated in the future. After establishing the best mounting technique, different tests were conducted to assess how the μLEDs could handle the fabrication process of the wafer and decide at which point of the fabrication these could be mounted, and to measure their electrical behavior and output optical power.

5.1 Soldering Approach

The first approach to be tried was to solder the μLEDs to the patterned Au tracks on PI on the wafer. In the μLEDs datasheet, the advised approach for mounting the μLEDs on the desired circuit was to solder them as their electrodes were prepared for that process. Thus, solder paste was first utilized. The approach consisted in placing some of these small solder balls with flux of the solder paste on top of the μLED's contact pads, apply heat (250° C) until these melted and conformed to them, and finally place the μLED on top of the target Au tracks and reapply the heat. A dummy silicon wafer (appendix III) with exposed Au tracks on top of SiO2, was used for these first tests. The wafer had exposed Au tracks with 30 nm in thickness that resembled the ones of the device wafer (Figure 40).

The procedure is depicted in Figure 51. The placement and flipping of the μLED for the contact pads to face up was done manually with tweezers. Then, the solder balls were also manually dispensed, followed by heat application (250° C) to induce the melting and adhesion of the solder. In Figure 51b, it is possible to observe the spreading of the solder on top of the Au track when applying heat, which is expected to

occur when utilizing solder, signaling that its melting point was successfully reached. This process did not lead to the mounting of the μLED, as it was still loose after cooling down, and detached from the substate. By post inspection of the mounting site (Figure 51c), it is visible that the Au tracks were extensively damaged, with material being completely removed.

The same approach was employed with a different solder with lower Sn composition and utilizing Bi and Ag in the place of Pb. This solder was not available in solder paste form, and thus it was scrapped onto small flakes, deposited on top of Au tracks and wetted with flux. The result was similar to the one previously mentioned, culminating in the removal of the Au tracks. Fragile and loosely attached solder material was also left on top of the substrate, once again showing that the soldering was not viable.

This behavior can be attributed to the high solubility of Au on Sn, a main compound of both of the used solders. Effectively, Sn is known to scavenge Au [151] and this can be the reason why the tracks were dissolved onto the solder. The reduced thickness of the Au tracks, with only 30 nm, compared to the amount of solder can also have played a role in the failure of this approach. As the amount of track material is greatly smaller than the amount of solder, the scavenging and dissolution of the Au tracks can be greatly enhanced.

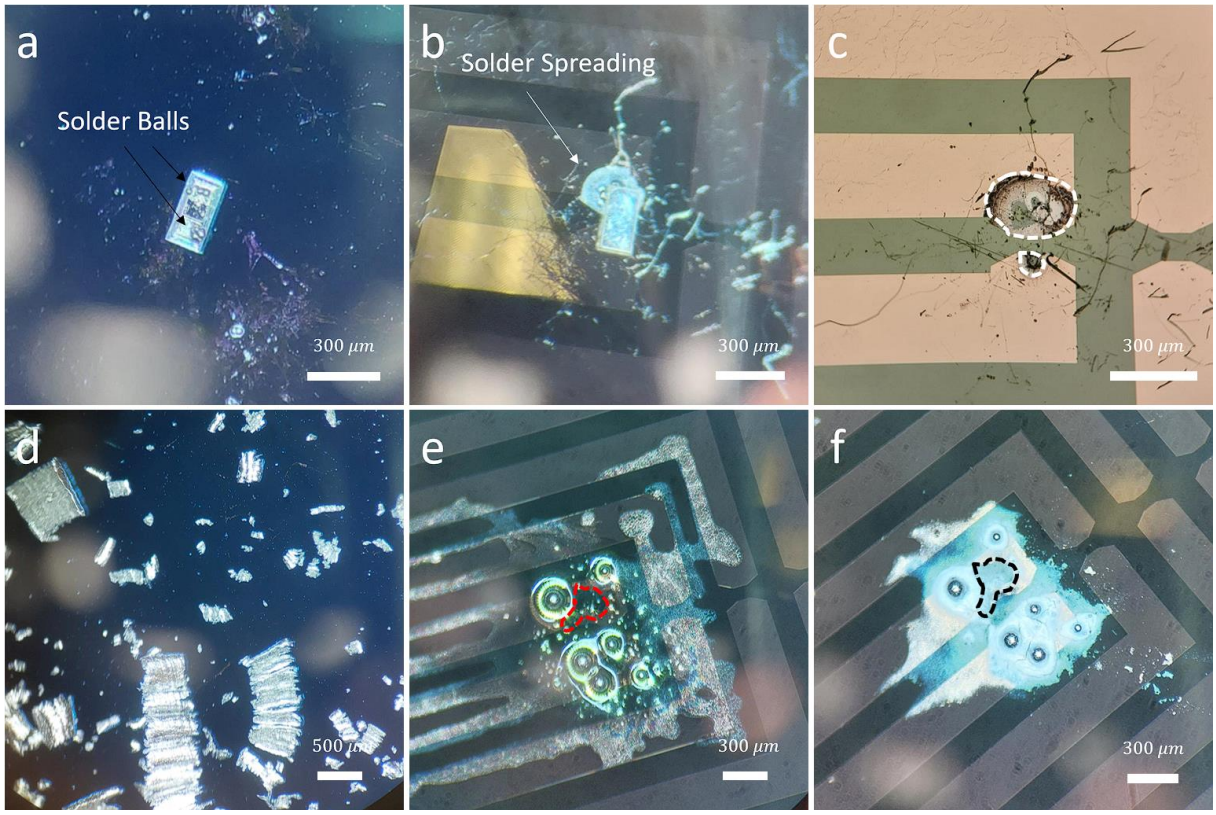


Figure 51 – Process of applying solder to μLED and wafers.
(a) Solder balls applied on the μLED's electrodes. These are visible as small spheres pointed by the arrows. (b) μLED placed on top of mounting site on test wafer. The solder spread along the tracks after being heated to curing temperature. (c) Aftermath of the soldering process with the solder balls. The Au tracks were damaged

and removed in the locations marked by the dashed shapes. (d) Image of the scraps of the lower melting point solder. (e) Image taken during the process of heating the solder scraps and flux on mounting site. The scraps are seen to melt and agglomerate forming tiny spheres. (f) Aftermath of the heating process, with visible white stains due to flux. The dashed area marks a spot where the Au tracks were damaged and removed. It is also possible to see that the solder did not spread along the tracks.

To try and circumvent the extensive damage to the tracks by the soldering approach, a Ni layer was electroplated on top of the pre-existent Au tracks. Electroplating consists of creating a metal layer on top of a conductive material immersed in an electrolyte composed of a salt of this same metal. For this to happen, a voltage is applied between the immersed target conductive material, which will act as a cathode, and a second immersed electrode, usually made of the material to be deposited or an inert metal, that will act as anode. Reduction of metal ions dissolved in the solution will occur at the cathode, forming a metal layer.

The electroplating was employed as it required no additional lithography processes, and a thicker layer of material could be achieved with relative ease on top of the pre-existing tracks to reduce the removal of track material after application and curing of solder paste.

After the electroplating of the Ni on top of a test region of the Au tracks, profilometer measurements were performed to address deposited thickness (Figure 52a,b). The measured thickness of the Ni layer ranged between 150 nm and 200 nm, which is approximately a 6-fold increase on the overall track thickness. Scraps of the lower Sn composition solder were placed on top of the Ni layers and heat was applied. The results are shown in Figure 52d. Although the wetting of the solder on top of the tracks was improved, portions of the Au track were still damaged and removed. This indicated that the Ni thickness was not enough to withstand the soldering process.

From the obtained results, we concluded that for the soldering approach to be viable, a thicker layer of conductive material would have to be deposited, or another solder paste, without Sn or flux should be tested. As achieving thicker layers would require many optimization steps and there were no other solders available, the soldering approach was abandoned.

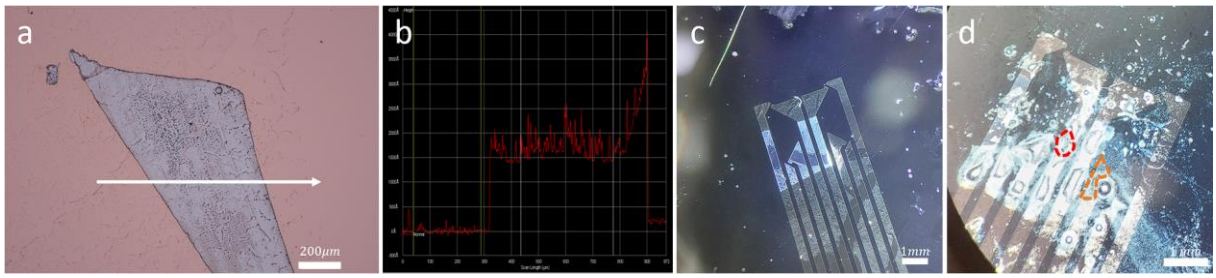


Figure 52 – Soldering on top of electroplated Ni layer.
(a) Test zone of the Ni electroplating on a region covered in Au. The white arrow indicates the direction of the profile's measurement in (b). (b) Contact profilometer measurements from the region in (a). An average thickness of approximately 175 nm was electroplated. (c) Mounting site region electroplated with Ni with the

same parameters as in (a). The electroplated region shows a lighter color while the bare Au tracks present a gold tonality. (d) Aftermath of applying solder scraps and heat to the region in (c). Although the solder appears to have spread more successfully not forming isolated solder spheres, the Au tracks were damaged and removed in the area denoted by the red dashed line. The orange dashed line denotes a second region where Ni electroplating did not take place and the Au tracks also got removed due to spreading of the solder.

5.2 Stamping and Pick-and-Place

In the previous section it was shown that the reduced thickness and material of the conductive tracks is a limiting factor when it comes to soldering the μLEDs. As such, incorporating methodologies that avoid the modification of the underlying material could in principle achieve better attachment of the μLEDs. One suitable option was the usage of conductive resins. Conductive resins are epoxy based substances with a filler material that provides conductivity. The conductive resin (Ablestik 8037 TI) used to test this approach was a silver nanoparticle filled heat cured epoxy resin that could be used to electrically connect and mechanically attach the μLEDs on the Au tracks. To achieve this, a stamping process followed by picking and placing of the μLEDs was performed on a system, described in section 3.3.2, followed by heat curing.

The stamping process was based on utilizing an adequately sized tip that was dipped on conductive resin to stamp it on the μLEDs mounting site. The small-sized tip presented dimensions smaller than the pads to grant enough precision when stamping. The following pick-and-place process was achieved by using a custom sized vacuum tip for the LA HB12FP1 μLEDs. Its dimensions considered the size of the LA HB12FP1 chips, allowing for alignment and maneuverability. The complete process is depicted in Figure 53a, separated into the stamping and pick-and-place parts. The stamping process started by dispensing a drop of conductive resin in an area where the stamping tip could reach. This was followed by dipping the tip on the conductive resin, so it got sufficiently wet. The immersion time of the tip could be tuned to achieve different amounts of resin on the tip. The last step was the stamping of the conductive resin on the desired spot, in this case the conductive Au tracks (Figure 53a.2,c). The applied force (0.02 N) was of major importance, as the underlying PI substrate is soft and can get easily damaged (Figure 53b). Furthermore, care is needed when stamping the substrate as to not induce short circuits – an excess of conductive resin could flow outwards to undesired areas. The alignment of the component and the tip was also of great importance, as a poor alignment could complicate the placement on the mounting site. The μLED was then picked up by moving the tip on top of it and applying vacuum, and then moved to the desired mounting site. On the mounting site, the μLED was lowered making sure that its electrodes and the previously conductive-resin-stamped Au tracks were aligned. Pressure is temporarily (0.02 N)

applied prior to the μLED release to ensure good mechanical contact with the substrate. The vacuum was then removed from the tip, releasing the μLED. The success of the mounting procedure could already be assessed at this point by applying electrical current to the tracks and observed if light is emitted. If poor connection was established, the tips were reutilized to press on top of the μLEDs and do small adjustments to its positioning to ensure good electrical connection. Finally, the last step of the process, was the curing of the resin, so it became rigid, and its conductivity enhanced.

To further test the procedure, the same steps were repeated with the smaller footprint μLEDs (LA UB06FP2) (Figure 53e,f). A smaller distance (25 μm) between conductive tracks for these components increased chances of short-circuit in the stamping procedure. The pick-and-place tip was not designed for this device's size, but successful pick-and-place was achieved.

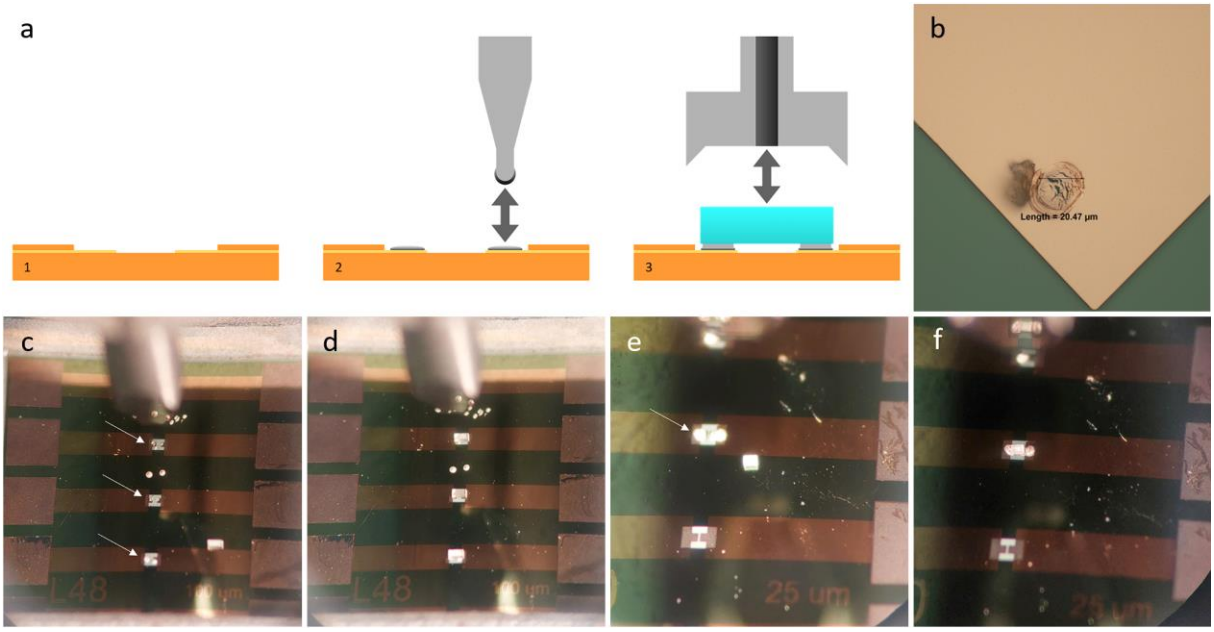


Figure 53 – Stamping and pick-and-place process.
(a) Schematic of the stamping and pick-and-place process. (1) The mounting site is ready with the tracks for connection of the μLED's electrodes exposed. (2) Conductive resin is stamped by using a wetted stamping tip. (3) The pick-and-place tip is used to grab the μLED by vacuum and relocate it on the mounting site, where it is placed by applying some pressure and removing the vacuum in the tip. (b) Effect of applying excessive force during the stamping procedure. An indentation is left on the Au track and some material is visibly lifted (c) μLED mounting test chip with 100 μm separating each Au track for connection. Conductive resin was already stamped, marked by the white arrows. A LA HB12FP1 μLED is also visible, with a footprint of 150 μm × 300 μm. (d) Chip in (c) after the pick-and-placing of the μLEDs. (e) Another μLED mounting test chip but only with 25 μm separating each Au track. Conductive resin was already stamped in the spot marked by the white arrow. An LA UB06FP2 chip is visible with only 89 μm × 150 μm footprint. (f) Chip in (e) with the μLED already pick-and-placed. The same pick-and-place tip used in (d) was also employed for this μLED size.

After correctly placing the μLEDs in position, the curing process can present a problem as it requires the components to be exposed to an increased temperature to an extended period. In the case of the resin used in this work, the recommended curing takes place over an hour, with a ramp of 30 minutes from

ambient temperature up to 150° C and a plateau at that temperature for the same amount of time. The LA HB12FP1 chips were first tested with this procedure and conditions and got successfully mounted on the substrate, withstanding the curing process. On the other hand, the smaller μLEDs, the LA UB06FP2, although operational before the curing process stopped emitting light after the curing. To ensure these smaller chips withstand the curing process, curing conditions were modified and a ramp of 30 minutes from ambient temperature up to 140° C was employed, followed by a plateau at this same temperature for 45 minutes, which resulted in a successful mounting of the uLED without damage.

The mounting of the μLEDs must be done before the assembly of all the three device's layers. The mounting site is located on the μLEDs array, fabricated on a rigid wafer but later released. Mounting the μLEDs immediately prior to the release of the layers would be beneficial, as one could take advantage of the provided rigidity to facilitate handling and mounting processes. For this to be possible, the conductive glue and the μLEDs should be able to withstand the harsh conditions of the etching of the sacrificial layer. To assess this possibility, LA HB12FP1 μLEDs were mounted on test chips and exposed to the process and conditions for release of the PI layers, involving exposure fo HF gas (see section 3.2.6). The results of this tests are depicted in in Figure 54. The utilized μLED was slightly mechanically damaged prior to the test, but it was fully functional upon application of electrical current and securely fixated on the substrate. However, after exposure to the release process, the μLED was destroyed in the process. In the OM images, it is possible to observe that the conductive resin remained in place, although the μLED got detached. This leads to the hypothesis that the μLED's electrode contacting the conductive resin was etched during the release process. Furthermore, the μLED was broken into multiple parts, rendering it unusable. These results indicate that the mounting of the μLEDs cannot take place before the release process. Thus, after fabrication of the device and its release, the μLEDs array must be handled independently to allow for the stamping, pick-and-place, and curing processes to take place.

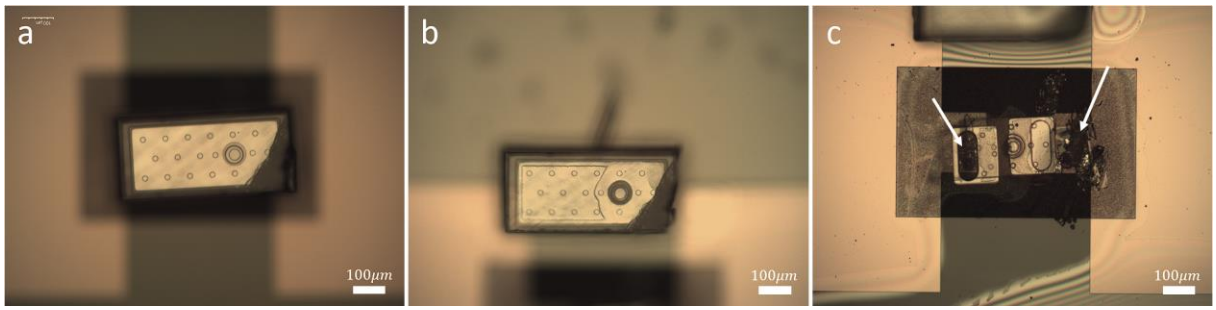


Figure 54 - Effect of the PI release process on the μLEDs.
(a) OM image of a mounted μLED prior to exposure to the PI release process. (b) Detached μLED after exposure to the process. A different texture is visible, implying that the release process modified the μLED. (c) Region in (a)

after the process, showing the absence of the bulk of the μLED. Some remnants of it are still near the mounting site. The white arrows regions indicate stamped conductive resin.

Mechanical robustness of the connection achieved when mounting the μLEDs is of paramount importance. To minimize the possibility of detachment of the μLEDs, an extra process was tested, posterior to the μLED mounting. This process consisted in the application of a transparent UV-cured glue on top of the μLED. For this, a custom stamping tip was printed utilizing an SLA 3D printer (Forms 3+, Formlabs), consisting of a tapered cone with a 400 μm diameter circular base. A process similar to the stamping of the conductive glue was applied and is depicted in Figure 55. A small drop of UV-glue is dispensed in the tip's reach, which is then dipped in it. Some of the adhesive remained in the printed tip which was then maneuvered to the already mounted μLED. At this point the wet tip gently touched the μLED from either the side or the top, in two different approaches, effectively transferring some of the UV-glue to the μLED and/or substrate. After this process, the UV-glue was cured by application of intense UV light for 5 seconds. Effectively, the only approach that improved adhesion to the substrate was the transfer of glue to the side of the μLED. Nevertheless, adding the UV-glue to the top of the μLED provided interesting modifications to the optical properties of the μLEDs, as the formed UV-glue dome (Figure 55e) possesses a shape resembling a lens. The optical properties of the LA HB12FP1 μLEDs are addressed in the next section.

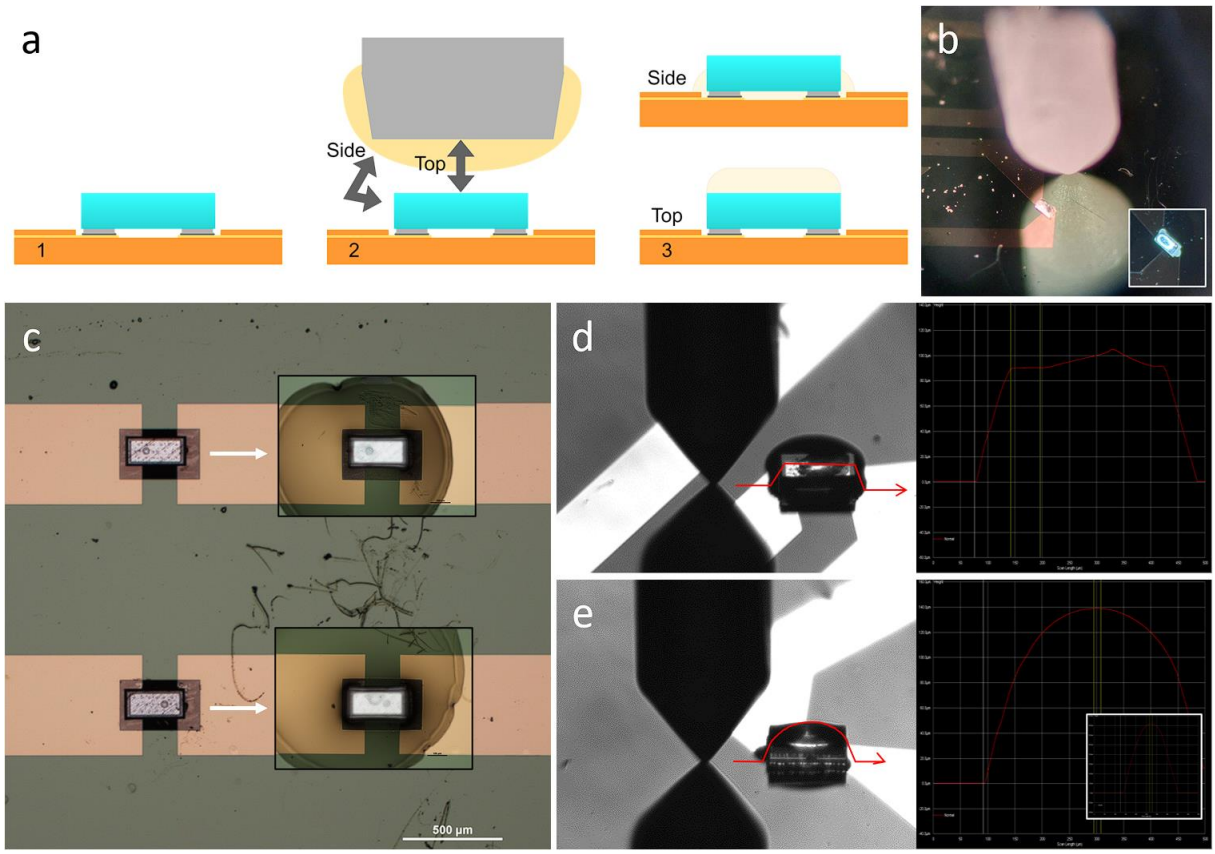


Figure 55 – Application of UV-glue.
(a) Schematic of the process for adding UV-glue to the mounted µLEDs. (1) The µLED is mounted with the stamping and pick-and-place process. (2) The printed tip is wetted in UV-glue and placed in the µLED by gently contacting it from the side or the top. (3) When contacted from the side the UV-glue spreads on the laterals of the µLED while it forms a blob on its top if contacted from the top. (b) Image of the printed tip close to a µLED (150 µm * 300 µm * 80 µm). (Inset) Visible light refraction after application and curing of the UV-glue on top of the µLED. (c) OM image of µLEDs before and after (insets) the application of the UV-glue on their sides. The darker regions in the insets correspond to areas covered in UV-glue. (d) Scanning tip of the mechanical profilometer next to a µLED with UV-glue applied from the side. The measured profile is visible in the right and is denoted by the red arrows. (e) Scanning tip of the mechanical profilometer next to a µLED with UV-glue applied from the top. The measured profile is visible in the right and is denoted by the red arrows. The inset is the obtained measurement when measuring in a direction perpendicular to the displayed one. A regular round shape is visible in both directions.

5.3 µLEDs Electrical and Optical Properties

After successfully mounting µLEDs with the stamping and pick-and-place technique, the optical properties of the µLEDs could be addressed. As the information displayed in the datasheet was reduced, no information on the I-V curve of the µLEDs and its relationship with the outputted optical power was mentioned. This information is crucial to tune the amount of current passing through the tracks and emitted optical power when stimulating the brain tissue.

The relationship between applied voltage, V_{LED}, current drawn, I, and emitted optical power, $P_{Optical}$, was addressed, with the setup described in section 3.3.6, for a single µLED mounted with the stamping and pick-and-place process. The results are plotted in Figure 56a.

In addition, the effect of the usage of the UV-glue on µLEDs' performance was assessed by measuring the current drawn and respective output optical power. The obtained results are depicted in Figure 56b for four different µLEDs mounted in the dummy wafer (see appendix III) with the stamping and pick-and-place process. The µLEDs LED 1 and LED 2 were subject to the UV glue process and correspond to the images Figure 55 (e) and (d), respectively, whilst the µLEDs 3 and 4 were not. A similar trend is visible for µLEDs 2, 3, and 4, showing an output of roughly 0.27 mW/mA, while the µLED 1 shows a steeper tendency of 0.34 mW/mA. The fact that µLED 1 shows a steeper curve and can achieve a higher optical power output can be attributed to the presence of a dome shaped UV-glue blob on top of it, which could potentially improve the light focus on the sensor. To confirm this hypothesis, the µLEDs were lit near a white sheet of paper to inspect the shape of the beam and its diffusion. The results are visible in the insets of Figure 55b, where it is noticeable how light propagates differently depending on the use of the UV-glue on top of the µLED or not. Although µLED 2 is also partially covered with UV-glue, it does not present focusing properties. Nevertheless, no difference is visible in relation to µLEDs 3 and 4 in terms of output optical power, meaning that the UV-glue is transparent to the output wavelength and will not reduce their efficiency. These conclusions imply that utilizing the UV-glue can be advantageous for enhancing the mechanical reliability of the µLEDs mounted by this process without drawbacks in output optical power.

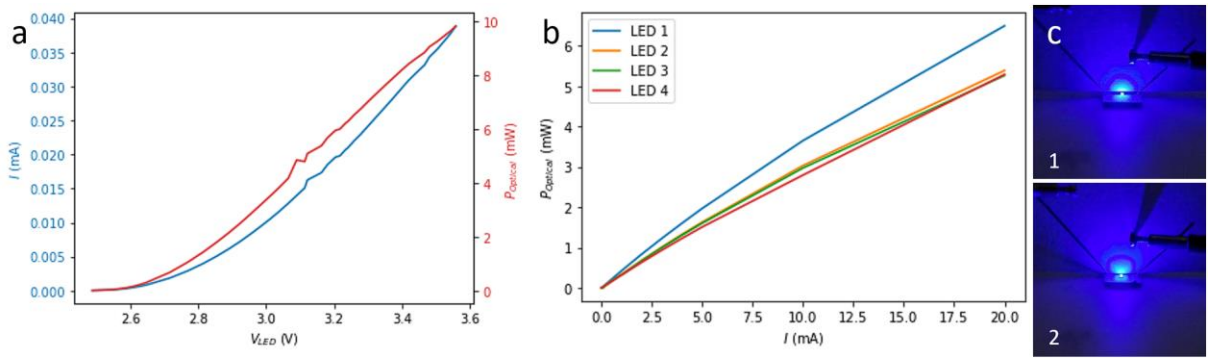


Figure 56 – Measured electrical and optical properties of the µLEDs.
(a) Plot of the drawn current, I, and the measured optical power, $P_{Optical}$, of a µLED as a function of the applied voltage, V_{LED}. (b) Plot of the optical power as a function of the draw current for four mounted µLEDs. LED 1 and LED 2 correspond to the µLEDs in Figure 55 e and d, respectively. (c) Visualization of the emitted light by µLEDs with UV-glue applied from the side (1) and top (2). Light appears more focused towards the top in the µLED in (2).

5.4 Concluding Remarks on μLED Mounting

The task of mounting μLEDs on patterned Au tracks of a wafer was successfully achieved. The first approach tested, using soldering, proved to be non-viable. The alternative solution, using conductive resin was successful in not only achieving an electrical, but also a mechanical connection between the μLED and the tracks on the substrate.

The stamping and pick-and-place of the μLEDs was very successful, providing the intended connection. The techniques were also space-efficient, occupying a footprint not larger than the μLED itself. Although the soft PI substrate could be damaged during stamping, reliable connections managed to be secured with enough care. Furthermore, the possibility of utilizing UV-glue to further enhance the mechanical reliability of the mounting is very beneficial for the overall reliability of the final device, increasing the toughness of the connection. The successful mounting of the μLEDs also allowed for the measurement of their light output capabilities in order to tune the output of power necessary in the final device, already taking into account the transmittance of the PI.

In summary, the mounting of the μLEDs was successful by utilizing the stamping and pick-and-place approach, and relevant properties were measured. These results allow for a smooth integration of the light emitting components in the projected neurochemical graphene-based sensor without the need for a complex microfabrication of μLEDs on the polyimide. In turn, the fabrication of the overall device becomes facilitated, more reliable and economic.

6. Graphene Dry Transfer

The dry transfer of graphene is a promising technique to scale graphene technologies, making them cleaner, more controllable, and more affordable. For it to become widely used, different drawbacks must be addressed, and some mechanisms must be understood. In this section, the dry transfer of graphene is explored, and different aspects are taken into account to optimize the process to the point that it becomes a reliable technique for the fabrication of graphene devices, as the one developed in this thesis. The development of the dry transfer of graphene in this work was not linear, and different aspects of the process were only understood after various trials and errors. This section is divided into two main parts to facilitate understanding. The first one will encompass in a general manner the processes required to reliably transfer the graphene from the growth substrate onto the final substrate by the usage of an intermediate water-soluble support polymer, PVA. The second section will explore different approaches for the dry transfer process, causes affecting reproducibility, and detail the underlying mechanisms in graphene decoupling from the Cu substrate.

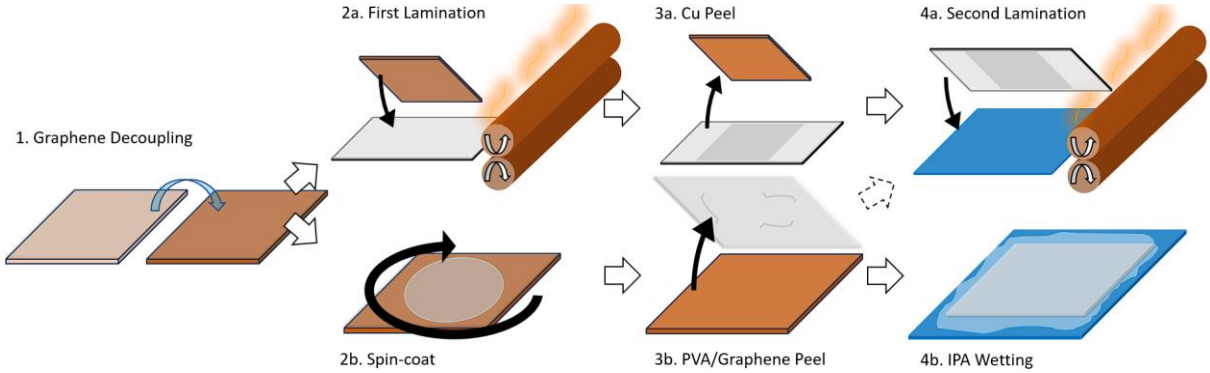


Figure 57 - Routes for the dry transfer of graphene.
(1) Graphene decoupling is necessary for both possible routes of transfer. (Top) (a) The lamination process entails a first lamination (2), followed by the peel of the Cu, leaving graphene on PVA (3), and finally, a second lamination onto the target substrate (4). (Lower) (b) The spin-coat process requires the PVA to be spin-coated and cured, forming a thin layer (2) that is then carefully peeled together with the graphene (3) and finally transferred by wetting the surface of the target substrate with IPA and laying the thin PVA with the graphene facing down (4). However, the lamination route can also be taken at this stage, represented by the dashed arrow.

The dry transfer process encompasses very distinct steps, each with its nuances. In the approach studied here, the whole process can be divided into three main parts: the graphene decoupling from the Cu native substrate (Figure 57.1), the transfer onto the PVA support polymer (Figure 57.2,3), and finally, the transfer onto the desired target substrate (Figure 57.4).

The detailed study of the first step will be delayed to section 6.2, and emphasis will be put on the last two steps in section 6.1.

6.1 Graphene Transfer from the Native Substrate

The graphene-Cu decoupling step is always performed before the transfer onto the PVA-supporting polymer. Assuming the decoupling step does not limit the quality of the transfer (although it certainly does), the most critical steps are the two following transfers. In this work, two approaches, depicted in Figure 57, were tested: lamination and spin-coating of the PVA. Although these two approaches utilize the same support polymer, they perform differently. On the one hand, the former requires significant forces to be applied during lamination to ensure good mechanical contact. Still, it then provides straightforward graphene peeling and reliable support between transfers. On the other hand, the latter presents a more delicate way of applying the support polymer but also requires more delicate peeling and handling.

The two approaches were tried multiple times with many different CVD graphene on Cu samples. The following sections highlight the main differences and effects of the lamination and spin-coating approaches, mainly by roughly analyzing the transferred graphene sheets' electrical resistance, coverage, and Raman spectrum. The randomness associated with different CVD graphene samples did not allow for quantitative comparisons.

6.1.1 Polyvinyl Alcohol Lamination

The lamination of PVA on top of the CVD-grown graphene on Cu was first demonstrated in [14]. In this work, one tried to reproduce their results by employing a similar process (Figure 31), described in section 3.4.4 albeit with different graphene growing parameters and a different PVA foil.

Initially, the temperatures in [14] (110°C for all laminations and bakes) were also employed. However, due to the different specifications of our PVA foil, these had to be changed and optimized. It was observed that the first lamination process (Figure 57.2a) produced lower graphene-on-PVA (Figure 58b) electrical resistances when higher temperatures, in the 130-160°C range, were applied, and a consequent longer cooling time was needed prior to peeling of the Cu from the PVA. The lower electrical resistance can be attributed to a more successful lamination process, which ensures better mechanical contact between the PVA and the graphene as the polymer gets softer and more readily conforms to the graphene/Cu

substrate. The higher temperature and prolonged cooling expose the PVA to a bigger temperature and deformation amplitude due to thermal expansion/contraction. The contraction of the PVA during the cooling can aid in decoupling the graphene from the substrate. The effect of graphene-substrate decoupling has been demonstrated in [57], where contraction forces improved transfer yield. Longer curing times for a resin applied on top of graphene allowed for enhanced compression, which facilitated delamination.

During the second and final lamination of the graphene (Figure 57.4a) onto the final substrate, higher temperatures were also employed, in the 130-140°C range, contributing to better results, attributed to enhanced conformation of the PVA to the substrate. Nevertheless, exposing the PVA to overly high temperatures overbaked it to a point where it was hard to remove by immersion in DI water in the final step, and significant amounts of PVA residues were left on top of the graphene surface, reducing the transfer quality.

One critical aspect of the lamination approach is that significant amounts of Cu residues were present in transferred samples (Figure 58a). The residues were attributed to the lamination process and the presence of Cu oxides. These oxides are typically mechanically weak and weakly coupled to graphene, thus easily detaching from the substrate if enough force is applied. This detachment can be induced by peeling the Cu from the PVA after the first lamination, and residues of Cu oxides remain on the graphene transferred onto the polymer. The Cu oxide residues then unwantedly transfer onto the target substrate.

Furthermore, another critical aspect of the lamination process was the formation of air bubbles amid the first and second lamination (Figure 58a). As the lamination was not performed in a vacuum, air was always present between the two laminated materials, and was not able to be pushed out by the pressing forces. It then became trapped and created air bubbles that hindered good conformity and coverage. This phenomenon was especially noticeable after the second lamination (Figure 58c) by looking at the graphene before the removal of the PVA (Figure 58d). Air pockets formed between the substrate and the PVA resulted in compromised transfers, resulting in small regions with no graphene coverage (Figure 58e). These aspects contributed to poorer conductivity of the graphene sheet.

Although the lamination approach is very convenient, problems such as the graphene's cleanliness, Cu residues, and air bubbles may hinder its viability for large-area transfer and application on more complex graphene devices, and thus a different approach was tried in the next section.

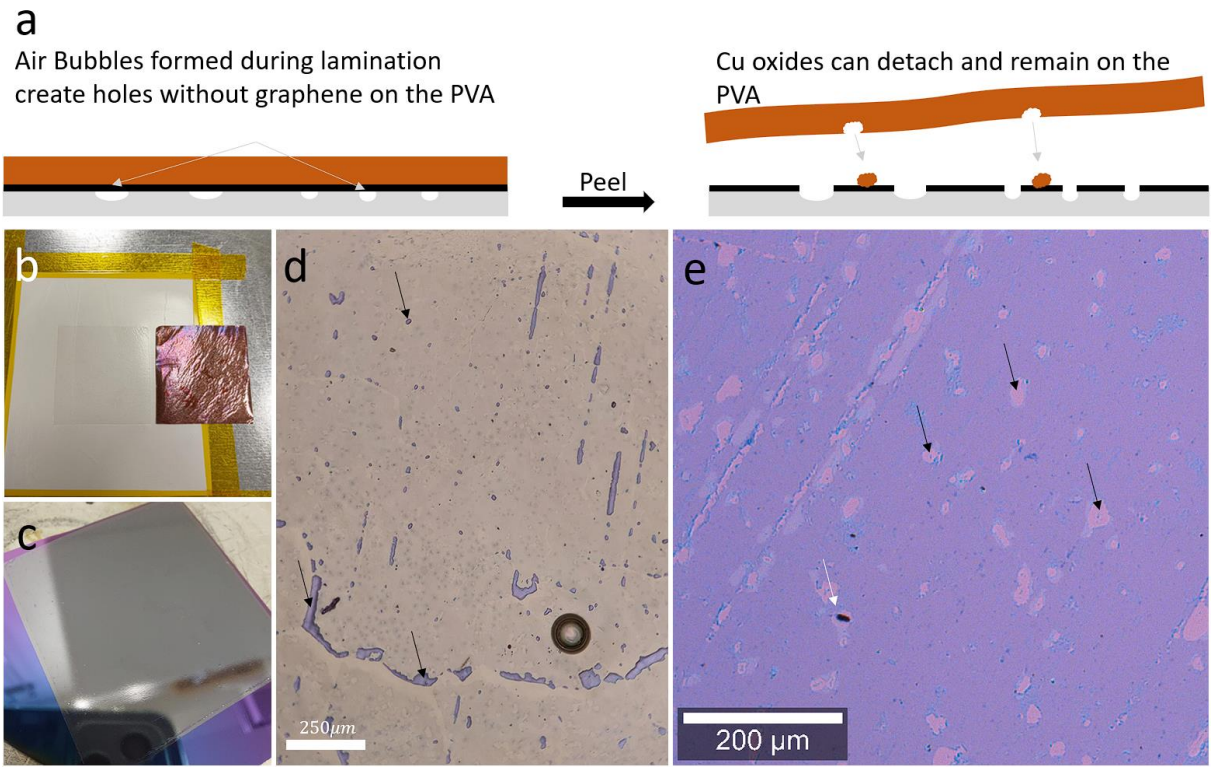


Figure 58 – Lamination transfer process and drawbacks.
(a) Schematic of the formation of bubbles and Cu oxide residues during lamination of the Cu/graphene (left) onto PVA and peeling (right). (b) Image of graphene-on-PVA and the respective Cu growth substrate. Graphene is seen as a darker square in the middle of the PVA sheet. (c) PVA/graphene/SiO_2 during baking on a hotplate after removal of the support paper. (d) OM image of the stack in (c). Examples of formed air bubbles due to the lamination process are pointed with black arrows. (e) Results of the dry transfer via lamination onto SiO_2 under the OM. The black arrows point to holes in the graphene sheet due to the formation of air bubbles during lamination. The white arrow points at a Cu oxide residue.

6.1.2 Polyvinyl Alcohol Spin Coating

Applying the PVA support polymer to the graphene becomes more manageable if liquid. It avoids the need for intense pressing forces that could damage the graphene. Furthermore, it avoids the formation of air bubbles, as trapped air can slowly escape through the liquid, and a smooth surface coverage is achieved. PVA can be spin-coated on top of the CVD-grown graphene as an aqueous solution and later dried to form a mechanically stable flat support polymer that can be peeled [152]. This approach was tried as described in Figure 32 and section 3.4.5.

The spin-coating of the PVA onto the CVD graphene on Cu was achieved by mounting the metal foil on a support substrate (Figure 57.2b). After the spin-coat step, two different routes were taken: curing by baking on a hot plate or letting the PVA solution dry at room temperature. Both curing by baking or drying at room temperature induce the same compressing effect previously mentioned, but the latter method avoided the exposure of the PVA to increased temperatures, which can prevent the formation of residues challenging to remove from the graphene's surface (Figure 60). Given this, drying the PVA at room temperature was the preferred method.

After the solidification of the PVA on top of the graphene, the peeling followed (Figure 57.3b). The PVA film achieved was very thin and fragile. The PVA polymer was peeled off the Cu foil, contrary to what happens in the lamination approach, where the PVA foil is fixated on a support substrate and the Cu peeled. This inversion reduced the amount of Cu oxide residues, as the Cu foil no longer needed to withstand peeling forces. On the other hand, the PVA and graphene were subject to these forces, which can induce cracks and defects as the PVA easily deforms either elastically or plastically (Figure 59a). Thicker layers of PVA could be spin-coated to reduce this effect, but it brings drawbacks in the following transfer step.

Transferring the graphene from the support polymer onto the target substrate took two different routes. The first was the previously discussed route of lamination (Figure 57.4a). Nevertheless, lamination-induced problems were unavoidable and, in some instances, amplified. As the PVA film in the spin-coating case was thinner, it was harder to maintain in a flat state, and wrinkles or air bubbles formed more easily (Figure 59b). Furthermore, the PVA needed to be exposed to higher temperatures, possibly complicating its removal. The second option for completing the second transfer onto the target substrate was to take advantage of the thin PVA layer. The support polymer and the graphene were carefully laid on a wet surface by wetting the target substrate with IPA (Figure 57.4b). Surface tension forces ensured that the thin PVA film and the graphene became flat as the underlying IPA slowly evaporated, avoiding exposure to higher temperatures and harsher mechanical forces, preserving graphene integrity.

The graphene transfer process was finished after the removal of the PVA film by dissolution in DI water. Overall, cleaner samples were achieved utilizing the IPA-assisted technique for the second transfer, and fuller coverage of graphene is observed on the target substrate. Nevertheless, the drawback of possibly enhancing the number of defects was present. The enhancement of defects is very noticeable in Figure

59d Raman spectrum. Although graphene coverage appeared to be continuous, a high intensity of the D peak was visible, with an intensity in the order of the G peak, which is not desired.

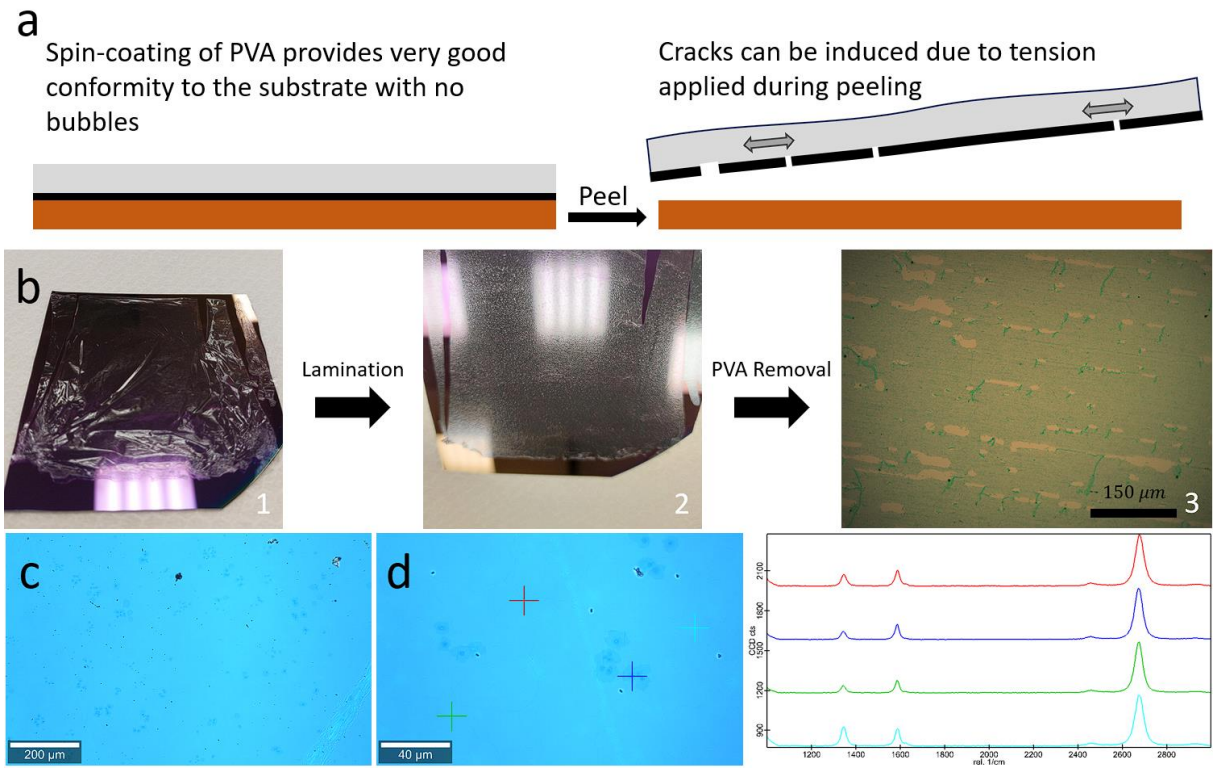


Figure 59 – Spin-coat transfer process and drawbacks.
(a) Schematic of the formation of cracks on graphene during peeling after the spin-coating of PVA. The stretching of the PVA can break the graphene. (b) Transferring the spin-coated and peeled PVA/graphene via lamination. The peeled stack is the first layer on the target substrate with graphene facing down (1). The following lamination creates many bubbles due to the non-planarity of the PVA/graphene stack, as the PVA is very thin (2). The formed bubbles are spread throughout the graphene sheet and visible under the microscope (3). (c) OM image of graphene on SiO_2 transferred by spin-coated PVA and IPA final transfer. The graphene appears continuous with no visible cracks or holes. (d) Higher zoom image of (c) and respective Raman measurements (right). The D peak is evident at the 1350 cm^{-1} mark, with an amplitude close to that of the G peak at the 1580 cm^{-1} mark. Although all spectra correspond to monolayer graphene, the dark blue cross is on a darker patch of graphene, meaning the spectrum corresponds to decoupled multilayer graphene, presenting as monolayer graphene through the Raman measurements.

6.1.3 Direct Comparison

In the previous sections, the two utilized semi-dry transfer processes were discussed, and it was observed that each had different effects on the overall quality of the transferred graphene sheets. To better understand the advantages and disadvantages of each transfer process, CVD graphene samples originating from the same CVD graphene growth run were transferred in parallel to similar SiO_2 substrates. The laminated sample followed the process described in Figure 31, while the spin-coated sample followed the path denoted by the dashed arrow, in which the second transfer onto the final substrate was done by

lamination. Results can be seen in Figure 60. The laminated sample presented lower electrical four-point resistance values, close to 1.5 kΩ compared to values around 2.5 kΩ for the spin-coated sample. Although the coverage in graphene appears to be greater in the spin-coated sample, this is an area where there was no air bubble formation. A more representative region is observed in the inset of Figure 60b, showing large holes in the spin-coated sample due to air bubble formation (Figure 59b). Furthermore, in the Raman measurements, it is possible to argue that slightly higher peaks corresponding to defects at the $1350\ cm^{-1}$ point are visible in the spin-coated sample, which can be attributed to defects created during the peeling process of the PVA, contributing to higher resistance. Poorer coverage of graphene in some regions was attributed to the air bubble formation. Nevertheless, the laminated sample showed a higher density of residues, visible as dark spots in Figure 60a, which contrasts with the spin-coated sample, which has a cleaner appearance.

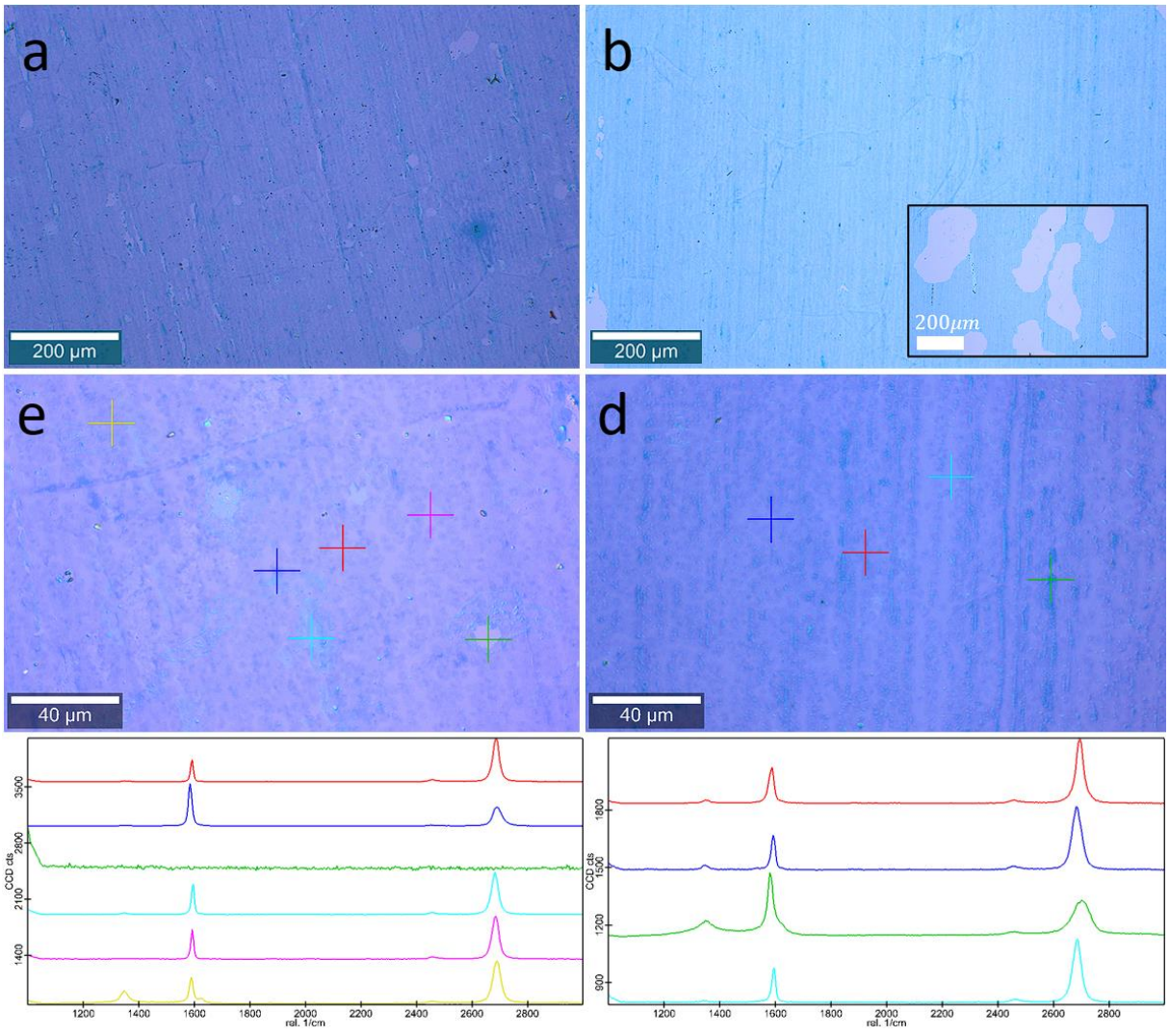


Figure 60 – Comparison of lamination and spin-coat + lamination transfer processes.

OM image of a region of transferred graphene by the lamination transfer process (a) and spin-coat + lamination transfer process (b). The inset of (b) shows a region where bubble formation occurred during the lamination of the spin-coated PVA and graphene. (c) Higher zoom image of (a) and respective Raman measurements. There is continuous graphene coverage except in the green cross, where an air bubble prevented successful transfer, and no signal was observed at the G and 2D peak regions. (d) Higher zoom image of (b) and respective Raman measurements. Graphene coverage is continuous. An increased number of defects is present at the green cross. (c,d) Throughout the OM images, it is possible to observe bright blue dots attributed to PVA residues due to the heat applied during the lamination processes.

To further compare both approaches and to test their viability on a different substrate of interest, CVD graphene samples were dry transferred onto the dummy wafer (appendix III), which had already patterned Au tracks on polyimide. In this case, the transferred samples did not originate in the same CVD run, and thus, electrical resistance measurements were not performed to compare the two transfer processes. Furthermore, the PI substrate makes it very complicated to acquire a Raman signal from graphene (see appendix VII). As such, OM and SEM images were utilized to assess the quality of each of the transfer processes (Figure 61). The two transfer processes, lamination, and spin-coating (with IPA-assisted transfer) produced distinct results visible in the OM and corresponding SEM images. The laminated sample presented many tears attributed to the formation of air bubbles amid the lamination process, visible in the OM images taken before the removal of the PVA support in the inset of Figure 61a, highly compromising the graphene coverage. The tears visible in the OM images became even more evident under the SEM (Figure 58c,e), where it was assessed that the coverage of graphene in the PI substrate areas is inferior, culminating in various charging artifacts forming in the acquired images. These aspects are highly contrasting to the spin-coated sample, where the coverage appeared smooth in the OM and SEM images, with no visible charging artifacts appearing in the PI substrate areas (Figure 58b,d,f). These evident differences somewhat vanished by analyzing graphene-covered regions at a smaller scale, as both samples closely resembled each other (Figure 58g,h). Small filament-like objects are visible throughout the graphene sheets, which were absent in the wet transferred graphene onto the device wafer (see section 4.2.4), leading to the possible conclusion that they were PVA residues and pointing towards the need to improve the PVA removal process. Furthermore, at the step-edges separating the PI substrate from the Au tracks, no evident differences were discernible, hinting that although the lamination process requires the application of pressing forces, these do not play a significant role at this scale and do not induce fractures on the graphene when non-flat target substrates are used. Tiny bright spots were visible throughout the images in both the laminated and spin-coated samples, but by examination of a region of the dummy wafer where no graphene transfer took place (inset of Figure 61g), it was concluded that these residues were not related to the dry transfer of graphene, as they are present throughout the whole wafer.

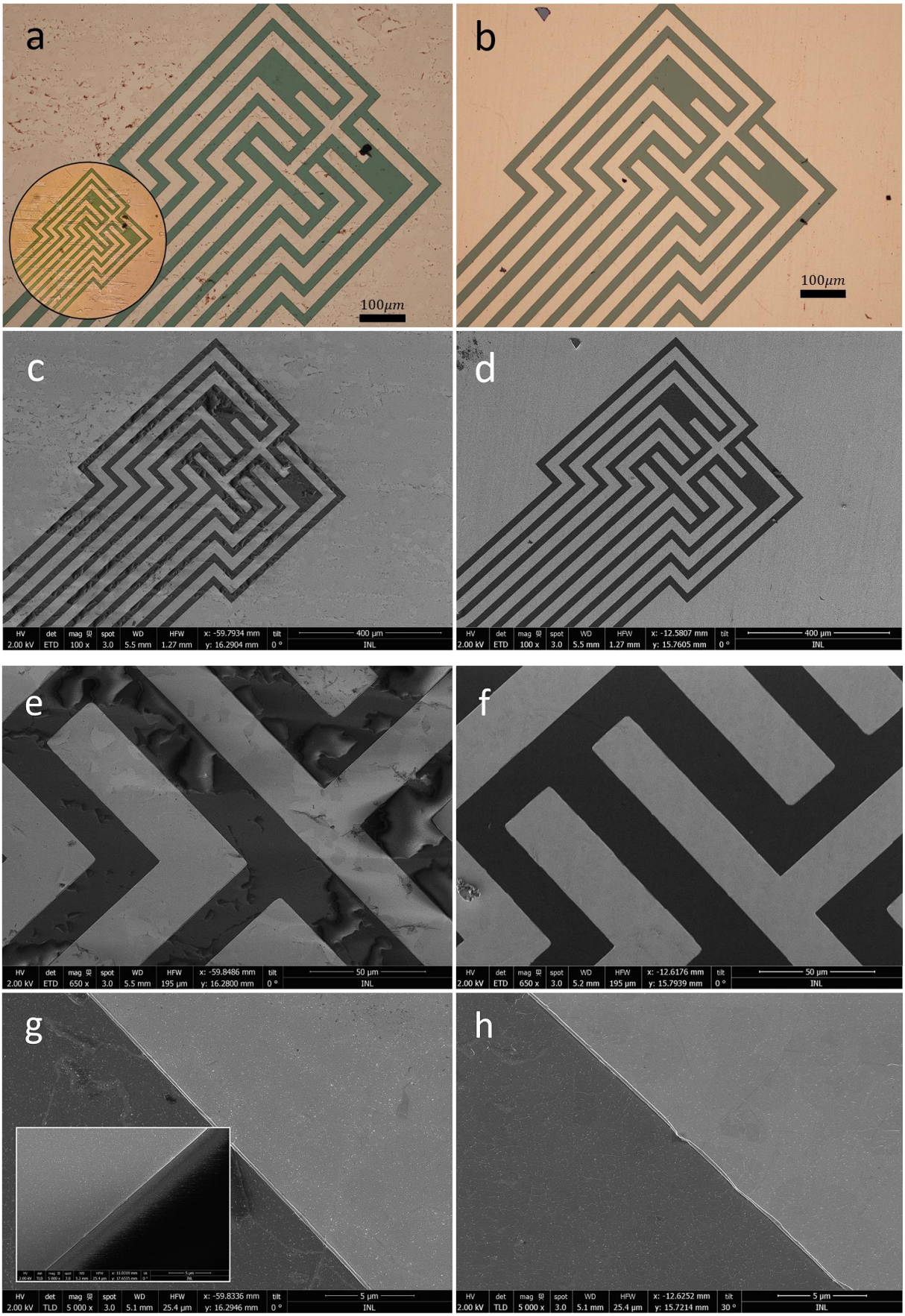

a
100μm
b
100μm
c
HV 2.00 kV | det ETD | mag 100 x | spot 3.0 | WD 5.5 mm | HFW 1.27 mm | x: -59.7934 mm | y: 16.2904 mm | tilt 0 ° | 400 µm | INL
d
HV 2.00 kV | det ETD | mag 100 x | spot 3.0 | WD 5.5 mm | HFW 1.27 mm | x: -12.5807 mm | y: 15.7605 mm | tilt 0 ° | 400 µm | INL
e
HV 2.00 kV | det ETD | mag 650 x | spot 3.0 | WD 5.5 mm | HFW 195 µm | x: -59.8486 mm | y: 16.2800 mm | tilt 0 ° | 50 µm | INL
f
HV 2.00 kV | det ETD | mag 650 x | spot 3.0 | WD 5.2 mm | HFW 195 µm | x: -12.6176 mm | y: 15.7939 mm | tilt 0 ° | 50 µm | INL
g
HV 2.00 kV | det TLD | mag 5 000 x | spot 3.0 | WD 5.1 mm | HFW 25.4 µm | x: -59.8336 mm | y: 16.2946 mm | tilt 0 ° | 5 µm | INL
h
HV 2.00 kV | det TLD | mag 5 000 x | spot 3.0 | WD 5.1 mm | HFW 25.4 µm | x: -12.6252 mm | y: 15.7214 mm | tilt 30 ° | 5 µm | INL

Figure 61 – Dry transfer process by lamination (a,c,e,g) and spin-coat (b,d,f,h) onto the dummy wafer comparison.
(a,b) OM images of the transferred graphene on the Au tracks (gold-colored) on PI (green-colored) of the dummy wafer. In the inset of (a), a sample OM image before the removal of the PVA, where air bubbles can be observed in the form of brighter areas. (c,d) SEM images corresponding to (a,b), respectively. Dark regions correspond to PI, while lighter regions correspond to the Au tracks. Slight changes in the shade are attributed to the presence (darker) or absence (lighter) of graphene on the Au tracks, while the presence or absence of graphene on the PI is attributed to the non-formation or formation of artifacts, respectively. (e,f) Higher zoom SEM images of the regions in (c,d). (g,h) SEM images zooming on Au edges covered in graphene. The inset in (g) shows an edge where no graphene transfer occurred.

These results put the dry transfer utilizing spin-coated PVA at a higher standard, but care should be taken as excessive peeling force, as already mentioned, can damage the graphene. In a distinct run of the dry transfer utilizing spin-coated PVA onto the dummy wafer, although graphene coverage seemed very good by observing the transferred area at a large scale, more careful examination revealed extended fractures on the graphene following a brick-like pattern, attributed to excessive forces and deformations applied during the peeling step from the Cu substrate. These features explain the highly intense D-peaks present in the plots of Figure 59d, where although OM images show no visible cracks, a similar effect visible in the SEM images probably took place during the transfer of that sample.

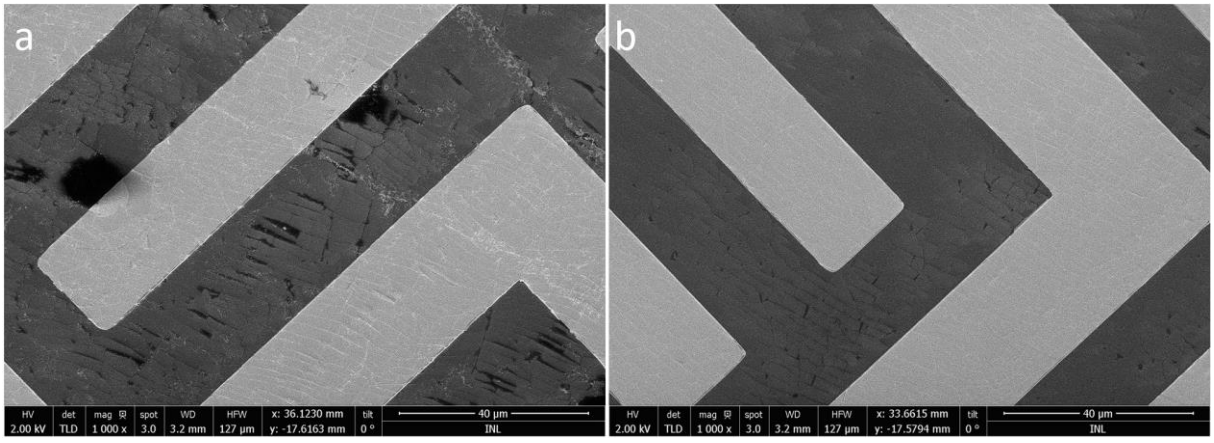


Figure 62 – SEM images of fractured graphene transferred by the spin-coat approach.
Although the effect is more pronounced in the region depicted in (a), it can be noticed that it is also present in (b), with both images presenting a brick-like fracture pattern.

Considering all of the mentioned aspects, strong arguments could be made to favor any of the two transfer processes utilized in this work. However, if one aims to reduce Cu residues and maintain a high degree of graphene coverage, the spin-coating process has the edge, although delicate peeling is essential to obtain a high-quality transfer.

6.2 Decoupling Graphene from Copper

The processes above for transferring graphene from the Cu native substrate onto the PVA support polymer and onto the target substrate are significant in the successfulness of the semi-dry transfer procedure. Nevertheless, they highly depend on decoupling graphene from the Cu native substrate, which will not happen if the adhesion force between PVA and graphene fails to exceed the adhesion force between the 2D material and the native substrate [61]. Moreover, a partial decoupling from the Cu substrate inhibits delamination and transfer onto the PVA support polymer and affects the obtained graphene coverage on the final substrate [71].

During the development of this work, distinct behaviors between CVD-grown graphene samples were observed, with different samples producing consistently distinct results when dry transferred, although the same processes were employed. Therefore, a deeper investigation of the decoupling phenomenon was required to optimize the dry transfer process.

6.2.1 The Effect of Graphene Nucleation Site Density

Different CVD graphene samples were transferred by dry transfer, producing very different results for the same transfer process. The high number of tunable parameters of the growth and transfer of the graphene and the fact that experimental conditions are hardly exactly reproducible complicates the interpretation of the results. Nevertheless, a remarkable tendency was observed when OxGr and noOxGr samples (see section 3.4.1) were utilized.

On average, noOxGr samples presented lower electrical resistance measurements after the completion of a dry transfer of graphene, independent of the kind of transfer process utilized. Furthermore, before the transfer onto the final substrate, graphene patches on the PVA support presented a different shade depending on whether the sample was OxGr or noOxGr. Figure 63d shows that the noOxGr sample has a darker appearance than the OxGr sample, although both were decoupled and transferred under the same conditions.

Moreover, by analyzing OM images of both graphene samples after the dry transfer process, these differences in shading were translated in many darker areas throughout the noOxGr sample. It is well known that although graphene is a transparent material, it absorbs a small percentage of light, meaning that multilayers of graphene will have lower transmittance and thus appear darker under the OM than monolayer graphene [26]. Raman measurements on both samples also revealed that the noOxGr samples present more multilayer graphene areas than OxGr samples by analyzing the ratio between the 2D and

G peaks. It is worth noting that although multilayers of graphene translate in a smaller 2D/G ratio, there are instances where stacked graphene layers do not produce the expected Raman signal, showing the same behavior as monolayer graphene (turbostratic graphene) [153]. These multilayers can be decoupled from each other, acting as multiple distinct monolayers and providing an augmented single-layer Raman signal. Nevertheless, they still present as darker areas under OM images. Thus, OM image inspection is more reliable when assessing the number of graphene layers on a compatible substrate.

The darker regions are typically associated with nucleation sites of graphene, where double or multilayer growth can occur [154]. Extensive studies have shown correlations between the oxidation state of the Cu growth substrate before the graphene CVD growth and the number of nucleation sites [155]. These studies point out that the pre-oxidation of the Cu substrate reduces the number of nucleation sites, increasing the size of the crystallites and resulting in a higher degree of monolayer graphene. Due to the pre-oxidation of the Cu substrate, the oxygen incorporated at the surface scavenges deleterious carbon and aids in achieving a clean sample, effectively decreasing the available nucleation sites. The nucleation site density directly correlates with the crystallinity of graphene, as more nucleation sites imply a more significant number of graphene crystals, meaning that the grain boundaries encountered in noOxGr will be significantly increased when compared with OxGr. Furthermore, nucleation sites and grain boundaries are known to be a pathway for the diffusion of molecules, facilitating the intercalation of H_2O and O_2, which are crucial for the oxidation of the interface between the graphene and the substrate in the decoupling stage of the dry transfer.

Combining these facts allows us to understand why noOxGr samples present a reduced electrical resistance since they are more easily decoupled from the substrate due to the enhanced intercalation of water and oxygen molecules. Thus, the dry transfer process occurs more smoothly, preserving graphene's structural integrity.

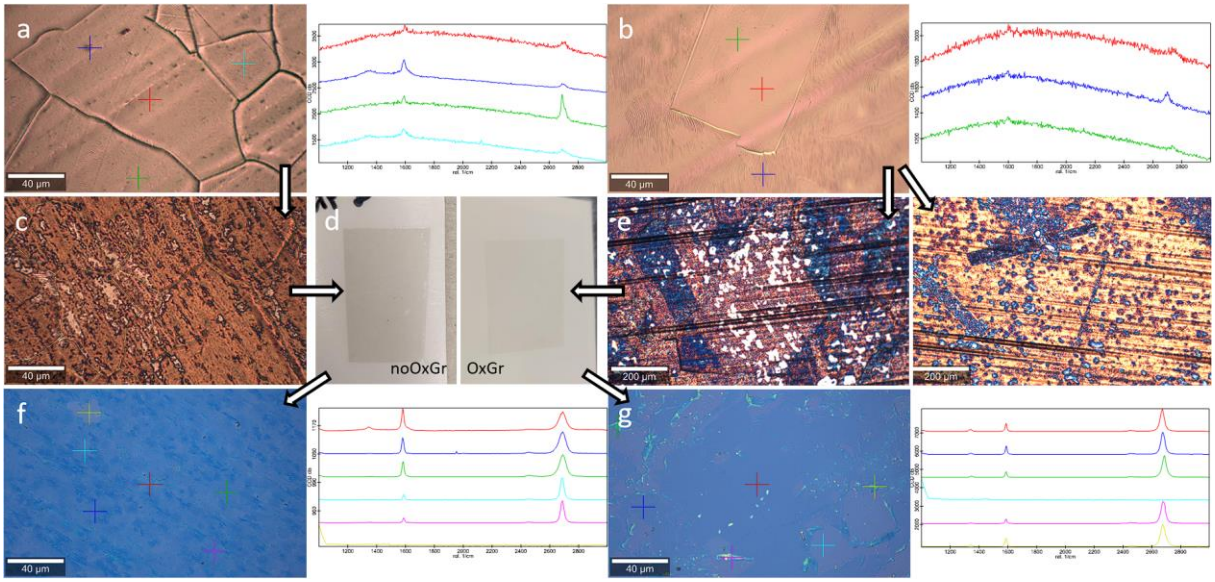


Figure 63 – Images depicting the steps in transferring noOxGr and OxGr samples by lamination. (a,b) OM images and respective Raman measurements of noOxGr and OxGr, respectively. The noOxGr samples appear "dirtier" than OxGr samples, although many wrinkles are visible in the latter. Graphene coverage appears continuous on both types of samples. (c,e) OM images of noOxGr and OxGr samples after oxidation in DI water, respectively. The former presents a very homogeneous behavior, while the latter can give rise to differently colored Cu substrates depending on the region. (d) The appearance of noOxGr and OxGr samples after transfer onto the PVA support polymer. The noOxGr samples appear as darker patches than OxGr samples. (f,g) OM images and their respective Raman measurements of noOxGr and OxGr samples, respectively, after dry transfer onto SiO_2. The noOxGr sample shows darker spots throughout the transferred area, which can be interpreted as nucleation sites with multilayer graphene, confirmed by the Raman measurements. The OxGr sample shows a higher prevalence of monolayer graphene. In this case, many regions with no graphene coverage are visible in the OM image, shown as lighter-colored parts, and folded graphene is visible as bright filaments.

The OxGr samples presented a different behavior towards oxidation by immersion in DI water (Figure 63e). The oxidation of the Cu surface was heterogeneous throughout the sample, and some regions do not get oxidized entirely, as observed by their apparent color under the OM. By performing Raman measurements on these regions (Figure 64), it was possible to observe that the non-transferred regions mainly correspond to multilayer graphene areas, which preserve the non-oxidized state of the Cu substrate directly below them. Even so, this behavior was not homogenous, as different multilayer regions of the samples appear to decouple the substrate successfully. Figure 64a represents one of these Cu substrate regions with heterogeneous behavior and the corresponding area after the graphene is transferred onto a SiO_2 substrate (Figure 64b). It becomes evident that the top portion of the OM image of the substrate, which presents a different color (and thus a different degree of oxidation) from the rest, corresponds to an area on the SiO_2 samples with better graphene coverage, namely in the multilayer regions. Furthermore, these multilayer regions presented an enhanced oxidation rate near the edges and

sometimes the center, similar to the behavior of individual graphene flakes immersed in water in Figure 7a [69].

These heterogeneities also applied to monolayer regions, as different areas of the OxGr samples appear to get the Cu substrate to oxidize at different rates. Different colors obtained by the Cu growth substrate after immersion in DI water were correlated with different degrees of oxidation, which appear to be different in different Cu grains. These facts hinder homogeneity and good coverage after transferring OxGr samples. Similar effects have been noted in several studies correlating the apparent oxidation of the Cu substrate underlying graphene and its crystallographic orientation [74], [156], or even the relative crystallographic orientations between Cu and graphene [157].

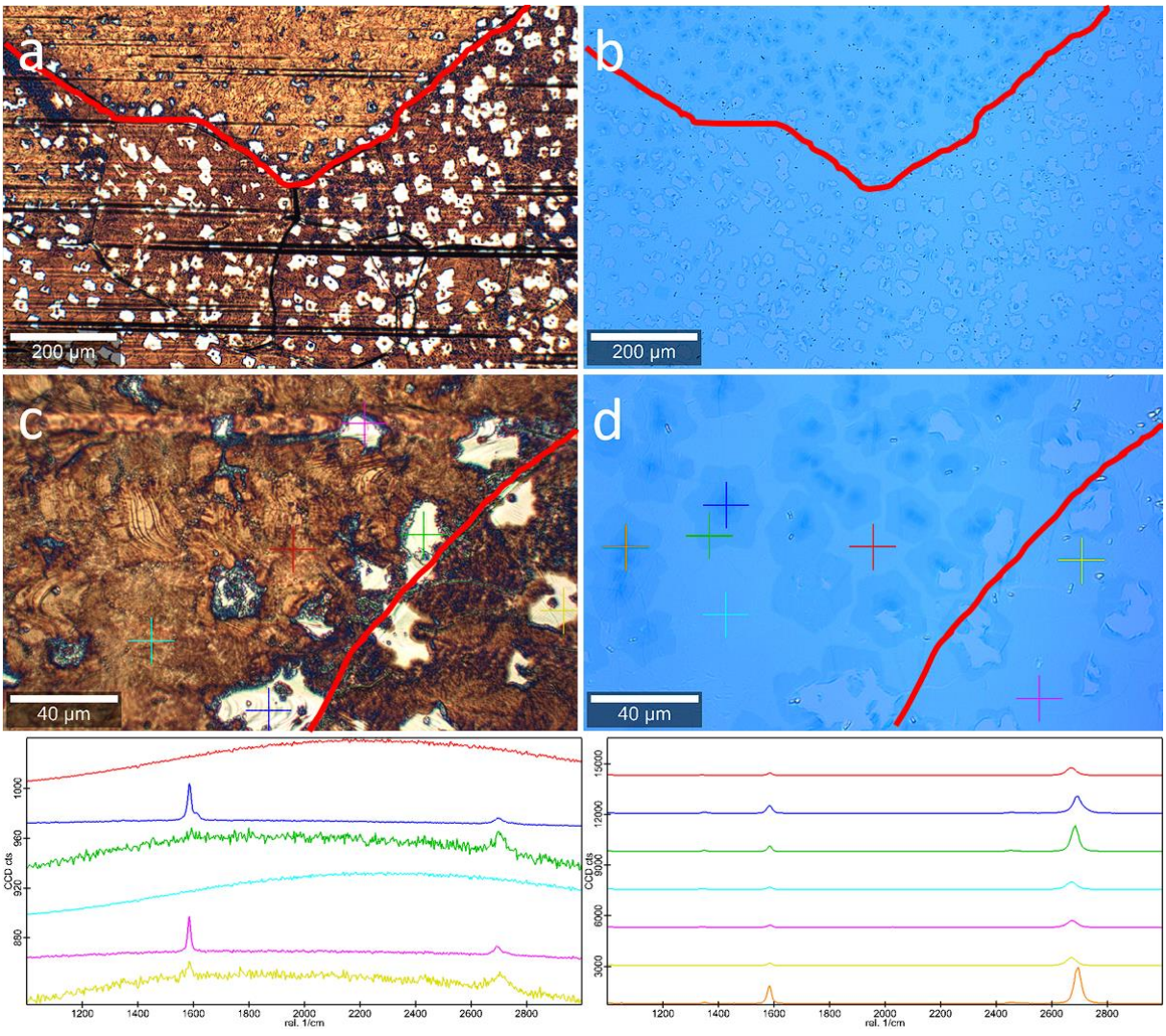


Figure 64 – Different behavior of OxGr samples in respect to the decoupling.
(a) OM image of the boundary between regions with different behaviors and the corresponding transferred graphene onto a SiO_2 substrate. The red line delimits the same two regions in both images, in which the upper region appears to have a higher coverage of graphene than the lower one. (c) OM image and the respective Raman measurements of a zoomed region of (a) after the graphene transfer. (d) Graphene transferred from the region in (c) onto a SiO_2 substrate and respective Raman measurements. It can be observed that the non-oxidized regions (bright colored) in (c) show the presence of graphene by observing the Raman measurements, and a light

color in (d) is visible in the corresponding regions, effectively showing that non-oxidized regions of the substrate hinder the graphene dry transfer. The red line denotes the boundary between the two regions in (a,b). Also, while all Raman measurements point to monolayer graphene in (d), the OM image shows that dark blue, green, and orange crosses are on top of multilayer graphene.

6.2.2 Enhancing Decoupling by Intercalation of Molecules

Although the correlation between diffusion pathways and the enhanced decoupling of graphene is evident, it is, in a sense, counterproductive. There is interest in reducing the number of grain boundaries and nucleation sites and achieving ever larger continuous monolayer graphene single crystals [36], [158], [159]. So, there is an interest in decoupling them to enable the dry transfer. Achieving that goal entails enhancing the decoupling of the graphene even if the amount of nucleation sites and grain boundaries is limited.

Methods that facilitate the graphene-Cu decoupling can rely on enhancing the intercalation of the oxidative molecules between graphene and the Cu-substrate, which can be achieved by intercalating other molecules. This intercalation increases the distance between the Cu growth substrate and the graphene, decreasing the interactions that hold the two together. Decreased interaction between the graphene and the substrate could facilitate oxidation by immersion in DI water. Molecules such as H_2 can be intercalated [74] successfully and even induce the reduction of the Cu surface if sufficient thermal energy is supplied. As such, this process was tried as described in section 3.4.6. A preliminary test was conducted on an OxGr sample exposed to the atmosphere for over two weeks but not immersed in DI water. An annealing at 250° C under H_2 atmosphere was performed, followed by immersion in DI water for three consecutive days and a subsequent transfer onto SiO_2 using the PVA spin-coat method. Raman measurements were performed, and OM images were acquired prior to the annealing and after each step. The results are exposed in Figure 65. The measurements were done in random sites. Neither OM images nor Raman measurements show noticeable differences in the graphene quality before and after the H_2 annealing process (Figure 65b,d). The Raman spectra show a clear presence of the 2D peak, with varying relative heights to the G peak, which can be assigned to monolayer graphene, with a few exceptions.

Most importantly, the D peak appears to either be absent or have a smaller amplitude than the noise on both measurements, which indicates that the annealing process does not damage the graphene. After the immersion in DI water for three days, an interesting result was observed. The heterogeneity of behavior previously observed is attenuated, and different grains show similar colors, indicating similar oxidation levels of the Cu surface. Regions covered by multilayer graphene still presented seemingly no oxidation, which indicates that the H_2 intercalation did not facilitate their decoupling. The Raman

measurements taken at this step (Figure 65f) also showed an absence of the D peak, indicating that the oxidation of the Cu's interface with graphene did not induce defect formation. The transfer of this sample onto the SiO_2 substrate shows a graphene coverage that appears continuous except for multilayer regions, where only the borders were successfully transferred, although in some cases, complete regions were decoupled and transferred, as in section 6.2.1. Furthermore, by analyzing the corresponding Raman measurements, it can be seen that the D peak is now present, which is attributed to defects induced by the PVA spin-coat transfer process.

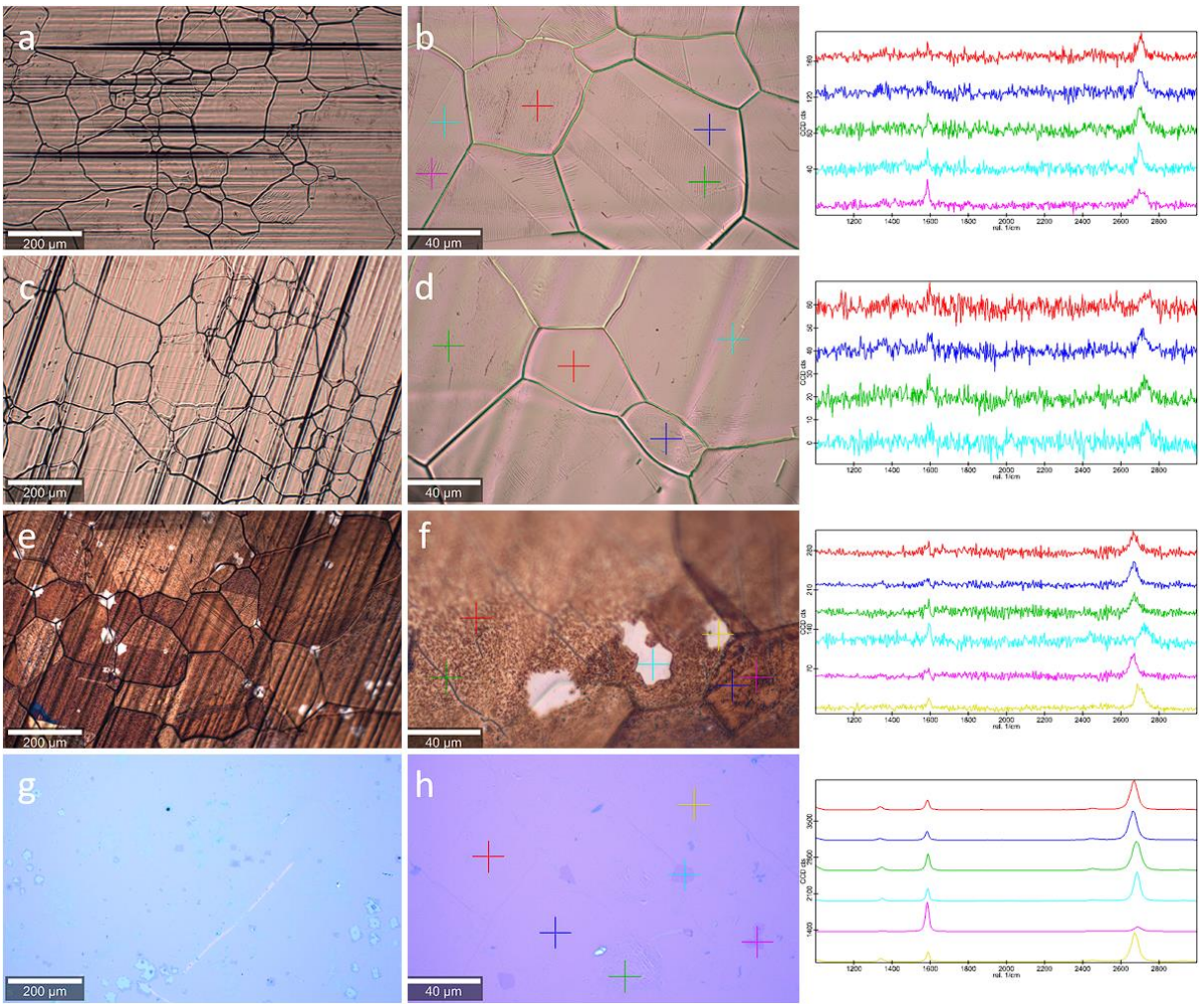


Figure 65 – Measurements between steps of the dry transfer with H_2 intercalation process. (a,b) Prior to annealing in H_2 atmosphere, (c,d) after the annealing, (e,f) after oxidation in DI water for 3 days, and (g,h) after transfer onto SiO_2 substrate. (b,d,f,h) correspond to zoomed regions and respective Raman measurements of the images in (a,c,e,g), respectively. Raman background signal of (b,d,f) was removed for clarity.

This experiment was tried a second time, but in this case, the H_2 annealing procedure took place immediately after the CVD growth of the OxGr sample. The sample was then immersed in DI water for 3 days and OM images were acquired, depicted in Figure 66a. The homogeneity of the oxidation was not

as evident as in Figure 65e, as different grains appeared to have very different behaviors, with some presenting almost no oxidation at all. Some non-oxidized regions also resembled the hexagonal shape of graphene crystals, typically observed in graphene multilayers grown around a seed layer, which can explain why the underlying Cu was not oxidized. This behavior shows that the natural intercalation of O_2 [46] under ambient atmosphere is crucial to achieving the complete oxidation and decoupling of graphene from the native substrate before any DI water immersion.

Additionally, certain regions among the annealed OxGr sample presented a homogeneous, complete oxidation. An example of such a region is depicted in Figure 66b, where no non-oxidized regions are visible, and color differences are subtle, indicating homogenous oxidation. Furthermore, no Cu grain boundaries are in sight, indicating that the region corresponds to a single grain of the underlying Cu substrate.

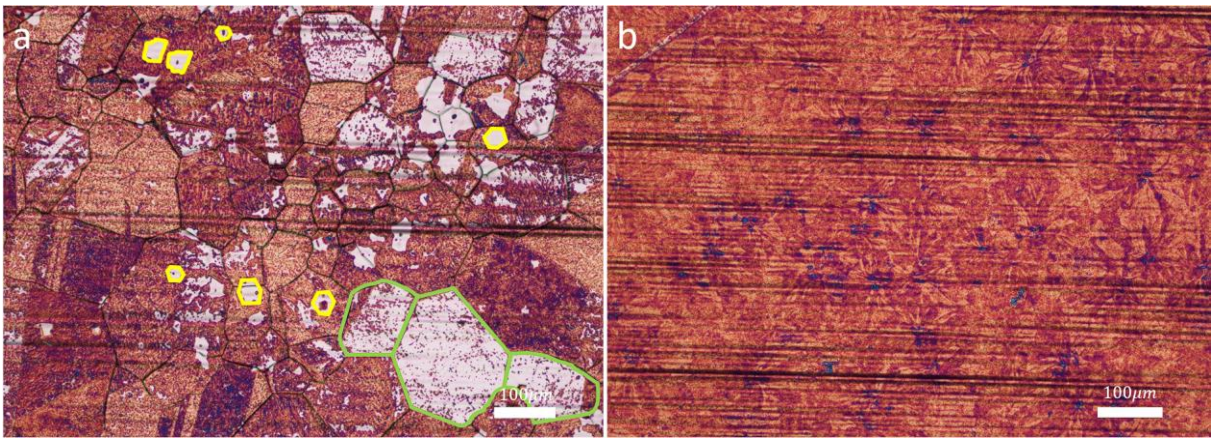


Figure 66 – OM images of oxidized Cu substrate after 3 days immersion in DI water without buffer time to promote O_2 intercalation in ambient atmosphere.
(a) Random region showing different behaviors towards oxidation of different grains. Yellow outlines mark non-oxidized regions presumably covered by multilayer graphene, with some presenting hexagonal shape. Green outlines mark grains where oxidation was inhibited. (b) Region of the same sample belonging to a large sized grain where oxidation appears to be homogeneous and complete, with no evidence of multilayer graphene regions inhibiting oxidation of the underlying substrate.

In summary, the H_2 annealing process appears beneficial for decoupling graphene when the OxGr sample is exposed to the ambient atmosphere for enough time. The annealing did not induce defects in the graphene and did not require any modification to the already established transfer process in this work.

6.2.3 The Role of the Underlying Copper Grain Orientation

The behavior of OxGr samples when decoupled via immersion in DI water or exposure to water vapor is very different from the noOxGr samples. By analyzing OM images of both samples, it is evident that the oxidation of the Cu surface interfacing graphene is different, which is also visible to the naked eye (Figure

67). The noOxGr samples achieved a relatively homogenous behavior of the Cu substrate throughout the whole sample, while the OxGr samples present very distinctive regions, like those depicted in Figure 64 and Figure 66. The type of region observed in Figure 66b, common to all OxGr samples, appears to correspond to copper grains where oxidation is homogeneous as they present an oxidated homogeneous color. These regions are visible to the naked eye, as they are associated with larger Cu grains than the average (Figure 67b) and get a distinctive orange tint.

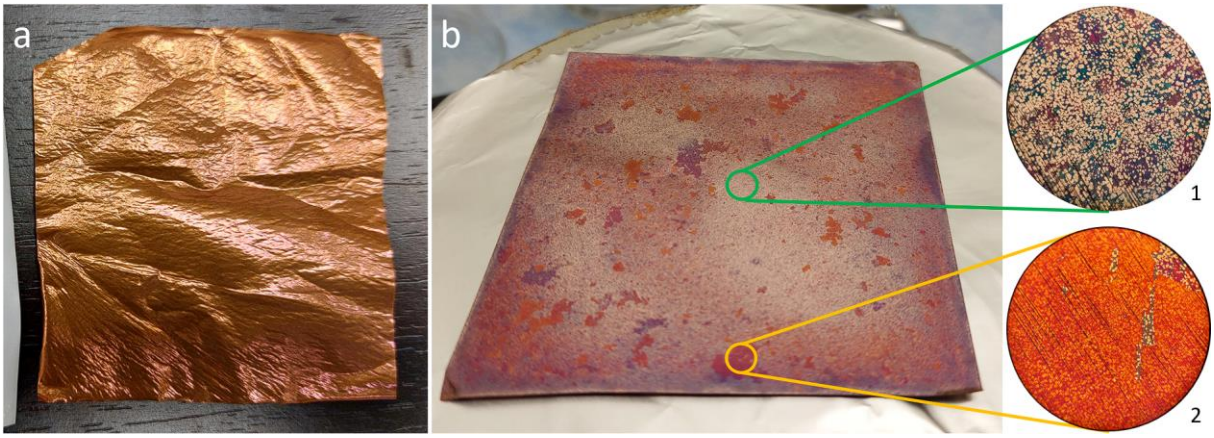


Figure 67 – Comparison of behavior of noOxGr and OxGr samples towards oxidation seen through the naked eye. (a) Homogeneous ppearance of a noOxGr sample after oxidation in DI water for 7 days. (b) Appearance of OxGr sample after oxidation in DI water for 3 days. Distinct regions are observable, with emphasis on orange-tinted large spots. The insets denote a random region, with oxidation largely inhibited by multilayer graphene regions and a substrate color ranging from red, to green, and blue (1), and a region of homogenous oxidation corresponding to an orange grain (2). The diameter of the insets corresponds to approximately 1 mm.

The interest in these regions comes not only from the fact that their oxidation was apparently facilitated but also from the fact that they appeared to be more efficient at decoupling monolayer and multilayer regions of graphene in OxGr samples. For example, in Figure 67b, various regions are spread throughout the OxGr sample, showing a different texture. By inspection under the OM, it is evident that the sample is covered in multilayer graphene regions in the shape of small crystals (10-20 μm). The underlying substrate does not get oxidized in general (Figure 67b.1), except if these multilayer regions are located in the orange-colored grains (Figure 67b.2). This effect can also be observed in Figure 68, where an OxGr sample is depicted after three days of immersion in DI water. The grain corresponding to the homogeneous orange region presented a completely oxidized surface. Contrastingly, neighboring grains show very bright regions with no apparent oxidation of the underlying substrate. The non-oxidized regions are covered with multilayer graphene, demonstrated by analyzing the Raman measurements (Figure 68b). However, in Figure 71c, multilayer graphene Raman signals are also present, although the

underlying substrate got successfully oxidized, further confirming oxidation on the homogeneously colored orange grain was facilitated.

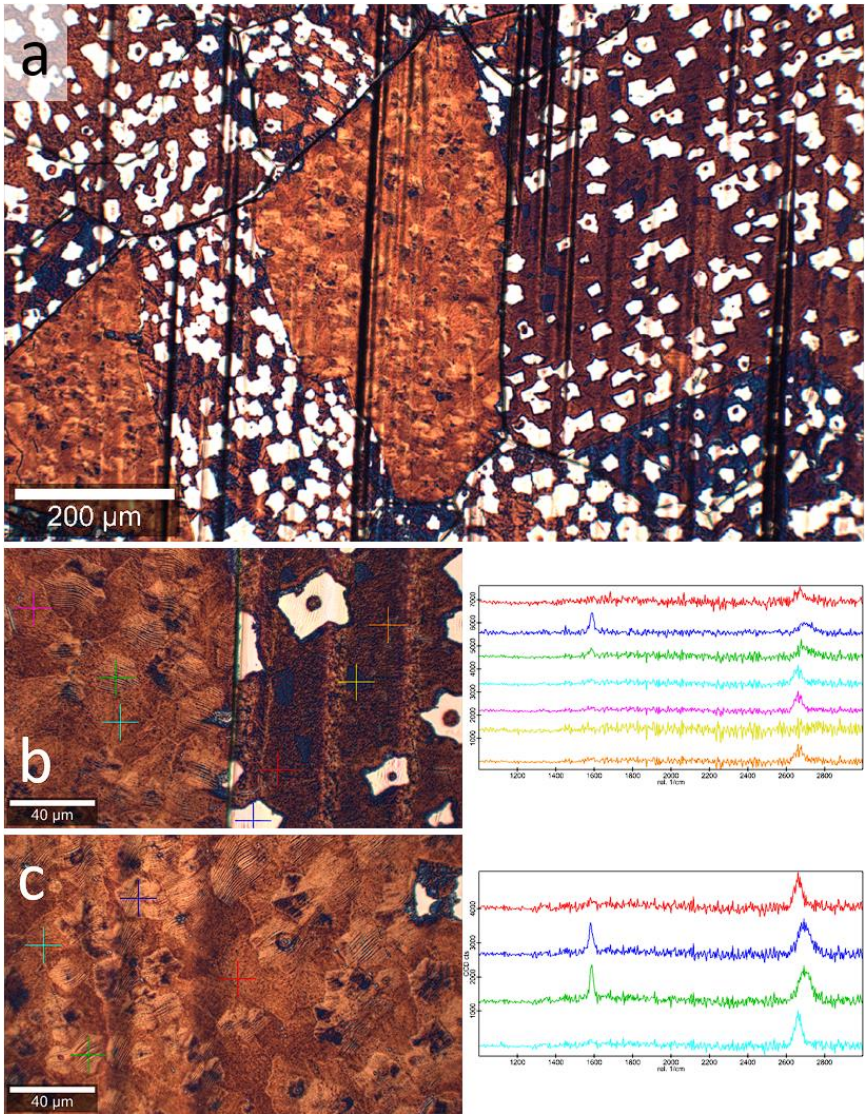


Figure 68 – Different oxidative behavior of different grains in OxGr samples with respect to multilayer graphene. (a) OM image showing a region with two orange grains with apparent complete oxidation of the substrate surrounded by grains with various non-oxidized regions shaped as graphene flakes, signaling multilayer regions. (b) Zoomed OM image and corresponding Raman measurements of a boundary of the orange grain. Dark blue cross denotes a spot where the substrate did not get oxidize and multilayer graphene presence is observed. (c) Zoomed OM image and corresponding Raman measurements of an interior area of the orange grain. Instances of multilayer graphene regions (dark blue and green) Raman spectra are acquired in lighter-colored regions of the orange grain. This entails that although the multilayer region also was oxidized, the oxidation occurred more softly.

These similarly colored and behaving grains in Figure 64, Figure 66b and Figure 68c showed greater oxidation of the Cu growth substrate and, thus, should also have better decoupling performances. Interesting results were observed by tracking the position of the graphene overlying these regions during

the dry transfer. Figure 69 displays a broader image of the regions in Figure 64a. It becomes evident how the graphene in the region delimited by the Cu grain transferred more completely, showing a better coverage of the SiO_2 substrate than on the surrounding Cu grains.

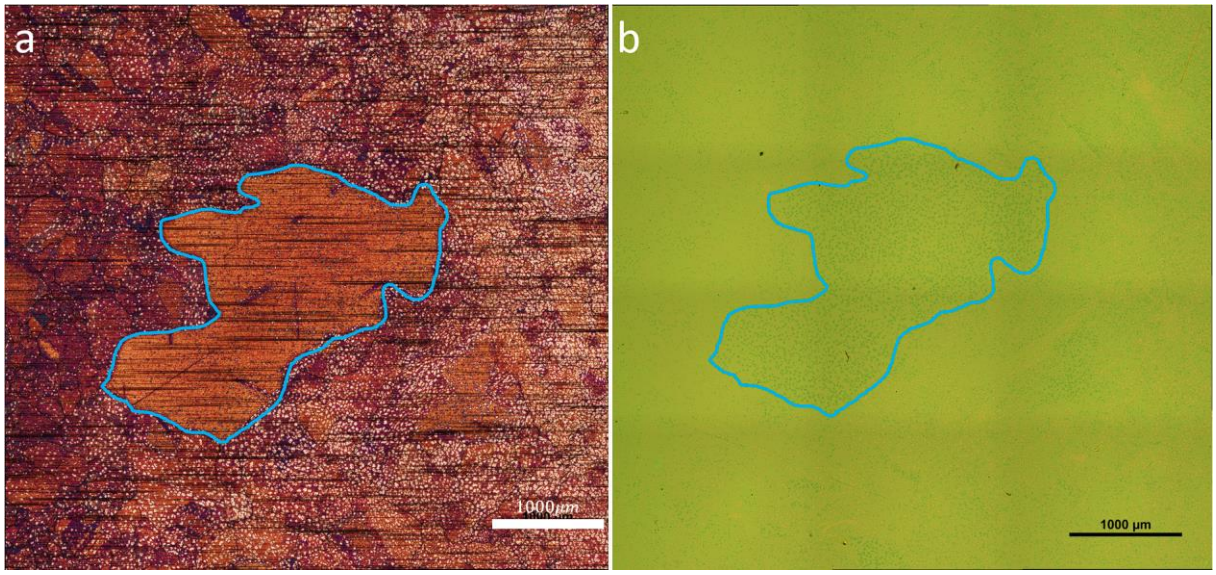


Figure 69 – Stitched OM images of the Cu substrate and corresponding dry transferred graphene onto SiO2. (a) OM image of the oxidized Cu growth substrate, with highlight in blue of the outline of a homogeneously colored orange grain. (b) Corresponding graphene transferred onto SiO_2 substrate where an area with a more complete coverage can be assigned to the grain in (a), as it possesses the same shape. The grid like pattern is an artifact of the stitching process of the multiple images taken under the OM.

The enhanced oxidation of the substrate and decoupling of graphene appeared tightly correlated with the grains of the Cu substrate. A correlation between the crystallographic orientation of the underlying Cu and the decoupling was investigated by acquiring XRD PF measurements. These were performed on the homogeneously-colored orange grains, and two in random regions (Figure 72 and Figure 73), originating from the same OxGr sample (Figure 67b). The sample first underwent decoupling by immersion in DI water for over a week, followed by a lamination transfer process to remove the graphene. The Cu substrate was then cut into four pieces and individually laminated to improve flatness, prior to the XRD PF measurements. Samples A and B possessed large orange grains up to 3 mm (Figure 72), while samples C and D showed many different grains spread through their area (Figure 73).

The XRD measurements are possible due to the existence of a periodic arrangement of atoms in crystaline materials [160], such as in Cu. These periodic arrangements form different planes of atoms with different directions and different spacings for each plane. X-Ray radiation can diffract off of these planes and

interact constructively depending on the used wavelength, λ, angle of incidence with the plane, θ, and spacing of the planes, d, as expressed in Equation (4), Bragg's law, where n is an integer.

$$n\lambda = 2d\sin(\theta) \qquad \text{Equation (4)}$$

T2T measurements are limited to detecting crytallographic planes that are parallel to the sample normal, which can allow to quantify the fraction of Cu crystallites with, for example, (111) or (100) growing orientations. In polycrystaline materials, different grains can show different crystal facets at the surface, which can be difficult to detect or quantify if their facets parallel to the surface correspond to a high index plane with a weak diffraction signal. In PF measurements, one sets the θ and 2θ angles to a detectable peak corresponding to a crystal plane. This plane exists in every grain, although more commonly than not not parallel to the surface. The grain can be detected if one rotates the sample in such a way that the incident and diffracted beam angles to the the plane's normal are simetric and the Bragg's law can be satisfied (Figure 70).

In the present work's measurements, the PFs were measured to qualitatively assess the composition of the Cu sample's crystallographic orientation. For such, the X-Ray source's beam collimator was set to a value granting that the whole sample would be hit with radiation and every grain would be contributing to the measured intensity at all times. Given unavailability of appropriate software during the work, standard data correction treatment was not performed [160].

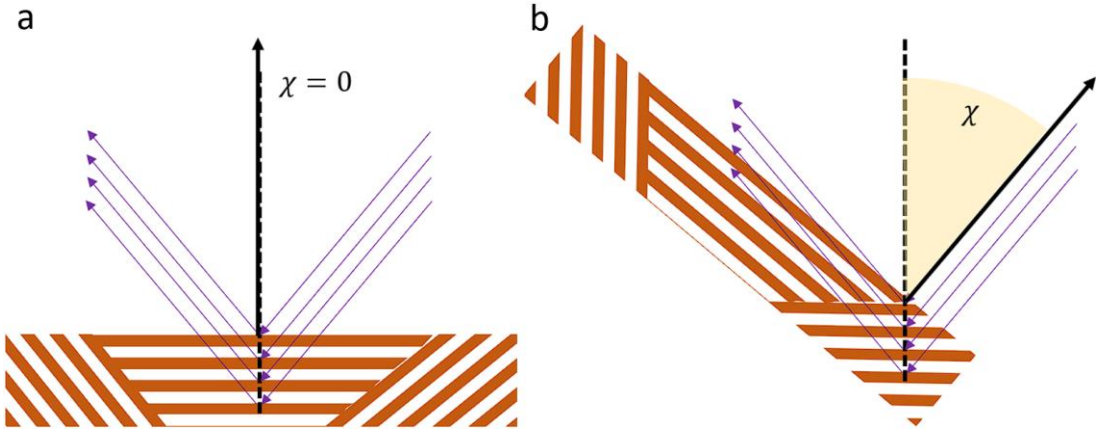


Figure 70 – Schematic of X-Ray radiation reflection off of a given group of crystal planes. In (a), with $\chi = 0$ a given grain contributes to the reflection for the fixated θ and 2θ parameters, and its neighbors do not, as their crystallographic orientation differs. Nevertheless, in (b), after adequate rotation in χ, one of the neighboring grains has the correct planes oriented in relation to the X-Ray beam and contribute to reflection. From here, one can extrapolate the plane family that is present at the sample's surface.

To then interpret the acquired pole figures, the theoretical (111) PF of a face centered cubic (FCC), like Cu, single crystal was computed (Figure 71c) utilizing a custom Python script. It was computed by supposing that an FCC single crystal stands in a reference frame such that (100), (010), and (001)

planes' normal vectors align with the x, y and z axis, respectively (Figure 71a). A rotation M was defined such that after being applied to the initial reference frame, the (01-1), (-211), and (111) plane's normal vectors represent the unit vectors of the new reference frame, the chosen pole's ((111) in this case) reference frame. It is represented as follows:

$$M = \begin{bmatrix} 0 & -2/\sqrt{6} & 1/\sqrt{3} \\ 1/\sqrt{2} & 1/\sqrt{6} & 1/\sqrt{3} \\ -1/\sqrt{2} & 1/\sqrt{6} & 1/\sqrt{3} \end{bmatrix}$$

Thus, M denoted the transformation from the sample's reference frame onto the pole's reference frame. By applying the inverse transformation M^{-1}, one computed the coordinates of a given plane's normal into the sample's reference frame. For example, applying M^{-1} to the plane's normal of (111) brings it to be parallel with the z axis unit vector. This can be thought of as rotating the crystal in such a way that the (111) plane is parallel with the equatorial plane of the unit sphere (Figure 71c). Upon projection onto the equatorial plane of the unit sphere, a point arises at (0,0), as expected in a PF of (111) orientation, meaning that a high intensity point should be measured when the setup is placed at the correct θ and 2θ for the (111) associated peak, and both φ and χ are set to 0, in the presence of a (111) crystal facet. By repeating this procedure of bringing a pole to the sample's reference frame utilizing the same M^{-1} matrix (or in other words, multiplying M^{-1} by the unit vector corresponding to a given plane), one can then stereographically project different plane's normals to obtain the theoretical (111) PF for a single crystal with a given crystallographic orientation. It is also noteworthy that given the symmetry of the Cu's FCC crystal lattice, the presence of a facet implies the existence of planes that belong to the same family. For example, the <100> index family possesses 6 different directions ([100],[010],[001],[-100],[0-10],[00-1]). Nevertheless, as angles $\chi > 90°$ would require transmission mode, χ was limited to 85° and one could only detect intensity peaks that would be projected from the north hemisphere of the unit sphere. For example, in the <111> index family there are 8 different directions, but only 4 can be detected when χ scan is limited to the north hemisphere ([111],[-111],[1-11],[11-1]). So, only poles that are placed in the north hemisphere of the unit sphere after rotation by M^{-1} matrix could be detected in the utilized setup. Furthermore, the polar projections of each plane direction in Figure 71c cannot be directly correlated to the obtained intensity peaks in PFs, but the relative position of the peaks of each family to the (111) direction can. For example, if when measuring a (111) PF one detects a peak at $\chi \approx 35°$, the instensity corresponds to the beam being correctly aligned in relation to a plane of the <111> family, which can be though of as rotating the crystal in Figure 71b to a point where the angle between the (111)

plane normal and the z axis is around $35°$, implying (by observation of Figure 71c) that the a plane of the <110> family is parallel to the surface of the sample.

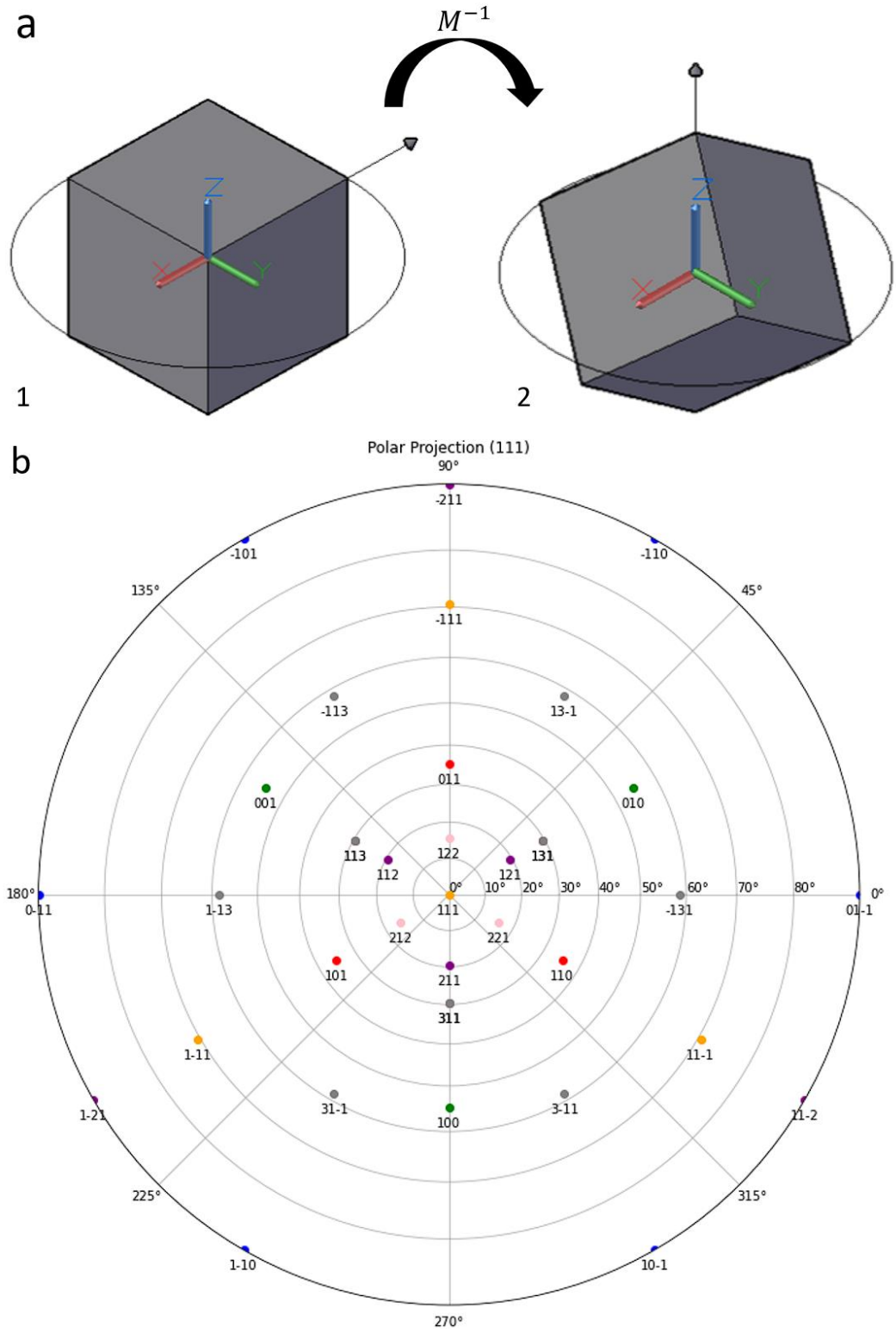


Figure 71 – Conceptual representation of a pole and PF.
(a) Representation of a cubic crystal in a reference frame before (1), and after (2) applying the M^{-1} rotation. The intersection of the unit sphere with the equatorial plane and a vector denoting the direction of the (111) plane are also represented. In (1) the (111) plane normal is unaltered, but in (2) it aligns itself with the z axis. (b)

Computed stereographic projection of several plane families, identified by different colors, present in the north hemisphere after rotation by the M^{-1} matrix.

After measurements, the PFs of samples A and B show a narrow distribution of high-intensity points (Figure 72), while samples C and D present a wider distribution (Figure 73). It means that samples C and D possess more Cu grains with a higher distribution of orientations, as expected from analyzing the OM images. Furthermore, a feature common to both C and D samples is that their PF resembles the shape of the PF of the Cu substrate prior to any CVD growth (Figure 73E) or, in other words, prior to the recrystallization of the Cu substrate that occurs at the growth temperature (1040 °C). One can conclude that while in samples C and D the Cu preserved the crystallographic orientation exhibited before the CVD process, the pre-CVD crystallographic memory was lost in samples A and B. Figure 72 shows that samples A and B suffered a more intense recrystallization with barely any resemblance to the original Cu substrate's PF.

The distribution of higher intensity points of samples A and B can be used to determine the grain orientations of the bigger grains. In the case of sample A, the observed pattern belongs to a (111) oriented Cu grain as the highest intensity point corresponds to the center of the PF, and three other high-intensity points are located at $\chi \approx 70°$ and spaced by $\Delta\varphi \approx 120°$ (see Figure 71c). In sample B, the center point also corresponds to the highest intensity point, but the other three high-intensity peaks expected to be observed near $\chi \approx 70°$ in the case of (111) oriented grains are more challenging to observe. Nevertheless, the points marked with dashed yellow circles could be associated with these three high-intensity points, assuming their position was skewed due to a non-flat sample. Furthermore, sample B is significantly larger than sample A, which can intensify these effects if the sample is non-flat. Sample B has more high-intensity points spread in the PF that can be associated with a more significant number of randomly oriented smaller grains than in sample A. It can be concluded that sample A is more textured in (111) than sample B is.

Regarding samples C and D, the OM images show that sample C possesses more orange-colored grains than sample D, and by the previous analysis, should also present significantly higher intensity points near the center and $\chi \approx 70°$ regions of the PF, corresponding to (111) grains. By analyzing the PFs of these two samples, it is not clear that sample C possesses more (111) oriented grains than sample D, although an argument could be made by noticing that close to the $\chi \approx 70°$ regions, sample C shows a greater density of high-intensity points than sample D.

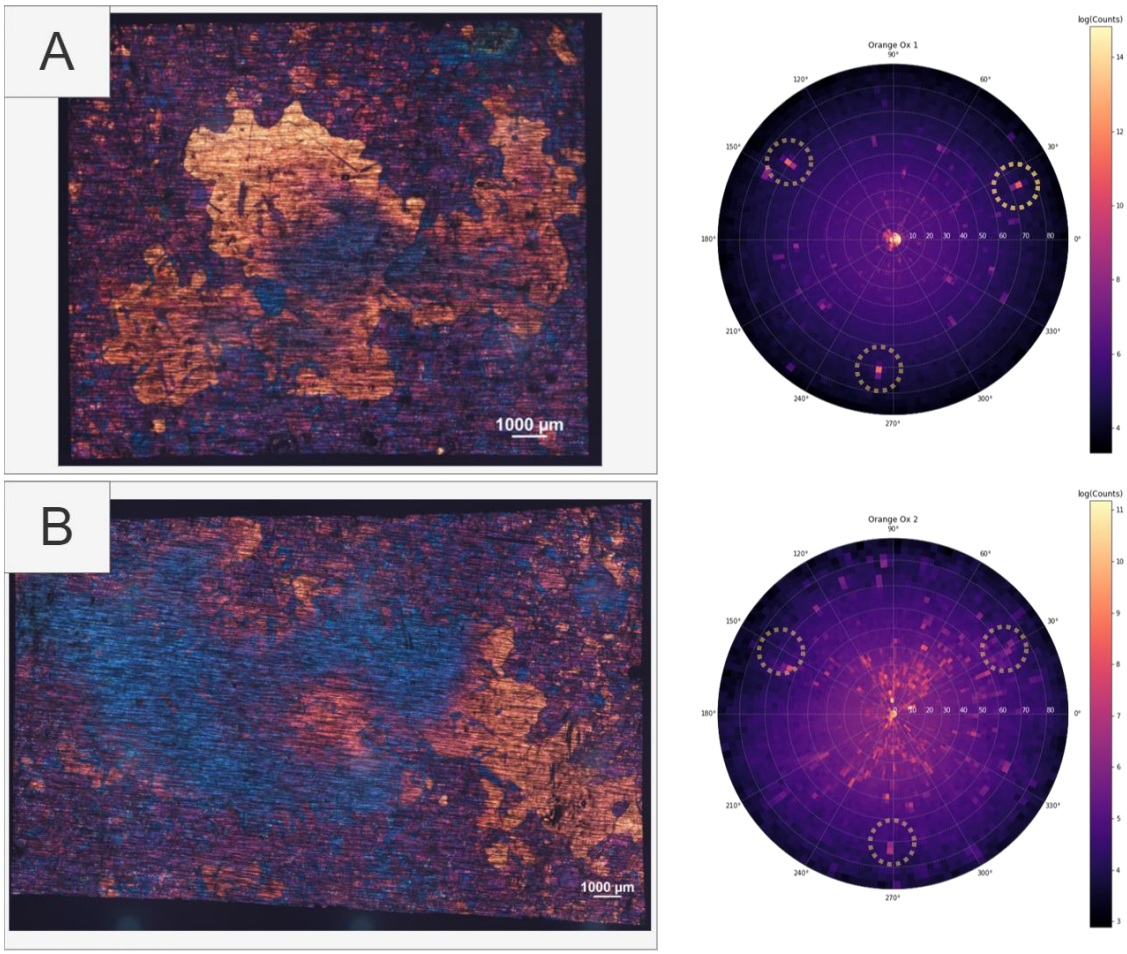


Figure 72 – PF of the samples A and B (right), and corresponding OM images (left), corresponding to random regions of an oxidized Cu substrate (C,D) and the Cu substrate prior to any CVD growth of graphene (E). The PF of (E) closely resembles that of rolled pure copper [161]. The PFs of (C) and (D) show a sparse distribution of points, slightly following the tendencies of PF (E).

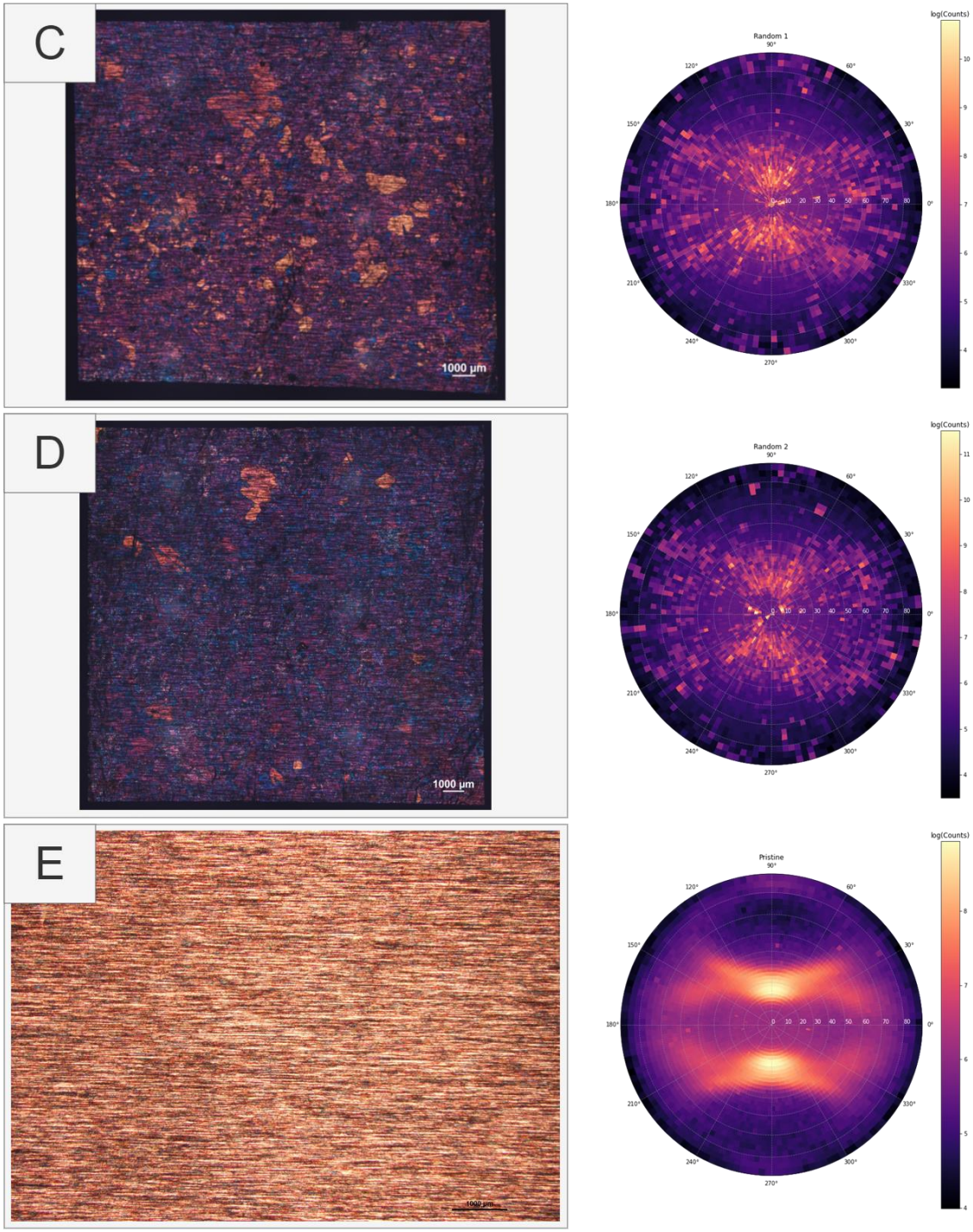


Figure 73 - PF of the samples C and D (right), and corresponding OM images (left), corresponding to random regions of an oxidized Cu substrate. Sample E corresponds to the Cu substrate prior to any CVD growth of graphene. The PF of (E) closely resembles that of rolled pure copper [161]. The PFs of (C) and (D) show a sparse distribution of points, slightly following the tendencies of PF (E).

These results seem to prove that the regions where decoupling of graphene is best achieved correspond to Cu grains oriented in the (111) orientation. The formation of large (111) oriented grains via slow cooling of the Cu growth substrate after the CVD growth of graphene has been previously demonstrated [46], which goes in accordance with the results obtained in this work, as the cooling stage of the CVD growth

of the graphene samples used in this work is slow, taking close to 6 hours. In regard to the oxidation of the interface between graphene and the underlying Cu substrate, the results in this thesis are contradictory to what is typically observed in the literature. One study [74] claims that (111) orientations of Cu oxidize via strong contributions of graphene wrinkles, which are typically more reactive and result in non-homogenous oxidation. Another, more recent study [156], claims (111) oriented Cu grains demonstrate poor homogeneity of oxidation and low transfer yield and points higher index orientations such as (168) at a higher level in relation to its desirability for the dry transfer of graphene. On the other hand, a different study [73], points that (111) Cu orientations coated in monolayer graphene are more reactive than, for example, regions of (100) oriented Cu. In this same study, it is also shown that Cu regions covered in bilayer graphene are a lot less reactive than monolayer graphene covered ones, which was also verified in this work. Unfortunately, no correlation is explored between the bilayer graphene decoupling and the corresponding orientation of the underlying substrate in [73] – which was observed in the present work.

6.3 Concluding Remarks on Graphene Dry Transfer

The graphene dry transfer proved to be a complex process with various nuances that hinder or promote a successful transfer.

How the PVA is applied is critical. The lamination process promotes bubble formation, which hinders good coverage of the target substrate, a problem absent when the polymer is spin-coated. Nevertheless, the spin-coating transfer process poses a higher risk of inducing small-sized graphene defects. The conclusion is that the PVA application should be made by spin-coating, but the peeling of the PVA should have the same stability as with the laminated polymer. A hybrid approach entailing PVA spin-coating followed by lamination with a thicker PVA foil could provide the benefits of both approaches without the drawbacks.

Regarding the decoupling processes, the roles of the existing nucleation sites and grain boundaries proved crucial in making the transfer of graphene more efficient, with the noOxGr samples being more straightforward to decouple than the OxGr ones. Furthermore, the OxGr samples entailed a heterogeneous behavior towards the oxidation. This inconsistent behavior led to trying to promote intercalation of H_2 molecules on OxGr samples, showing positive results.

The different behaviors of the Cu substrate on OxGr led to the study of the grains that would promote efficient graphene decoupling by homogenous substrate oxidation, even in hard-to-decouple multilayer

graphene regions. These grains were found to have a crystallographic orientation (111), which contradicts results seen in the literature, proving to be an exciting result for the overall understanding of the decoupling process of graphene and its interaction with the underlying substrate.

Overall, the dry transfer process was demonstrated and highlighted different aspects worth investigating. Good coverage of the target substrates was achieved, and underlying mechanisms enabling the transfer were understood, opening way for further development and enhancement of the dry transfer process. By incorporating this transfer methods in the projected neurochemical graphene-based sensor, PMMA residues can be avoided, and the associated manufacturing costs significantly lowered. Furthermore, a possible future integration with roll-to-roll technology could enable the large-scale fabrication of such devices, making them more affordable and available.

7. Conclusions and Future Work

The work done in this dissertation project was extensive and covered multiple areas of research. The development of a graphene field-effect transistor fabrication process was investigated. Simultaneously, a method for integration of flip chip micron-sized light emitting diodes in the same substrate was established. Finally, a scalable and affordable method for the transfer of graphene was explored. The conjoined efforts in all these areas aimed towards the development of a flexible device based on graphene transistors for the detection of neurotransmitters ex vivo.

This work allowed for the development, testing, optimization, and validation of various parts of the fabrication process of graphene transistor in polyimide. The device layout was established, and the use of polyimide substrate and gold conducting tracks were validated. Furthermore, the graphene wet transfer was successfully tested, although problems with residues arose in the device wafer. Other critical points that need further optimization in next iterations of the device were highlighted. Future work regarding this device development entails the correction of the edges obtained in the Au tracks and completion of the projected fabrication process. Possibly, the testing of different deposition methods on top of the graphene would also be beneficial, such as evaporation.

Concerning the micron-sized light emitting diodes mounting, the stamping and pick-and-place approach were very successful, and their integration with the designed fabrication process of the wafer was accomplished. The developed approaches proved adequate, conferring low complexity and reliable mounting with the addition of a transparent epoxy. As the polyimide release process proved to be destructive for the micron-sized light emitting diodes, testing the mounting in released polyimide substrates would be of great importance in the future. Furthermore, the assessment of the endurance of the achieved connections and the micron-sized light emitting diodes in a biological environment would be crucial, to validate the reliability of the approach for in-vivo applications, as high humidity levels and deformations are unavoidable.

Finally, the dry transfer of graphene was explored in this work with satisfying results. The importance of different approaches for transferring graphene to the PVA support polymer and the crucial role of decoupling the graphene from the Cu native substrate were demonstrated. The application of PVA via lamination and spin-coating were assessed, highlighting benefits and drawbacks, and emphasizing the need for a hybrid method to transfer the graphene. Furthermore, the importance of the crystallographic orientation regarding the decoupling was demonstrated, finding that (111) orientations of Cu promote the

decoupling of monolayer and multilayer graphene. These findings open the way for exploring graphene growing on top of (111) substrates via controlled cooling to enable efficient dry transfer of graphene, and even pave the way for application in roll-to-roll technologies.

Overall, the three different areas studied here could converge towards fabricating a GFET-based neurotransmitter sensor, with integrated μLEDs mounted via stamping and pick-and-place methods and utilizing dry transferred graphene, as all processes are compatible. The well-established micro-fabrication technologies would benefit from the practical mounting technique of micron-sized light emitting diodes and the affordability and cleanliness of the dry transfer of graphene, enabling the development of an inexpensive, effective, and reliable device.

REFERENCES

[1] F. A. C. Azevedo *et al.*, "Equal numbers of neuronal and nonneuronal cells make the human brain an isometrically scaled-up primate brain," *J Comp Neurol*, vol. 513, no. 5, pp. 532–541, Apr. 2009, doi: 10.1002/cne.21974.

[2] C. S. von Bartheld, J. Bahney, and S. Herculano-Houzel, "The search for true numbers of neurons and glial cells in the human brain: A review of 150 years of cell counting," *Journal of Comparative Neurology*, vol. 524, no. 18, pp. 3865–3895, Dec. 2016, doi: 10.1002/cne.24040.

[3] W. Muangpaisan, A. Mathews Mbbs, H. Hori, and D. Seidel Mphil, "A Systematic Review of the Worldwide Prevalence and Incidence of Parkinson's Disease," 2011. [Online]. Available: http://www.mat.or.th/journal

[4] E. R. Dorsey and B. R. Bloem, "The Parkinson Pandemic—A Call to Action," *JAMA Neurol*, vol. 75, no. 1, p. 9, Jan. 2018, doi: 10.1001/jamaneurol.2017.3299.

[5] R. Mayeux and Y. Stern, "Epidemiology of Alzheimer disease," *Cold Spring Harb Perspect Med*, vol. 2, no. 8, 2012, doi: 10.1101/cshperspect.a006239.

[6] G. Buzsáki *et al.*, "Tools for probing local circuits: High-density silicon probes combined with optogenetics," *Neuron*, vol. 86, no. 1. Cell Press, pp. 92–105, Apr. 08, 2015. doi: 10.1016/j.neuron.2015.01.028.

[7] B. Ji *et al.*, "Flexible polyimide-based hybrid opto-electric neural interface with 16 channels of micro-LEDs and electrodes," *Microsyst Nanoeng*, vol. 4, no. 1, Dec. 2018, doi: 10.1038/s41378-018-0027-0.

[8] K. Y. Kwon, B. Sirowatka, A. Weber, and W. Li, "Opto-μECoG Array: A Hybrid Neural Interface With Transparent μECoG Electrode Array and Integrated LEDs for Optogenetics," *IEEE Trans Biomed Circuits Syst*, vol. 7, no. 5, pp. 593–600, Oct. 2013, doi: 10.1109/TBCAS.2013.2282318.

[9] D. Sahni *et al.*, "Biocompatibility of pristine graphene for neuronal interface: Laboratory investigation," *J Neurosurg Pediatr*, vol. 11, no. 5, pp. 575–583, May 2013, doi: 10.3171/2013.1.PEDS12374.

[10] M. Abrantes *et al.*, "Ultrasensitive dopamine detection with graphene aptasensor multitransistor arrays," *J Nanobiotechnology*, vol. 20, no. 1, p. 495, Nov. 2022, doi: 10.1186/s12951-022-01695-0.

[11] G. Wu *et al.*, "Implantable Aptamer-Graphene Microtransistors for Real-Time Monitoring of Neurochemical Release in Vivo," *Nano Lett*, 2022, doi: 10.1021/acs.nanolett.2c00289.

[12] J. Kang, D. Shin, S. Bae, and B. H. Hong, "Graphene transfer: Key for applications," *Nanoscale*, vol. 4, no. 18. Royal Society of Chemistry, pp. 5527–5537, Sep. 21, 2012. doi: 10.1039/c2nr31317k.

[13] S. Ullah *et al.*, "Graphene transfer methods: A review," *Nano Research*, vol. 14, no. 11. Tsinghua University, pp. 3756–3772, Nov. 01, 2021. doi: 10.1007/s12274-021-3345-8.

[14] A. Shivayogimath *et al.*, "Do-It-Yourself Transfer of Large-Area Graphene Using an Office Laminator and Water," *Chemistry of Materials*, vol. 31, no. 7, pp. 2328–2336, Apr. 2019, doi: 10.1021/acs.chemmater.8b04196.

[15] N. Hong, D. Kireev, Q. Zhao, D. Chen, D. Akinwande, and W. Li, "Roll-to-Roll Dry Transfer of Large-Scale Graphene," *Advanced Materials*, vol. 34, no. 3, Jan. 2022, doi: 10.1002/adma.202106615.

[16] C. J. Shearer, A. D. Slattery, A. J. Stapleton, J. G. Shapter, and C. T. Gibson, "Accurate thickness measurement of graphene," *Nanotechnology*, vol. 27, no. 12, Feb. 2016, doi: 10.1088/0957-4484/27/12/125704.

[17] M. Pozzo, D. Alfè, P. Lacovig, P. Hofmann, S. Lizzit, and A. Baraldi, "Thermal expansion of supported and freestanding graphene: Lattice constant versus interatomic distance," *Phys Rev Lett*, vol. 106, no. 13, Mar. 2011, doi: 10.1103/PhysRevLett.106.135501.

[18] J. Yang, Y. Yuan, and G. Chen, "First–principles study of potassium adsorption and diffusion on graphene," *Mol Phys*, vol. 118, no. 1, Jan. 2020, doi: 10.1080/00268976.2019.1581291.

[19] F. D. M. Haldane, "Model for a Quantum Hall Eff'ect without Landau Levels: Condensed-Matter Realization of the 'Parity Anomaly.'"

[20] A. K. Geim and K. S. Novoselov, "The rise of graphene." [Online]. Available: www.nature.com/naturematerials

[21] A. H. Castro Neto, F. Guinea, N. M. R. Peres, K. S. Novoselov, and A. K. Geim, "The electronic properties of graphene," *Rev Mod Phys*, vol. 81, no. 1, pp. 109–162, Jan. 2009, doi: 10.1103/RevModPhys.81.109.

[22] L. A. Falkovsky, "Optical properties of graphene," *J Phys Conf Ser*, vol. 129, 2008, doi: 10.1088/1742-6596/129/1/012004.

[23] S. E. Zhu, S. Yuan, and G. C. A. M. Janssen, "Optical transmittance of multilayer graphene," *EPL*, vol. 108, no. 1, Oct. 2014, doi: 10.1209/0295-5075/108/17007.

[24] R. R. Nair *et al.*, "Fine structure constant defines visual transparency of graphene," *Science (1979)*, vol. 320, no. 5881, p. 1308, Jun. 2008, doi: 10.1126/science.1156965.

[25] G. Yang, L. Li, W. B. Lee, and M. C. Ng, "Structure of graphene and its disorders: a review," *Science and Technology of Advanced Materials*, vol. 19, no. 1. Taylor and Francis Ltd., pp. 613–648, Dec. 31, 2018. doi: 10.1080/14686996.2018.1494493.

[26] Z. H. Ni *et al.*, "Graphene thickness determination using reflection and contrast spectroscopy," *Nano Lett*, vol. 7, no. 9, pp. 2758–2763, Sep. 2007, doi: 10.1021/nl071254m.

[27] N. O. Weiss *et al.*, "Graphene: An emerging electronic material," *Advanced Materials*, vol. 24, no. 43. pp. 5782–5825, Nov. 14, 2012. doi: 10.1002/adma.201201482.

[28] K. S. Novoselov *et al.*, "Electric field in atomically thin carbon films," *Science (1979)*, vol. 306, no. 5696, pp. 666–669, Oct. 2004, doi: 10.1126/science.1102896.

[29] N. A. A. Ghany, S. A. Elsherif, and H. T. Handal, "Revolution of Graphene for different applications: State-of-the-art," *Surfaces and Interfaces*, vol. 9. Elsevier B.V., pp. 93–106, Dec. 01, 2017. doi: 10.1016/j.surfin.2017.08.004.

[30] K. Parvez *et al.*, "Exfoliation of graphite into graphene in aqueous solutions of inorganic salts," *J Am Chem Soc*, vol. 136, no. 16, pp. 6083–6091, Apr. 2014, doi: 10.1021/ja5017156.

[31] S. Park and R. S. Ruoff, "Chemical methods for the production of graphenes," *Nat Nanotechnol*, vol. 4, no. 4, pp. 217–224, 2009, doi: 10.1038/nnano.2009.58.

[32] H. Huang, S. Chen, A. T. S. Wee, and W. Chen, "Epitaxial growth of graphene on silicon carbide (SiC)," in *Graphene: Properties, Preparation, Characterisation and Devices*, Elsevier Ltd., 2014, pp. 3–26. doi: 10.1533/9780857099334.1.3.

[33] N. Mishra, J. Boeckl, N. Motta, and F. Iacopi, "Graphene growth on silicon carbide: A review," *Physica Status Solidi (A) Applications and Materials Science*, vol. 213, no. 9. Wiley-VCH Verlag, pp. 2277–2289, Sep. 01, 2016. doi: 10.1002/pssa.201600091.

[34] C. Riedl, C. Coletti, and U. Starke, "Structural and electronic properties of epitaxial Graphene on SiC(0001): A review of growth, characterization, transfer doping and hydrogen intercalation," *J Phys D Appl Phys*, vol. 43, no. 37, Sep. 2010, doi: 10.1088/0022-3727/43/37/374009.

[35] X. Chen, L. Zhang, and S. Chen, "Large area CVD growth of graphene," *Synth Met*, vol. 210, pp. 95–108, Dec. 2015, doi: 10.1016/j.synthmet.2015.07.005.

[36] H. S. Jang *et al.*, "Toward Scalable Growth for Single-Crystal Graphene on Polycrystalline Metal Foil," *ACS Nano*, vol. 14, no. 3, pp. 3141–3149, Mar. 2020, doi: 10.1021/acsnano.9b08305.

[37] Y. Zhang *et al.*, "Comparison of graphene growth on single-crystalline and polycrystalline Ni by chemical vapor deposition," *Journal of Physical Chemistry Letters*, vol. 1, no. 20, pp. 3101–3107, Oct. 2010, doi: 10.1021/jz1011466.

[38] X. Li *et al.*, "Large-area synthesis of high-quality and uniform graphene films on copper foils," *Science (1979)*, vol. 324, no. 5932, pp. 1312–1314, 2009, doi: 10.1126/science.1171245.

[39] W. Yang *et al.*, "Epitaxial growth of single-domain graphene on hexagonal boron nitride," *Nat Mater*, vol. 12, no. 9, pp. 792–797, 2013, doi: 10.1038/nmat3695.

[40] S. Xu, L. Zhang, B. Wang, and R. S. Ruoff, "Chemical vapor deposition of graphene on thin-metal films," *Cell Reports Physical Science*, vol. 2, no. 3. Cell Press, Mar. 24, 2021. doi: 10.1016/j.xcrp.2021.100372.

[41] L. Lin, B. Deng, J. Sun, H. Peng, and Z. Liu, "Bridging the Gap between Reality and Ideal in Chemical Vapor Deposition Growth of Graphene," *Chemical Reviews*, vol. 118, no. 18. American Chemical Society, pp. 9281–9343, Sep. 26, 2018. doi: 10.1021/acs.chemrev.8b00325.

[42] B. Luo, P. R. Whelan, A. Shivayogimath, D. M. A. Mackenzie, P. Bøggild, and T. J. Booth, "Copper Oxidation through Nucleation Sites of Chemical Vapor Deposited Graphene," *Chemistry of Materials*, vol. 28, no. 11, pp. 3789–3795, Jun. 2016, doi: 10.1021/acs.chemmater.6b00752.

[43] J. Kraus, M. Böbel, and S. Günther, "Suppressing graphene nucleation during CVD on polycrystalline Cu by controlling the carbon content of the support foils," *Carbon N Y*, vol. 96, pp. 153–165, Jan. 2016, doi: 10.1016/j.carbon.2015.09.048.

[44] P. Braeuninger-Weimer, B. Brennan, A. J. Pollard, and S. Hofmann, "Understanding and Controlling Cu-Catalyzed Graphene Nucleation: The Role of Impurities, Roughness, and Oxygen Scavenging," *Chemistry of Materials*, vol. 28, no. 24, pp. 8905–8915, Dec. 2016, doi: 10.1021/acs.chemmater.6b03241.

[45] J. D. Wood, S. W. Schmucker, A. S. Lyons, E. Pop, and J. W. Lyding, "Effects of polycrystalline Cu substrate on graphene growth by chemical vapor deposition," *Nano Lett*, vol. 11, no. 11, pp. 4547–4554, Nov. 2011, doi: 10.1021/nl201566c.

[46] A. Y. Lu *et al.*, "Decoupling of CVD graphene by controlled oxidation of recrystallized Cu," *RSC Adv*, vol. 2, no. 7, pp. 3008–3013, Apr. 2012, doi: 10.1039/c2ra01281b.

[47] Y. Han *et al.*, "Direct Growth of Highly Conductive Large-Area Stretchable Graphene," *Advanced Science*, vol. 8, no. 7, Apr. 2021, doi: 10.1002/advs.202003697.

[48] Y. Ueda, T. Maruyama, and S. Naritsuka, "Effect of Growth Pressure on Graphene Direct Growth on an A-Plane Sapphire Substrate: Implications for Graphene-Based Electronic Devices," *ACS Appl Nano Mater*, vol. 4, no. 1, pp. 343–351, Jan. 2021, doi: 10.1021/acsanm.0c02634.

[49] H. Wang and G. Yu, "Direct CVD Graphene Growth on Semiconductors and Dielectrics for Transfer-Free Device Fabrication," *Advanced Materials*, vol. 28, no. 25, pp. 4956–4975, Jul. 2016, doi: 10.1002/adma.201505123.

[50] Z. Chen, Y. Qi, X. Chen, Y. Zhang, and Z. Liu, "Direct CVD Growth of Graphene on Traditional Glass: Methods and Mechanisms," *Advanced Materials*, vol. 31, no. 9. Wiley-VCH Verlag, Mar. 01, 2019. doi: 10.1002/adma.201803639.

[51] P. D. Cabral *et al.*, "Clean-room lithographical processes for the fabrication of graphene biosensors," *Materials*, vol. 13, no. 24, pp. 1–23, Dec. 2020, doi: 10.3390/ma13245728.

[52] J. W. Suk *et al.*, "Enhancement of the electrical properties of graphene grown by chemical vapor deposition via controlling the effects of polymer residue," *Nano Lett*, vol. 13, no. 4, pp. 1462–1467, Apr. 2013, doi: 10.1021/nl304420b.

[53] S. J. Park, O. S. Kwon, S. H. Lee, H. S. Song, T. H. Park, and J. Jang, "Ultrasensitive flexible graphene based field-effect transistor (FET)-type bioelectronic nose," *Nano Lett*, vol. 12, no. 10, pp. 5082–5090, Oct. 2012, doi: 10.1021/nl301714x.

[54] W. Regan *et al.*, "A direct transfer of layer-area graphene," *Appl Phys Lett*, vol. 96, no. 11, 2010, doi: 10.1063/1.3337091.

[55] A. Ballesio *et al.*, "A novel hot embossing Graphene transfer process for flexible electronics," *Microelectron Eng*, vol. 209, pp. 16–19, Mar. 2019, doi: 10.1016/j.mee.2019.02.010.

[56] M. Kim *et al.*, "Direct transfer of Wafer-scale graphene films," *2d Mater*, vol. 4, no. 3, Sep. 2017, doi: 10.1088/2053-1583/aa780d.

[57] L. P. Ma, S. Dong, H. M. Cheng, and W. Ren, "Breaking the Rate-Integrity Dilemma in Large-Area Bubbling Transfer of Graphene by Strain Engineering," *Adv Funct Mater*, vol. 31, no. 36, Sep. 2021, doi: 10.1002/adfm.202104228.

[58] Y. Wang *et al.*, "Electrochemical delamination of CVD-grown graphene film: Toward the recyclable use of copper catalyst," *ACS Nano*, vol. 5, no. 12, pp. 9927–9933, Dec. 2011, doi: 10.1021/nn203700w.

[59] L. Gao *et al.*, "Repeated growth and bubbling transfer of graphene with millimetre-size single-crystal grains using platinum," *Nat Commun*, vol. 3, 2012, doi: 10.1038/ncomms1702.

[60] K. Verguts, J. Coroa, C. Huyghebaert, S. De Gendt, and S. Brems, “Graphene delamination using ‘electrochemical methods’: An ion intercalation effect,” *Nanoscale*, vol. 10, no. 12, pp. 5515–5521, Mar. 2018, doi: 10.1039/c8nr00335a.

[61] S. J. Yang, S. Choi, F. O. Odongo Ngome, K. J. Kim, S. Y. Choi, and C. J. Kim, “All-Dry Transfer of Graphene Film by van der Waals Interactions,” *Nano Lett*, vol. 19, no. 6, pp. 3590–3596, Jun. 2019, doi: 10.1021/acs.nanolett.9b00555.

[62] J.-H. Lee *et al.*, “Wafer-Scale Growth of Single-Crystal Monolayer Graphene on Reusable Hydrogen-Terminated Germanium.” [Online]. Available: https://www.science.org

[63] I. Hamada and M. Otani, “Comparative van der Waals density-functional study of graphene on metal surfaces,” *Phys Rev B Condens Matter Mater Phys*, vol. 82, no. 15, Oct. 2010, doi: 10.1103/PhysRevB.82.153412.

[64] H. Xin, R. Borduin, W. Jiang, K. M. Liechti, and W. Li, “Adhesion energy of as-grown graphene on copper foil with a blister test,” *Carbon N Y*, vol. 123, pp. 243–249, Oct. 2017, doi: 10.1016/j.carbon.2017.07.053.

[65] T. Yoon, W. C. Shin, T. Y. Kim, J. H. Mun, T. S. Kim, and B. J. Cho, “Direct measurement of adhesion energy of monolayer graphene as-grown on copper and its application to renewable transfer process,” *Nano Lett*, vol. 12, no. 3, pp. 1448–1452, Mar. 2012, doi: 10.1021/nl204123h.

[66] R. Zacharia, H. Ulbricht, and T. Hertel, “Interlayer cohesive energy of graphite from thermal desorption of polyaromatic hydrocarbons,” *Phys Rev B Condens Matter Mater Phys*, vol. 69, no. 15, Apr. 2004, doi: 10.1103/PhysRevB.69.155406.

[67] M. Marchena *et al.*, “Dry transfer of graphene to dielectrics and flexible substrates using polyimide as a transparent and stable intermediate layer,” *2d Mater*, vol. 5, no. 3, May 2018, doi: 10.1088/2053-1583/aac12d.

[68] M. Schriver, W. Regan, W. J. Gannett, A. M. Zaniewski, M. F. Crommie, and A. Zettl, “Graphene as a long-term metal oxidation barrier: Worse than nothing,” *ACS Nano*, vol. 7, no. 7, pp. 5763–5768, Jul. 2013, doi: 10.1021/nn4014356.

[69] R. Wu, L. Gan, X. Ou, Q. Zhang, and Z. Luo, “Detaching graphene from copper substrate by oxidation-assisted water intercalation,” *Carbon N Y*, vol. 98, pp. 138–143, Mar. 2016, doi: 10.1016/j.carbon.2015.11.002.

[70] D. Luo *et al.*, "Role of Graphene in Water-Assisted Oxidation of Copper in Relation to Dry Transfer of Graphene," *Chemistry of Materials*, vol. 29, no. 10, pp. 4546–4556, May 2017, doi: 10.1021/acs.chemmater.7b01276.

[71] P. R. Whelan *et al.*, "Raman spectral indicators of catalyst decoupling for transfer of CVD grown 2D materials," *Carbon N Y*, vol. 117, pp. 75–81, Jun. 2017, doi: 10.1016/j.carbon.2017.02.028.

[72] S. Zhao, R. Mu, Y. Ning, Q. Fu, and X. Bao, "Modulating electronic structure of graphene overlayers through electrochemical intercalation," *Appl Surf Sci*, vol. 522, Aug. 2020, doi: 10.1016/j.apsusc.2020.146359.

[73] Y. Xu, J. Qu, Y. Shen, and W. Feng, "Different graphene layers to enhance or prevent corrosion of polycrystalline copper," *RSC Adv*, vol. 8, no. 27, pp. 15181–15187, 2018, doi: 10.1039/c8ra00412a.

[74] P. Braeuninger-Weimer *et al.*, "Crystal Orientation Dependent Oxidation Modes at the Buried Graphene-Cu Interface," *Chemistry of Materials*, vol. 32, no. 18, pp. 7766–7776, Sep. 2020, doi: 10.1021/acs.chemmater.0c02296.

[75] P. Gupta *et al.*, "A facile process for soak-and-peel delamination of CVD graphene from substrates using water," *Sci Rep*, vol. 4, Jan. 2014, doi: 10.1038/srep03882.

[76] S. Bae *et al.*, "Roll-to-roll production of 30-inch graphene films for transparent electrodes," *Nat Nanotechnol*, vol. 5, no. 8, pp. 574–578, Aug. 2010, doi: 10.1038/nnano.2010.132.

[77] M. Hempel *et al.*, "Repeated roll-to-roll transfer of two-dimensional materials by electrochemical delamination," *Nanoscale*, vol. 10, no. 12, pp. 5522–5531, Mar. 2018, doi: 10.1039/c7nr07369k.

[78] B. Jang *et al.*, "Damage mitigation in roll-to-roll transfer of CVD-graphene to flexible substrates," *2d Mater*, vol. 4, no. 2, Jun. 2017, doi: 10.1088/2053-1583/aa57fa.

[79] B. N. Chandrashekar *et al.*, "Roll-to-Roll Green Transfer of CVD Graphene onto Plastic for a Transparent and Flexible Triboelectric Nanogenerator," *Advanced Materials*, vol. 27, no. 35, pp. 5210–5216, Sep. 2015, doi: 10.1002/adma.201502560.

[80] A. H. Castro Neto, F. Guinea, N. M. R. Peres, K. S. Novoselov, and A. K. Geim, "The electronic properties of graphene," *Rev Mod Phys*, vol. 81, no. 1, pp. 109–162, Jan. 2009, doi: 10.1103/RevModPhys.81.109.

[81] O. M. Nayfeh, "Graphene transistors on mechanically flexible polyimide incorporating atomic-layer-deposited gate dielectric," *IEEE Electron Device Letters*, vol. 32, no. 10, pp. 1349–1351, Oct. 2011, doi: 10.1109/LED.2011.2163489.

[82] W. Wei *et al.*, "Graphene FETs with aluminum bottom-gate electrodes and its natural oxide as dielectrics," *IEEE Trans Electron Devices*, vol. 62, no. 9, pp. 2769–2773, Sep. 2015, doi: 10.1109/TED.2015.2459657.

[83] Y. Ohno, K. Maehashi, Y. Yamashiro, and K. Matsumoto, "Electrolyte-gated graphene field-effect transistors for detecting ph and protein adsorption," *Nano Lett*, vol. 9, no. 9, pp. 3318–3322, Sep. 2009, doi: 10.1021/nl901596m.

[84] V. C. Sanchez, A. Jachak, R. H. Hurt, and A. B. Kane, "Biological interactions of graphene-family nanomaterials: An interdisciplinary review," *Chemical Research in Toxicology*, vol. 25, no. 1. pp. 15–34, Jan. 13, 2012. doi: 10.1021/tx200339h.

[85] F. Yan, M. Zhang, and J. Li, "Solution-Gated Graphene Transistors for Chemical and Biological Sensors," *Adv Healthc Mater*, vol. 3, no. 3, pp. 313–331, 2014, doi: 10.1002/adhm.201300221.

[86] L. Han, Q. Wan, A. Zheng, Y. Guo, and Y. Chen, "Demonstration of a Flexible Graphene-Based Biosensor for Sensitive and Rapid Detection of Ovarian Cancer Cells," *Nanoscale Res Lett*, vol. 16, no. 1, 2021, doi: 10.1186/s11671-021-03633-9.

[87] P. Labroo and Y. Cui, "Flexible graphene bio-nanosensor for lactate," *Biosens Bioelectron*, vol. 41, no. 1, pp. 852–856, Mar. 2013, doi: 10.1016/j.bios.2012.08.024.

[88] J. H. An, S. J. Park, O. S. Kwon, J. Bae, and J. Jang, "High-performance flexible graphene aptasensor for mercury detection in mussels," *ACS Nano*, vol. 7, no. 12, pp. 10563–10571, Dec. 2013, doi: 10.1021/nn402702w.

[89] K. E. Laliberte, P. Scott, N. I. Khan, M. S. Mahmud, and E. Song, "A wearable graphene transistor-based biosensor for monitoring IL-6 biomarker," *Microelectron Eng*, vol. 262, Jun. 2022, doi: 10.1016/j.mee.2022.111835.

[90] D. Kireev *et al.*, "Graphene Field-Effect Transistors for In Vitro and Ex Vivo Recordings," *IEEE Trans Nanotechnol*, vol. 16, no. 1, pp. 140–147, Jan. 2017, doi: 10.1109/TNANO.2016.2639028.

[91] J. Gao *et al.*, "Ultrasensitive Label-free MiRNA Sensing Based on a Flexible Graphene Field-Effect Transistor without Functionalization," *ACS Appl Electron Mater*, vol. 2, no. 4, pp. 1090–1098, Apr. 2020, doi: 10.1021/acsaelm.0c00095.

[92] Y. Yang *et al.*, "Ultrafine Graphene Nanomesh with Large On/Off Ratio for High-Performance Flexible Biosensors," *Adv Funct Mater*, vol. 27, no. 19, May 2017, doi: 10.1002/adfm.201604096.

[93] Z. Wang, Z. Hao, S. Yu, C. Huang, Y. Pan, and X. Zhao, "A wearable and deformable graphene-based affinity nanosensor for monitoring of cytokines in biofluids," *Nanomaterials*, vol. 10, no. 8, pp. 1–9, Aug. 2020, doi: 10.3390/nano10081503.

[94] C. Huang, Z. Hao, T. Qi, Y. Pan, and X. Zhao, "An integrated flexible and reusable graphene field effect transistor nanosensor for monitoring glucose," *Journal of Materiomics*, vol. 6, no. 2, pp. 308–314, Jun. 2020, doi: 10.1016/j.jmat.2020.02.002.

[95] L. Xiang, Z. Wang, Z. Liu, S. E. Weigum, Q. Yu, and M. Y. Chen, "Inkjet-Printed Flexible Biosensor Based on Graphene Field Effect Transistor," *IEEE Sens J*, vol. 16, no. 23, pp. 8359–8364, Dec. 2016, doi: 10.1109/JSEN.2016.2608719.

[96] Y. H. Kwak *et al.*, "Flexible glucose sensor using CVD-grown graphene-based field effect transistor," *Biosens Bioelectron*, vol. 37, no. 1, pp. 82–87, Aug. 2012, doi: 10.1016/j.bios.2012.04.042.

[97] C. Sung, W. Jeon, K. S. Nam, Y. Kim, H. Butt, and S. Park, "Multimaterial and multifunctional neural interfaces: From surface-type and implantable electrodes to fiber-based devices," *Journal of Materials Chemistry B*, vol. 8, no. 31. Royal Society of Chemistry, pp. 6624–6666, Aug. 21, 2020. doi: 10.1039/d0tb00872a.

[98] E. Song, J. Li, S. M. Won, W. Bai, and J. A. Rogers, "Materials for flexible bioelectronic systems as chronic neural interfaces," *Nature Materials*, vol. 19, no. 6. Nature Research, pp. 590–603, Jun. 01, 2020. doi: 10.1038/s41563-020-0679-7.

[99] A. Schüz and G. Palm, "Density of neurons and synapses in the cerebral cortex of the mouse," *Journal of Comparative Neurology*, vol. 286, no. 4, pp. 442–455, Aug. 1989, doi: 10.1002/cne.902860404.

[100] J. Zhang, "Basic Neural Units of the Brain: Neurons, Synapses and Action Potential," May 2019, [Online]. Available: http://arxiv.org/abs/1906.01703

[101] L. P. Savtchenko and D. A. Rusakov, "The optimal height of the synaptic cleft," 2007.

[102] S. E. Hyman, "Neurotransmitters," *Current Biology*, vol. 15, no. 5, pp. R154–R158, Mar. 2005, doi: 10.1016/j.cub.2005.02.037.

[103] S. D. Iversen and L. L. Iversen, "Dopamine: 50 years in perspective," *Trends in Neurosciences*, vol. 30, no. 5. pp. 188–193, May 2007. doi: 10.1016/j.tins.2007.03.002.

[104] X. Yang *et al.*, "Bioinspired neuron-like electronics," *Nat Mater*, vol. 18, no. 5, pp. 510–517, May 2019, doi: 10.1038/s41563-019-0292-9.

[105] B. M. Blaschke *et al.*, "Flexible graphene transistors for recording cell action potentials," *2d Mater*, vol. 3, no. 2, Apr. 2016, doi: 10.1088/2053-1583/3/2/025007.

[106] C. Hébert *et al.*, "Flexible Graphene Solution-Gated Field-Effect Transistors: Efficient Transducers for Micro-Electrocorticography," *Adv Funct Mater*, vol. 28, no. 12, Mar. 2018, doi: 10.1002/adfm.201703976.

[107] B. M. Blaschke *et al.*, "Mapping brain activity with flexible graphene micro-transistors," *2d Mater*, vol. 4, no. 2, Jun. 2017, doi: 10.1088/2053-1583/aa5eff.

[108] W. H. Lee *et al.*, "Microfabrication and in Vivo Performance of a Microdialysis Probe with Embedded Membrane," *Anal Chem*, vol. 88, no. 2, pp. 1230–1237, Jan. 2016, doi: 10.1021/acs.analchem.5b03541.

[109] A. Weltin and J. Kieninger, "Electrochemical methods for neural interface electrodes," *J Neural Eng*, vol. 18, no. 5, Oct. 2021, doi: 10.1088/1741-2552/ac28d5.

[110] R. B. Keithley *et al.*, "Higher sensitivity dopamine measurements with faster-scan cyclic voltammetry," *Anal Chem*, vol. 83, no. 9, pp. 3563–3571, May 2011, doi: 10.1021/ac200143v.

[111] E. Castagnola *et al.*, "Glassy carbon microelectrode arrays enable voltage-peak separated simultaneous detection of dopamine and serotonin using fast scan cyclic voltammetry," *Analyst*, vol. 146, no. 12, pp. 3955–3970, Jun. 2021, doi: 10.1039/d1an00425e.

[112] B. Batra and C. S. Pundir, "An amperometric glutamate biosensor based on immobilization of glutamate oxidase onto carboxylated multiwalled carbon nanotubes/gold nanoparticles/chitosan composite film modified Au electrode," *Biosens Bioelectron*, vol. 47, pp. 496–501, Sep. 2013, doi: 10.1016/j.bios.2013.03.063.

[113] X. Liu and J. Liu, "Biosensors and sensors for dopamine detection," *View*, vol. 2, no. 1, p. 20200102, Feb. 2021, doi: 10.1002/viw.20200102.

[114] T. Hianik, "Aptamer-based biosensors," in *Encyclopedia of Interfacial Chemistry: Surface Science and Electrochemistry*, Elsevier, 2018, pp. 11–19. doi: 10.1016/B978-0-12-409547-2.13492-4.

[115] Q. Liu *et al.*, "Flexible Multiplexed In2O3 Nanoribbon Aptamer-Field-Effect Transistors for Biosensing," *iScience*, vol. 23, no. 9, Sep. 2020, doi: 10.1016/j.isci.2020.101469.

[116] H. J. Lee, N. Choi, E. S. Yoon, and I. J. Cho, "MEMS devices for drug delivery," *Advanced Drug Delivery Reviews*, vol. 128. Elsevier B.V., pp. 132–147, Mar. 15, 2018. doi: 10.1016/j.addr.2017.11.003.

[117] U. Chae *et al.*, “A new MEMS neural probe system integrated with push-pull microfluidic channels and biosensors for real-time monitoring of neurochemicals,” in *2016 IEEE 29th International Conference on Micro Electro Mechanical Systems (MEMS)*, IEEE, Jan. 2016, pp. 329–332. doi: 10.1109/MEMSYS.2016.7421627.

[118] M. M. Klein *et al.*, “Transcranial magnetic stimulation of the brain: Guidelines for pain treatment research,” *Pain*, vol. 156, no. 9. Lippincott Williams and Wilkins, pp. 1601–1614, Sep. 01, 2015. doi: 10.1097/j.pain.0000000000000210.

[119] H. J. Park, G. Bonmassar, J. A. Kaltenbach, A. G. Machado, N. F. Manzoor, and J. T. Gale, “Activation of the central nervous system induced by micro-magnetic stimulation,” *Nat Commun*, vol. 4, 2013, doi: 10.1038/ncomms3463.

[120] A. Khalifa *et al.*, “The development of microfabricated solenoids with magnetic cores for micromagnetic neural stimulation,” *Microsyst Nanoeng*, vol. 7, no. 1, Dec. 2021, doi: 10.1038/s41378-021-00320-8.

[121] W. Lee *et al.*, “Image-Guided Focused Ultrasound-Mediated Regional Brain Stimulation in Sheep,” *Ultrasound Med Biol*, vol. 42, no. 2, pp. 459–470, Feb. 2016, doi: 10.1016/j.ultrasmedbio.2015.10.001.

[122] S. S. Yoo *et al.*, “Focused ultrasound modulates region-specific brain activity,” *Neuroimage*, vol. 56, no. 3, pp. 1267–1275, Jun. 2011, doi: 10.1016/j.neuroimage.2011.02.058.

[123] S. Kim *et al.*, “Transcranial focused ultrasound stimulation with high spatial resolution,” *Brain Stimul*, vol. 14, no. 2, pp. 290–300, Mar. 2021, doi: 10.1016/j.brs.2021.01.002.

[124] K. Ko *et al.*, “Micromachined ultrasound transducer array for cell stimulation with high spatial resolution,” in *2015 28th IEEE International Conference on Micro Electro Mechanical Systems (MEMS)*, IEEE, Jan. 2015, pp. 651–654. doi: 10.1109/MEMSYS.2015.7051041.

[125] V. Salanova, “Deep brain stimulation for epilepsy,” *Epilepsy and Behavior*, vol. 88. Academic Press Inc., pp. 21–24, Nov. 01, 2018. doi: 10.1016/j.yebeh.2018.06.041.

[126] V. Jain *et al.*, “Focused Epicranial Brain Stimulation by Spatial Sculpting of Pulsed Electric Fields Using High Density Electrode Arrays,” *Advanced Science*, vol. 10, no. 20, Jul. 2023, doi: 10.1002/advs.202207251.

[127] S. Zhao *et al.*, “Full activation pattern mapping by simultaneous deep brain stimulation and fMRI with graphene fiber electrodes,” *Nat Commun*, vol. 11, no. 1, Dec. 2020, doi: 10.1038/s41467-020-15570-9.

[128] F. Zhang, A. M. Aravanis, A. Adamantidis, L. de Lecea, and K. Deisseroth, “Circuit-breakers: optical technologies for probing neural signals and systems,” *Nat Rev Neurosci*, vol. 8, no. 8, pp. 577–581, Aug. 2007, doi: 10.1038/nrn2192.

[129] F. Zhang *et al.*, “Optogenetic interrogation of neural circuits: Technology for probing mammalian brain structures,” *Nature Protocols*, vol. 5, no. 3. pp. 439–456, Mar. 2010. doi: 10.1038/nprot.2009.226.

[130] J. A. Sahel *et al.*, “Partial recovery of visual function in a blind patient after optogenetic therapy,” *Nat Med*, vol. 27, no. 7, pp. 1223–1229, Jul. 2021, doi: 10.1038/s41591-021-01351-4.

[131] F. Wu, E. Stark, P. C. Ku, K. D. Wise, G. Buzsáki, and E. Yoon, “Monolithically Integrated μLEDs on Silicon Neural Probes for High-Resolution Optogenetic Studies in Behaving Animals,” *Neuron*, vol. 88, no. 6, pp. 1136–1148, 2015, doi: 10.1016/j.neuron.2015.10.032.

[132] S. B. Goncalves, J. F. Ribeiro, A. F. Silva, R. M. Costa, and J. H. Correia, “Design and manufacturing challenges of optogenetic neural interfaces: A review,” *Journal of Neural Engineering*, vol. 14, no. 4. Institute of Physics Publishing, 2017. doi: 10.1088/1741-2552/aa7004.

[133] F. Mohit, A. Ricciardi, A. Cusano, and A. Cutolo, “Tapered multicore optical fiber probe for optogenetics,” *Results in Optics*, vol. 4, Aug. 2021, doi: 10.1016/j.rio.2021.100109.

[134] M. Schwaerzle, P. Elmlinger, O. Paul, and P. Ruther, “Miniaturized 3x3 optical fiber array for optogenetics with integrated 460 nm light sources and flexible electrical interconnection,” in *2015 28th IEEE International Conference on Micro Electro Mechanical Systems (MEMS)*, IEEE, Jan. 2015, pp. 162–165. doi: 10.1109/MEMSYS.2015.7050911.

[135] F. Wu *et al.*, “An implantable neural probe with monolithically integrated dielectric waveguide and recording electrodes for optogenetics applications,” *J Neural Eng*, vol. 10, no. 5, Oct. 2013, doi: 10.1088/1741-2560/10/5/056012.

[136] R. P. Kale, A. Z. Kouzani, K. Walder, M. Berk, and S. J. Tye, “Evolution of optogenetic microdevices,” 2015, doi: 10.1117/1.

[137] J. Voigts, J. Siegle, D. L. Pritchett, and C. I. Moore, “The flexDrive: An ultra-light implant for optical control and highly parallel chronic recording of neuronal ensembles in freely moving mice,” *Front Syst Neurosci*, no. MARCH 2013, Mar. 2013, doi: 10.3389/fnsys.2013.00008.

[138] A. N. Zorzos, E. S. Boyden, and C. G. Fonstad, “Multiwaveguide implantable probe for light delivery to sets of distributed brain targets,” 2010.

[139] Y. Son *et al.*, "In vivo optical modulation of neural signals using monolithically integrated two-dimensional neural probe arrays," *Sci Rep*, vol. 5, Oct. 2015, doi: 10.1038/srep15466.

[140] B. McGovern *et al.*, "A New Individually Addressable Micro-LED Array for Photogenetic Neural Stimulation," *IEEE Trans Biomed Circuits Syst*, vol. 4, no. 6, pp. 469–476, Dec. 2010, doi: 10.1109/TBCAS.2010.2081988.

[141] Y. U. Cho, S. L. Lim, J. H. Hong, and K. J. Yu, "Transparent neural implantable devices: a comprehensive review of challenges and progress," *npj Flexible Electronics*, vol. 6, no. 1. Nature Research, Dec. 01, 2022. doi: 10.1038/s41528-022-00178-4.

[142] D. W. Park *et al.*, "Graphene-based carbon-layered electrode array technology for neural imaging and optogenetic applications," *Nat Commun*, vol. 5, Oct. 2014, doi: 10.1038/ncomms6258.

[143] M. Thunemann *et al.*, "Deep 2-photon imaging and artifact-free optogenetics through transparent graphene microelectrode arrays," *Nat Commun*, vol. 9, no. 1, Dec. 2018, doi: 10.1038/s41467-018-04457-5.

[144] D. W. Park *et al.*, "Fabrication and utility of a transparent graphene neural electrode array for electrophysiology, in vivo imaging, and optogenetics," *Nat Protoc*, vol. 11, no. 11, pp. 2201–2222, Nov. 2016, doi: 10.1038/nprot.2016.127.

[145] D. W. Park *et al.*, "Electrical Neural Stimulation and Simultaneous in Vivo Monitoring with Transparent Graphene Electrode Arrays Implanted in GCaMP6f Mice," *ACS Nano*, vol. 12, no. 1, pp. 148–157, Jan. 2018, doi: 10.1021/acsnano.7b04321.

[146] N. Campos, A. M. Perez-Mas, P. Alvarez, R. Menéndez, and D. Gómez, "Surface treatment of polyimide substrates for the transfer and multitransfer of graphene films," *Appl Surf Sci*, vol. 349, pp. 101–107, Sep. 2015, doi: 10.1016/j.apsusc.2015.04.201.

[147] N. A. Nebogatikova *et al.*, "Functionalization of graphene and few-layer graphene films in an hydrofluoric acid aqueous solution," *Nanotechnol Russ*, vol. 9, no. 1–2, pp. 51–59, 2014, doi: 10.1134/S1995078014010108.

[148] N. A. Nebogatikova, I. V. Antonova, and V. Y. Prinz, "Hydrofluoric acid modifications of graphene films," in *12th International Conference and Seminar on Micro/Nanotechnologies and Electron Devices, EDM'2011 - Proceedings*, 2011, pp. 80–82. doi: 10.1109/EDM.2011.6006900.

[149] K. R. Williams, K. Gupta, and M. Wasilik, "Etch rates for micromachining processing - Part II," *Journal of Microelectromechanical Systems*, vol. 12, no. 6, pp. 761–778, Dec. 2003, doi: 10.1109/JMEMS.2003.820936.

[150] J. D. Yeager, D. J. Phillips, D. M. Rector, and D. F. Bahr, "Mechanical And Electrical Reliability of a Chronically Implanted Metal-Polyimide Electrode Array," 2009.

[151] F. G. Yost, "Soldering to gold films," *Gold Bull*, vol. 10, no. 4, pp. 94–100, Dec. 1977, doi: 10.1007/BF03215439.

[152] Z. Lu *et al.*, "Universal Transfer and Stacking of Chemical Vapor Deposition Grown Two-Dimensional Atomic Layers with Water-Soluble Polymer Mediator," *ACS Nano*, vol. 10, no. 5, pp. 5237–5242, May 2016, doi: 10.1021/acsnano.6b00961.

[153] D. R. Lenski and M. S. Fuhrer, "Raman and optical characterization of multilayer turbostratic graphene grown via chemical vapor deposition," *J Appl Phys*, vol. 110, no. 1, Jul. 2011, doi: 10.1063/1.3605545.

[154] C. C. Chan, W. L. Chung, and W. Y. Woon, "Nucleation and growth kinetics of multi-layered graphene on copper substrate," *Carbon N Y*, vol. 135, pp. 118–124, Aug. 2018, doi: 10.1016/j.carbon.2018.04.044.

[155] C. W. Magnuson *et al.*, "Copper oxide as a 'self-cleaning' substrate for graphene growth," *J Mater Res*, vol. 29, no. 3, pp. 403–409, Feb. 2014, doi: 10.1557/jmr.2013.388.

[156] O. J. Burton *et al.*, "Putting High-Index Cu on the Map for High-Yield, Dry-Transferred CVD Graphene," *ACS Nano*, 2022, doi: 10.1021/acsnano.2c09253.

[157] B. Luo *et al.*, "Graphene-Subgrain-Defined Oxidation of Copper," *ACS Appl Mater Interfaces*, vol. 11, no. 51, pp. 48518–48524, Dec. 2019, doi: 10.1021/acsami.9b15931.

[158] W. Guo, F. Jing, J. Xiao, C. Zhou, Y. Lin, and S. Wang, "Oxidative-Etching-Assisted Synthesis of Centimeter-Sized Single-Crystalline Graphene," *Advanced Materials*, vol. 28, no. 16, pp. 3152–3158, Apr. 2016, doi: 10.1002/adma.201503705.

[159] L. Gan and Z. Luo, "Turning off hydrogen to realize seeded growth of subcentimeter single-crystal graphene grains on copper," *ACS Nano*, vol. 7, no. 10, pp. 9480–9488, Oct. 2013, doi: 10.1021/nn404393b.

[160] F. Wagner, "Texture Determination by Using X ray Diffraction," in *Characterization Techniques of Glasses and Ceramics*, Berlin, Heidelberg: Springer Berlin Heidelberg, 1999, pp. 169–186. doi: 10.1007/978-3-662-03871-0_9.

[161] C. F. Gu, M. Hoffman, L. S. Toth, and Y. D. Zhang, "Grain size dependent texture evolution in severely rolled pure copper," *Mater Charact*, vol. 101, pp. 180–188, 2015, doi: 10.1016/j.matchar.2015.02.003.

[162] C. Da Liao *et al.*, “Optimizing PMMA solutions to suppress contamination in the transfer of CVD graphene for batch production,” *Beilstein Journal of Nanotechnology*, vol. 13, pp. 796–806, 2022, doi: 10.3762/BJNANO.13.70.

APPENDIX I – GFET FUNCTIONALIZATION PROCESS

The liquid gated GFETs can react to some components of the analyte applied on them. In complex analytes, there is an interest in detecting only a certain component, even if present only in small concentrations. As such, there have been developed processes to modify graphene that make it react with the desired molecule with high selectivity and affinity. The process intended to be utilized with the GFETs designed in this work rely on the utilization of aptamers, single strands of DNA designed for high affinity and selectivity towards specific molecules, in this case dopamine, described in [10], and as follows (Figure 74):

1. The GFETs are incubated in 2 mM 1-Dodecanethiol for 4h and then cleaned with DI water and dried under N_2 flow.
2. A drop of 20 µL of 10 mM 1-Pyrenebutyric acid N-hydroxysuccinimide, dissolved in dimethylformamide, is added on top of the GFETs for 2h in a humid chamber, and then cleaned as in the previous step.
3. The DNA aptamer sequence is dissolved in MilliQ water down to 20 µM and a 20 µL drop is applied on the GFETs for 16h in a humid chamber in the dark, followed by the cleaning procedure.
4. A drop of 20 µL of 100 mM ethanolamine dissolved in DI water is incubated on the GFETs for 30 minutes, followed by DI water rinse and dried under N_2 flow.

Succinctly, these steps encompass the passivation of the gate electrode (1), the introduction of the linker molecule on top of the graphene (2), the binding of the aptamer to the linker (3), and finally the passivation of linkers with no aptamer to prevent non-specific binding of molecules (4).

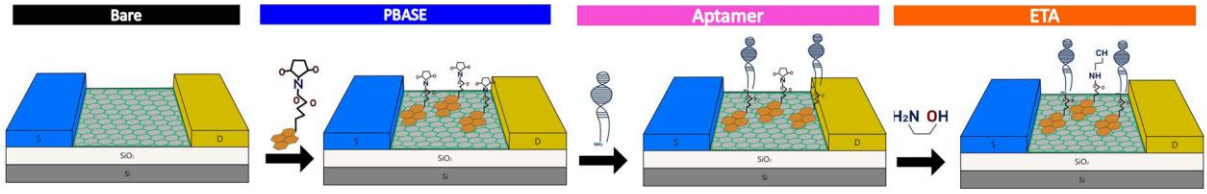


Figure 74 – Steps of the functionalization of graphene in liquid gated GFETs for dopamine detection with aptamers. The passivation of the gold electrode is omitted.

APPENDIX II – μLED MOUNTING TEST WAFER FABRICATION STEPS

Table 4 – Simplified runsheet of μLED mounting test wafer fabrication.
Metrology related steps are not represented.

Process Step	Description	Comment
Si Wafer	-	-
PECVD SiO2	Deposition of 500 nm of SiO_2	-
Spin Coat of PI 2611	Achieved 3.5 μm thickness of PI substrate.	Visible bubbles and "comets" on the surface after soft bake.
Patterning of AZ1505 for tracks lift-off	AZ1505 photoresist was spin-coated and lithographically patterned. The photoresist was soaked to improve definition.	-
Sputter Au/Cr	Cr and Au were sputtered on the wafer, achieving 5nm and 45 nm thickness, respectively.	-
Lift-off	The wafer was immersed in acetone, exposed to ultrasounds, and later cleaned in IPA and DI water.	-
Spin Coat of PI 2611	Achieved 3.5 μm thickness of PI passivation.	Visible bubbles and "comets" on the surface after soft bake. Good conformity.
Patterning of AZ1505 for AlSiCu Sacrificial Layer lift-off	AZ1505 photoresist was spin-coated and lithographically patterned.	-
Sputter AlSiCu Sacrificial Layer	Deposition of 100 nm of AlSiCu.	A soft etch was done prior to the deposition to enhance adhesion of the film.
Lift-off	The wafer was immersed in acetone, exposed to ultrasounds, and later cleaned in IPA and DI water.	-
PI Via Opening and Patterning by RIE	RIE in CF_4 and O_2 plasma was used to etch PI down to the Au/Cr.	The etch was done in steps until the etch rate reduced in regions with underlying Au. PI residues were left on top of Au tracks, of which the thickness was reduced.
AlSiCu Sacrificial Layer Strip	AlSiCu layer fully removed in Al etchant.	Immersion in acetone took longer than expected. Chemistry of the RIE possibly modified the AlSiCu, making is harder to remove.
Dicing	The wafer was covered in a thick layer of photoresist and diced in 6 mm x 6 mm chips.	Due to the topography of the wafer, the photoresist spin-coat was not even.
HF Dry Etch of SiO_2	Individual chips were exposed to the dry etch process to release PI from the Si substrate.	-

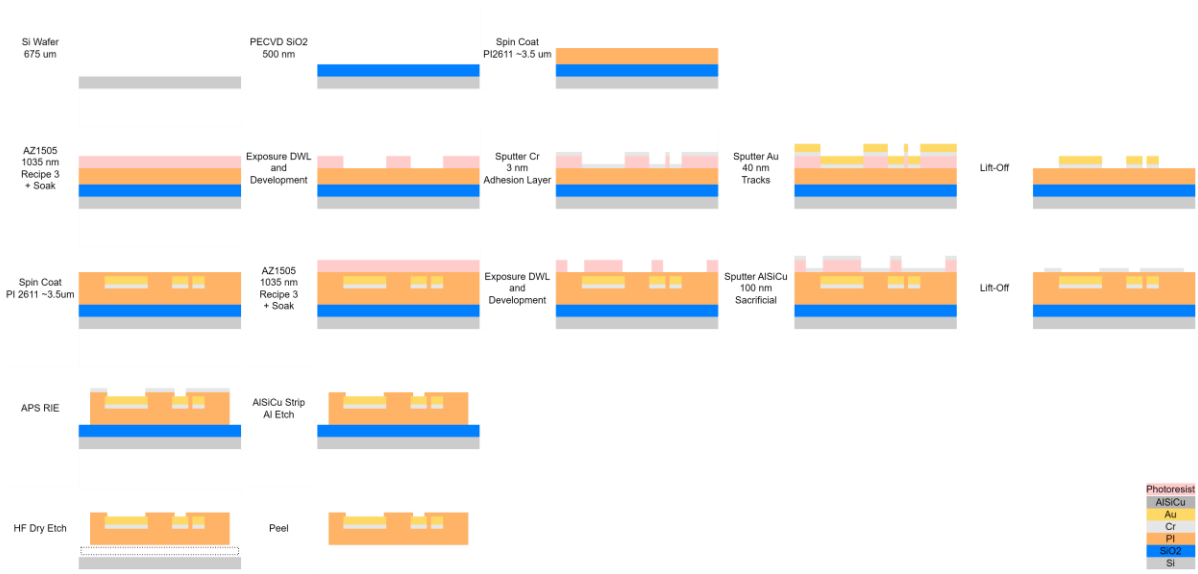


Figure 75 - Schematic of the fabrication steps of the µLED mounting test wafer.

APPENDIX III – DUMMY WAFER FABRICATION STEPS

Table 5 – Simplified runsheet of dummy wafer fabrication.
Metrology related steps are not represented.

Process Step	Description	Comment
Si Wafer	-	-
PECVD SiO2	Deposition of 500 nm of SiO_2	-
Spin Coat of PI 2611	Achieved 3.5 µm thickness of PI substrate.	Visible bubbles and "comets" on the surface after soft bake.
Sputter AlSiCu Sacrificial Layer	Deposition of 200 nm of AlSiCu	A soft etch was done prior to the deposition to enhance adhesion of the film.
Patterning of AlSiCu Sacrificial Layer	AZ1505 photoresist was spin-coated and lithographically patterned. AlSiCu was wet etched, and the photoresist later removed with acetone.	-
PI Patterning by RIE	RIE in CF_4 and O_2 plasma was used to etch PI down to the SiO_2.	A slight overetch was done to ensure complete PI removal.
AlSiCu Sacrificial Layer Strip	AlSiCu layer fully removed in Al etchant.	-
Patterning of AZ1505 for tracks lift-off	AZ1505 photoresist was spin-coated and lithographically patterned. The photoresist was soaked to improve definition.	The patterned PI hindered even spin-coating due to the non-uniform surface.
Sputter Au/Cr	Cr and Au were sputtered on the wafer, achieving 3nm and 35 nm thickness, respectively.	-
Lift-off	The wafer was immersed in acetone, exposed to ultrasounds, and later cleaned in IPA and DI water.	The non-even spin-coating of the photoresist resulted in a number of defects in the patterned Au/Cr tracks.

Figure 76 – Schematic of the fabrication steps of the dummy wafer. The non-executed fabrication steps are represented in fainter colors.

APPENDIX IV – SPACER LAYER PATTERNING

The spacer layer was fabricated in PET and patterned by CO_2 laser cutting. Two different cutting modes were utilized, being the scan and pulse. The scanning mode moves the laser while it continuously hits the PET with the high intensity focused light and was utilized to do the cutout of the layer in the PET film (Figure 77a). The pulse mode shines a short pulse of high intensity light at a given location, creating a cylindrical cavity in the film (Figure 77c).
The cavities created by the pulse mode would then be used to fit the μLEDs and, as such, require a diameter capable of accommodating them. By tuning the power of the laser, the diameter of the cavity could be modified, and a diameter of over 460 μm was achieved (Figure 77c) by applying 60% of laser power during a pulse. These dimensions are suitable for the fitting of the μLEDs.

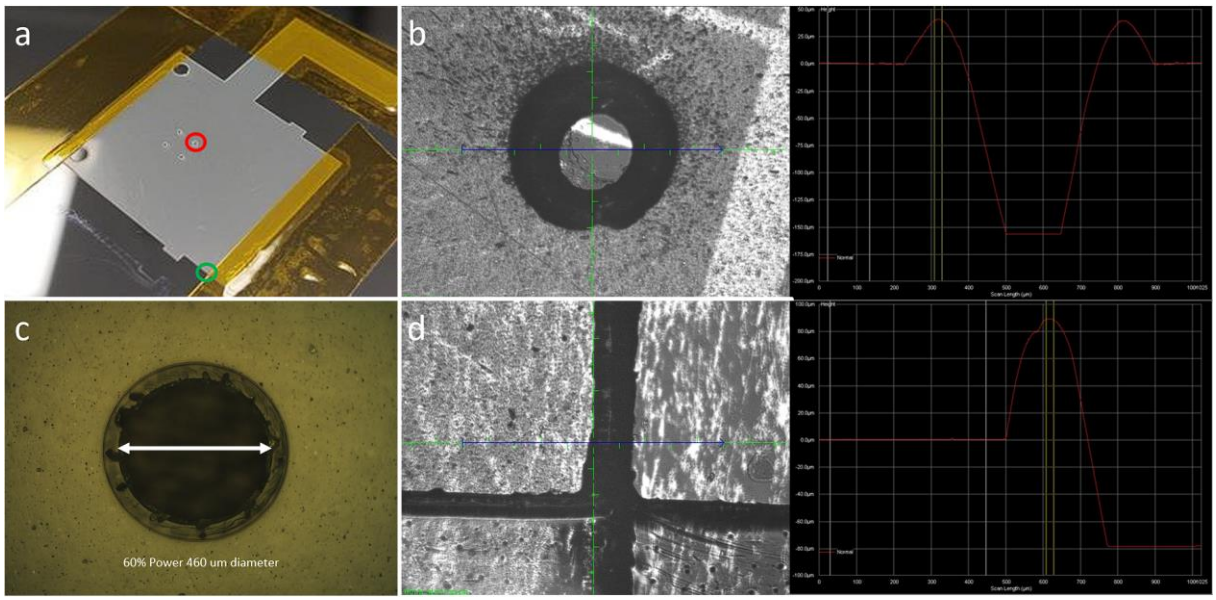


Figure 77 – Patterning of the PET layer.
(a) Image of a patterned PET layer. The red and green circles denote a cavity and an edge where contact profilometer measurements took place, respectively. (b,d) OM images and respective contact profilometer measurements of a patterned cavity and edge, respectively. (c) OM image of a patterned cavity with 460 μm in diameter seen from the top side.

Nevertheless, one should also consider the tall edges formed during the patterning of the PET. By performing contact profilometer measurements on both the cavities (Figure 77b) and the PET edge (Figure 77d), it is noticeable how a tall ridge is formed near the edges of both locations. These ridges can complicate assembly of the device and hinder a flat surface. To overcome this issue, the PET would be patterned in a mirrored layout and then flipped, so the ridges face the μLED layer instead of the GFET array. As there is a necessity to glue all the layers, the void space that these ridges would create would in turn be used to allocate the glueing material.

APPENDIX V – DEVICE WAFER FABRICATION STEPS

Table 6 – Simplified runsheet of µLED mounting test wafer fabrication.
Metrology related steps are not represented.

Process Step	Description	Comment
Si Wafer	-	-
PECVD SiO2	Deposition of 500 nm of SiO_2	-
Spin Coat of PI 2611	Achieved 3.5 µm thickness of PI substrate.	Visible bubbles and "comets" on the surface after soft bake.
Patterning of AZ1505 for tracks lift-off	AZ1505 photoresist was spin-coated and lithographically patterned. The photoresist was soaked to improve definition.	-
Sputter Au/Cr	Cr and Au were sputtered on the wafer, achieving 10 nm and 100 nm thickness, respectively.	-
Lift-off	The wafer was immersed in acetone, exposed to ultrasounds, and later cleaned in IPA and DI water.	-
Graphene Wet Transfer	OxGr was wet transferred onto the patterned Au/Cr tracks. PMMA was removed in acetone.	High number of residues and graphene tears present after the PMMA removal.

Figure 78 - Schematic of the fabrication steps of the device wafer. The non-executed fabrication steps are represented in fainter colors.

APPENDIX VI – PMMA RESIDUES ON GRAPHENE

The graphene wet transfer relies on the usage of a support polymer. One of the most used polymers, as the one used in this work, is PMMA, and it is known to produce residues on top of the graphene surface which p-type dope the material. The utilized PMMA in this work is prepared by dissolving PMMA-550k and PMMA-150k in 2:1 ratio (3% wt) in anisole (97% w), as it was deemed optimal for suppression of contaminations in the wet transfer of graphene, producing the highest quality transfer [162].
During the development of this work, an unusual behavior of the prepared PMMA was observed, and significant amounts of residues were being left on the graphene, even after adequate removal of the polymer with acetone. A standard wet transfer of noOxGr graphene was performed on top of an SiO_2 substrate, and OM images were acquired, as depicted in (Figure 79). It is visible throughout the area of the transfer that bright green dots are present, attributed to PMMA residues. In higher zoom images, these are also present in the form of a sheet that covers some areas of the graphene. Furthermore, higher dimension residues are also present, attributed to bigger-sized residues formed during the removal of the PMMA in acetone.

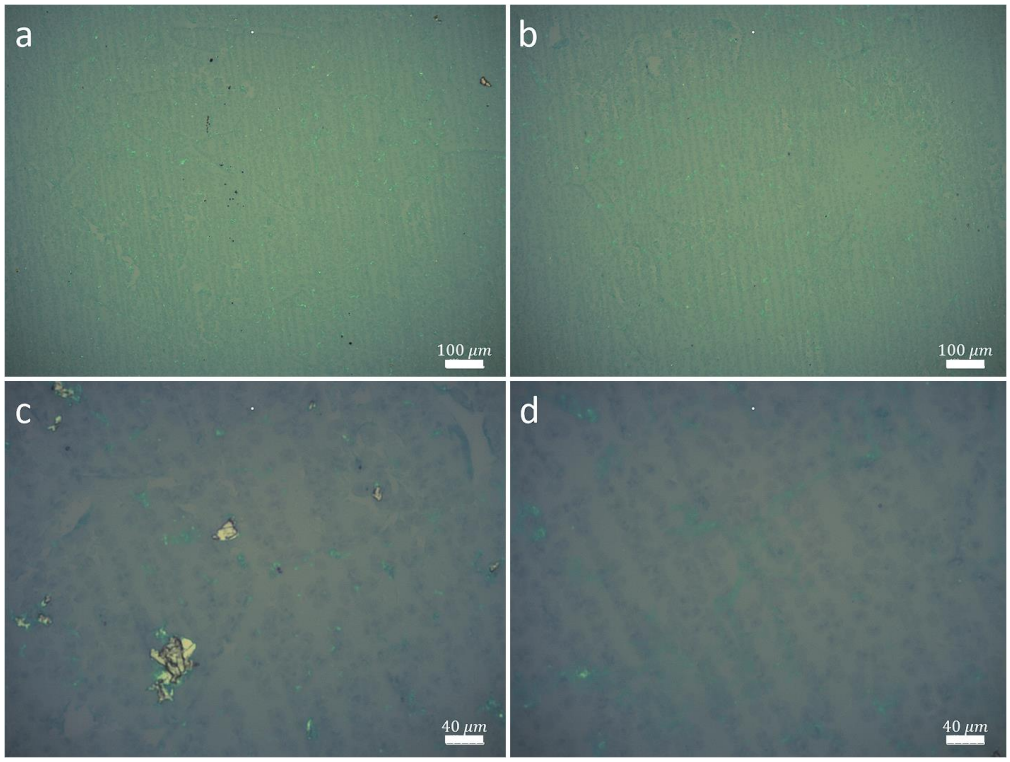


Figure 79 – OM images of wet transferred graphene onto SiO_2, after removal of compromised PMMA with acetone.

This entailed that one or more of the three utilized reagents might have been compromised, and a replacement was necessary. This replacement did not occur in time for this work, leading to the utilization of the compromised reagents during the wet transfer in section 4.2.4, and a subsequent hesitation on continuing the fabrication process of the device wafer.

APPENDIX VII – RAMAN MEASUREMENT OF GRAPHENE ON PI

Raman spectroscopy is a standard technique in the characterization of graphene and is utilized for both assessing graphene quality as well as coverage after a transfer onto a target substrate. As graphene is on top of a substrate, its Raman signal will also be detected, and it can be a limiting factor on the acquisition of signal from graphene.

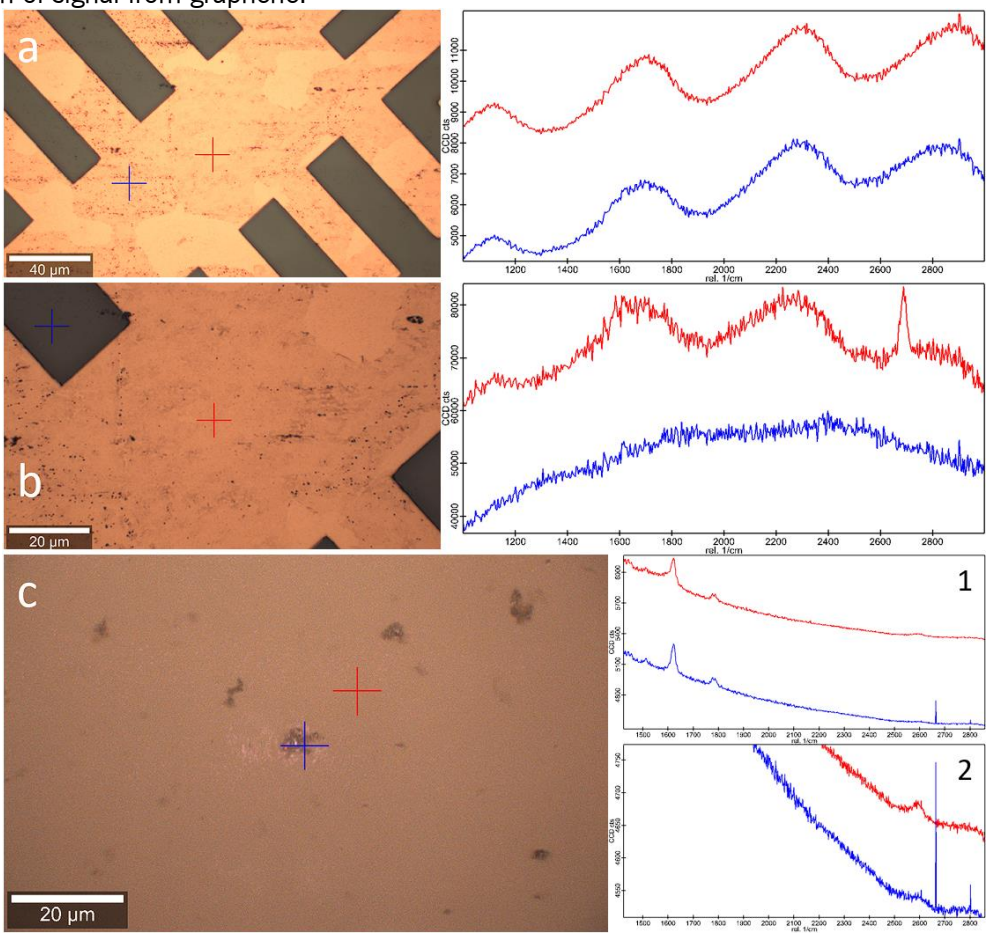


Figure 80 – Raman measurements of graphene on PI.
(a) Graphene transferred onto Au on PI and bare PI and respective Raman spectrum with 532 nm laser and 2 mW power with 50x zoom lens. (b) Region in (a) under 100x zoom lens and respective Raman spectrum. (c) Graphene transferred onto bare PI and Raman spectrum with 785 nm laser and 10 mW power utilizing 100x zoom lens.

Raman measurements were performed on graphene transferred on top of PI and Au on PI, on the dummy wafer, and results are exposed in Figure 80. In Figure 80a, measurements with 532 nm laser with 2 mW power show an oscillation on top of a background signal, attributed to interference caused by the 30 nm of Au deposited on top of the PI. Although in the OM images the graphene coverage is evident, no corresponding signal is detected. In Figure 80b, a higher zoom lens (100x) was utilized, in order to achieve a smaller depth of focus, and reduce the Raman signal originating from the PI. This time, on top of the Au it is possible to observe the 2D peak of graphene amid the oscillations, although the D and G peak are not noticeable. The Raman measurement from the graphene transferred onto the bare PI only shows a background signal from the PI, and the D, G and 2D peaks are not noticeable. In (FIG)c, a 785 nm laser, with 10 mW power, and the highest zoom lens (100x), with the smallest depth of focus, was

utilized in order to move away from the background signal originating from the PI. A region of graphene transferred onto bare PI was analyzed. With this laser, it is possible to observe typical PI peaks in the lower part of the spectrum. Unfortunately, these peaks mask the G peak of graphene. The 2D peak is noticeable near the $2600\ cm^{-1}$ point of the plot. It is blue shifted due to the utilization of a bigger wavelength laser. The peaks are very small in comparison to the background signal, and with no possibility of analyzing the G peak, possible assessments about the graphene quality are limited. Furthermore, the high power utilized can lead to an undesired damage of the substrate. Overall, all these facts and effects deem the analysis of graphene on PI by Raman spectroscopy unpractical with the available equipment, and other methods should be given priority.