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Hybrid Inverter Zeta-Ćuk for Grid-Tied Photovoltaic Applications

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Abstract— This paper proposes a novel single-phase integrated inverter for photovoltaic (PV) applications called Hybrid Inverter Zeta-Ćuk (HIZC). The HIZC operates in discontinuous conduction mode and employs four unidirectional power switches, which are achieved by associating series power diodes to MOSFETs. In addition, during the grid's positive half-cycle, the inverter acts similarly to the Zeta converter. On the other hand, during the negative half-cycle, the inverter operates similarly to the Ćuk converter. Due to the adopted design criteria, the Zeta and the Ćuk operation modes show similar behavior. The small-signals analysis considers the Zeta and Ćuk operation modes, showing a significant similarity between their frequency responses, proofing the similarity of the HIZC's functionality in both operation modes. The HIZC can boost the voltage of the PV array and perform the DC-AC conversion at the same time. The maximum power available at the PV array is harvested using a multi-loop control in conjunction with the perturb-and-observe algorithm, while an AF- $\alpha\beta$ -PLL system guarantees synchronism with the power grid. Experimental results prove the structure feasibility of the proposed topology for PV applications. In addition, the HIZC presents high-efficiency conversion and also low total harmonic distortion in the current injected into the power grid.

Index Terms— Ćuk converter, Integrated Inverter, Photovoltaic System, Power Electronics, Zeta Converter.

I. INTRODUCTION

In recent years, the investments in renewable energy sources have significantly improved [1,2]. This growth is motivated by a necessity to expand electricity generation and distribution [3-6]. Among the renewable energy sources, photovoltaic (PV) is widely employed due to its modular characteristics, guaranteeing large voltage and current ranges [2, 3, 7-9]. Once the PV generation occurs in direct current (DC), it is necessary to adopt one or more power conversion stages when the PV system is used for grid-tied alternating current (AC) applications [6,9].

Conventionally, a PV system uses a double power conversion stage, where a step-up converter, usually a boost converter, is associated with a voltage source inverter (VSI), commonly a full-bridge inverter. This system can control both structures once the power converters are decoupled [10-12].

On the other hand, this system can use many electrical components, presenting lower efficiency and higher weight and volume when compared to the integrated inverter [5, 6, 10, 11].

The integrated inverters are built in distinct ways, with different control strategies for each structure. Usually, these structures can step up the voltage across the PV array and inject a sinusoidal current into the utility grid through a single DC-AC power conversion stage [5, 9].

A modular grid-connected single-phase inverter is presented

in [13]. The module can obtain the individual maximum power in each panel. The topology is based on the Ćuk and SEPIC converters and employs a high-frequency transformer, guaranteeing the necessary gain and galvanic isolation.

In [14], a Ćuk inverter topology with a high-frequency transformer is also used, where a repetitive control is associated. An experimental 500 W setup proves the feasibility of the system. The main results show high efficiency and injected current with low total harmonic distortion (THD).

Similarly, [5] has proposed a bridgeless inverter based on the Zeta converter. The structure can operate in continuous conduction mode (CCM) or discontinuous conduction mode (DCM), using a feedback controller to identify the conduction mode boundaries. Both papers, [5] and [14] use repetitive controllers, guaranteeing a satisfactory response.

A topology based on the DC-DC Zeta converter named Modified Zeta Inverter (MZI) is presented in [6], where the MZI structure operates in DCM. However, its functionality differs from the conventional Zeta converter, which delivers a negative current through the magnetization inductor in the third operation stage. The magnetization inductors of the MZI are series associated with power diodes. Thus, these inductors' power flow is unidirectional once the diodes prevent negative currents.

An integrated inverter based on the Zeta converter for PV applications has been proposed in [9]. The topology named

¹This work was supported in part by the National Council for Scientific and Technological Development (CNPq) under Grant 308620/2021-6 and Grant 304707/2021-0; in part by the Coordenação de Aperfeiçoamento de Pessoal de Nível Superior - Brazil (CAPES) - Financing Code 001, and in part by the National Funds through the Portuguese funding agency FCT under Grant SAICTPAC/0004/2015-POCI01-0145-FEDER-016434

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Single-Phase Integrated Zeta Inverter (SP-IZI) operates in DCM and presents three operation stages in each switching period. The structure combines two modified Zeta modules, where one is responsible for the functionality during the positive half-cycle, and the other is responsible for operating in the negative half-cycle.

A four-switch single-stage and single-phase inverter has been proposed in [15]. The topology is based on the Buck-Boost DC-DC converter and can be employed in autonomous applications or on grid-tied. However, the topology needs an extra inductor for grid-tied applications once the inverter presents discontinuity in the output current.

Although the invert in [15] uses fewer semiconductors than the proposed HIZC, the current flows through three semiconductors simultaneously in some operation stages. The HIZC presents current in two or fewer semiconductors in each operation stage. The elevated number of semiconductors presenting current increases the conduction losses. The inverter in [15] corroborates this issue since the structure shows nearly 2/3 of conduction losses.

In [15], only the theoretical losses are shown, demonstrating the maximum value of 95.7%, which should be lower when measured. The HIZC achieves a maximum efficiency of nearly 96% in the experimental setup.

This paper proposes a new integrated inverter based on the Zeta and the Ćuk conventional topologies. The structure acts as an interface converter between the PV array and the utility grid. Fig. 1 presents the proposed inverter. The HIZC employs four unidirectional power switches built using a series of connected diodes. Thus, the HIZC can be used in microinverters as an interface converter between the PV array and the electrical power grid.

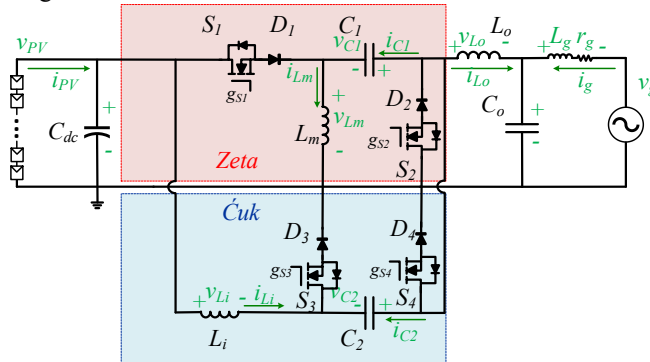


Fig. 1. HIZC proposed topology.

The HIZC proposed topology presents some advantages over other structures, such as: (i) The HIZC can increase the voltage of the PV array and simultaneously perform the DC-AC conversion to the power grid using only a single stage; (ii) The HIZC uses the total voltage of the PV array in the conversion stage, without the need for split capacitors; (iii) The HIZC does not employ a high-frequency transformer; (iv) The characteristics of the topology allows simple control strategies, guaranteeing a sinusoidal output with low distortion; (v) The HIZC is highly efficient; (vi) The voltages across all the semiconductors in the HIZC are relatively low when

considering the input and output voltages of the inverter.

The HIZC converter presents some advantages with respect to the MZI proposed in [6]: (i) The HIZC uses the total PV array voltage, while the MZI must split the voltage between two capacitors equally, and thus, the static gain of the MZI must be higher, provoking more losses; (ii) The magnetization inductors of the MZI operate only in half-cycle, while the magnetization inductors of the HIZC operate during the whole cycle, splitting the current between two inductors, reducing the peak and the RMS value of the current, and thus reducing the conduction losses; (iii) The voltage stress in the switches of the HIZC is lower than that of the MZI, which reduces the losses and the demonstrable damage to the components.

The HIZC offers some advantages with respect to the SP-IZI [9]. The main benefit is the fact that the HIZC uses the total voltage in the PV array, while the SP-IZI splits equally this voltage across two capacitors. In addition, the L_i inductor in the HIZC offers better input current filtering than the SP-IZI.

This paper is organized as follows: Section II presents the operation, functionality, main equations, and theoretical waveforms for the HIZC. Section III describes the modeling and control adopted. Section IV compares the experimental results with those of other integrated inverters. Finally, section V presents the conclusions.

II. OPERATION AND FUNCTIONALITY OF THE HIZC

The proposed HIZC acts as an interface converter between a PV array and the single-phase AC utility grid. The HIZC operates in DCM with linear static gain. In DCM, the HIZC operates similarly to the Zeta converter, presenting three operation stages during the positive half-cycle in each switching period, such as $D_{z1}T_s$, $D_{z2}T_s$, and $D_{z3}T_s$. On the other hand, the HIZC operates similarly to the Ćuk converter during the negative half-cycle of the power grid, which presents the following three operation stages: $D_{c1}T_s$, $D_{c2}T_s$, and $D_{c3}T_s$.

The HIZC structure employs four unidirectional power switches deployed by associating series power diodes to the switches. Furthermore, the inverter requires two input inductors, one output inductor, two coupling capacitors, and an output filter capacitor, as presented in Fig. 1.

The proposed control of the HIZC is designed to extract the maximum available power at the PV array while injecting this energy into the utility grid as a sinusoidal synchronized current. The HIZC uses the Perturb and Observe algorithm to perform the maximum power point tracking (MPPT), while the synchronism to the power grid is carried out by an adaptive alpha-beta phase-locked-loop (AF- $\alpha\beta$ -PLL) system. The controllers, MPPT, and PLL algorithms are discretized and embedded in a digital signals processor (DSP), as shown in Fig. 2.

The modulation strategy for the HIZC topology is based on the high-frequency signal obtained by the employed controller and PLL information. Thus, two switches (S_2 and S_4) operate at low-frequency and in a complementary way. In contrast, the signal for the switch S_1 occurs in the positive half-cycle of the power grid by comparing the high-frequency signal to a

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sawtooth wave at the switching frequency. Similarly, it occurs the same with the switch S_3 , during the negative half-cycle of the power grid.

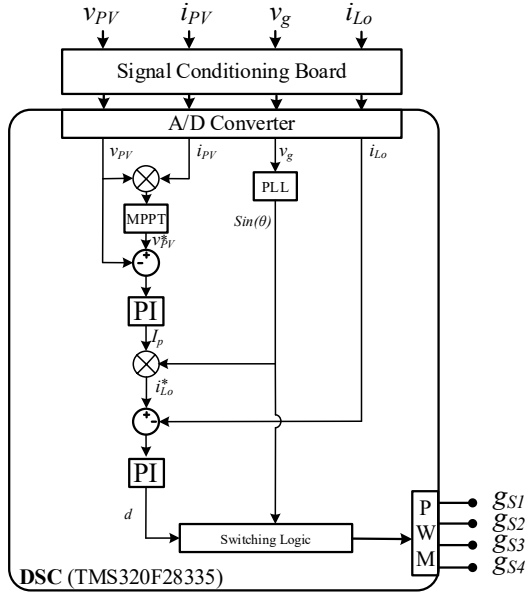


Fig. 2. HIZC control.

A. Zeta Mode

During the positive half-cycle of the power grid, the HIZC operates in Zeta mode. In this mode, switches S_1 and S_2 are commuted, while switches S_3 and S_4 remain turned off during this period.

The first stage of operation, $D_{z1}T_s$, starts when the switch S_1 turns on. The energy in the PV array flows through this switch and diode D_1 , which is forward-biased. In this stage, the inductor L_m is magnetized and energized with the PV-array voltage, v_{PV} , and the voltage across the inductor L_i is the difference between the coupling capacitors C_2 and C_1 , i.e., $v_{Li} = v_{C2} - v_{C1}$.

A relation between the PV voltage, capacitor C_1 , and the grid voltage gives the voltage across the output inductor, $v_{Lo} = v_{PV} + v_{C1} - v_g$. The current through the coupling capacitor C_1 is the sum of the L_o and L_i inductor currents, $i_{C1} = i_{Lo} + i_{Li}$, and the current through the capacitor C_2 is the same as the inductor L_i . Fig. 3 (a) shows the HIZC in this subinterval.

The second operation stage, in Zeta mode, starts when the switch S_1 turns off. The energy accumulated in the inductors flows through the switch S_2 and the power diode D_2 .

The inductor L_m is demagnetized, and its accumulated energy is transferred to the capacitor C_1 . The inductor L_m voltage is the same as the capacitor C_1 , $v_{Lm} = -v_{C1}$. The accumulated energy in the inductor L_i is transferred to the coupling capacitor C_2 . The voltage across this inductor is the difference between the PV-array and capacitor C_2 voltages, i.e. $v_{Li} = v_{PV} - v_{C2}$.

The current through the coupling capacitor C_1 is the same as the inductor L_m , while the current through the capacitor C_2 equals the L_i current during the whole Zeta mode. This stage is visualized in Fig. 3 (b).

The third operation stage, $D_{z3}T_s$, starts when the current through the switch S_2 and diode D_2 is not enough to polarize the diode D_2 , i.e., the sum of the inductors' currents is nearly zero. Thus, the D_2 is reverse-biased, and the currents do not flow through the switch S_2 , although this semiconductor remains turned on during the Zeta mode.

In this operations stage, the energy flows only in the passive elements. The output inductor current is the sum of the L_m and L_i inductors' currents, $i_{Lo} = i_{Lm} + i_{Li}$. The operation stage $D_{z3}T_s$ is shown in Fig. 3 (c).

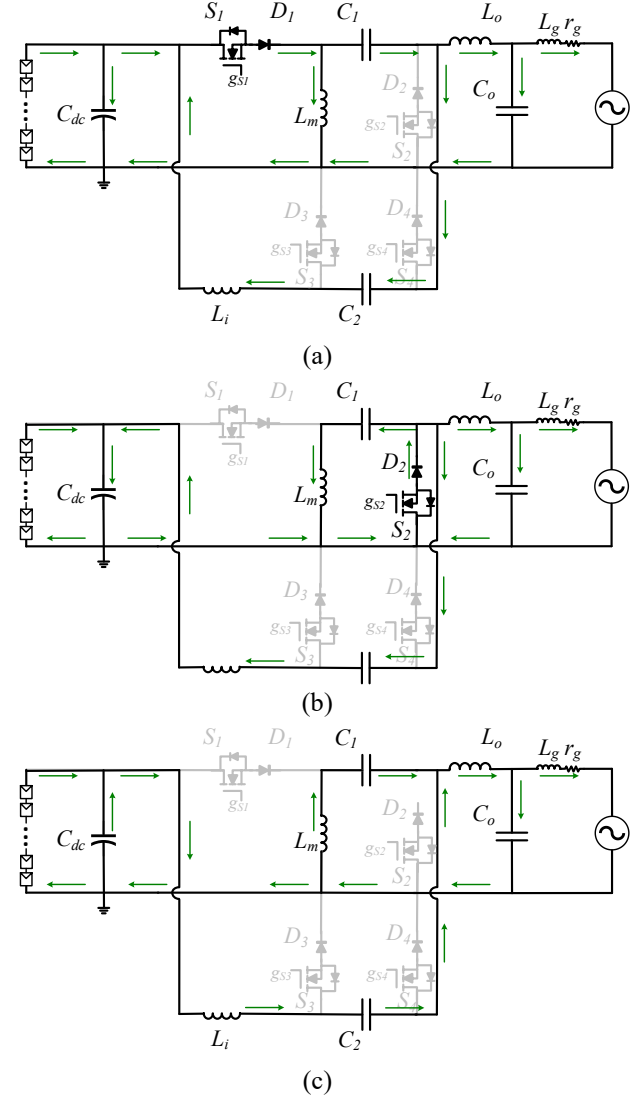


Fig. 3. Operation stages of the Zeta mode: (a) First, $D_{z1}T_s$; (b) Second, $D_{z2}T_s$; (c) Third, $D_{z3}T_s$.

B. Ćuk Mode

In the negative half-cycle of the utility grid, the HIZC topology operates in Ćuk mode. The switches S_3 and S_4 are driven in this mode, in which only switch S_3 is commuted with a high frequency. On the other hand, the switch S_4 is commuted at a low frequency. At the same time, the switches S_1 and S_2 keep turned off during this mode.

The first subinterval in Ćuk mode, $D_{c1}T_s$, starts when the switch S_3 is turned on, allowing the energy to flow through the

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associated diode D_3 . The inductor L_i is energized and magnetized with the power of the PV array, and the voltage across L_i is the PV array voltage, $v_{Li} = v_{PV}$.

The L_m inductor is magnetized with the voltage difference between the coupling capacitors, $v_{Lm} = v_{C2} - v_{C1}$. The difference between the coupling capacitor C_2 and the utility grid, $v_{Lo} = v_{C2} - v_g$ gives the voltage across the output inductor. The current through S_3 and D_3 semiconductors is the sum of the inductors' currents, $i_{S3} = i_{Lm} + i_{Li} + i_{Lo}$.

The current through the coupling capacitor C_2 is the sum of the L_m and L_o currents, $i_{C2} = i_{Lm} + i_{Lo}$, while the C_1 current is the same as the L_m inductor during the whole Ćuk mode. The operation stage $D_{c1}T_s$ is visualized in Fig. 4 (a).

The second operation stage in Ćuk mode, $D_{c2}T_s$, starts when switch S_3 turns off, and the energy flow polarizes de diode D_4 . Switch S_4 is turned on during the whole negative half-wave cycle of the utility grid.

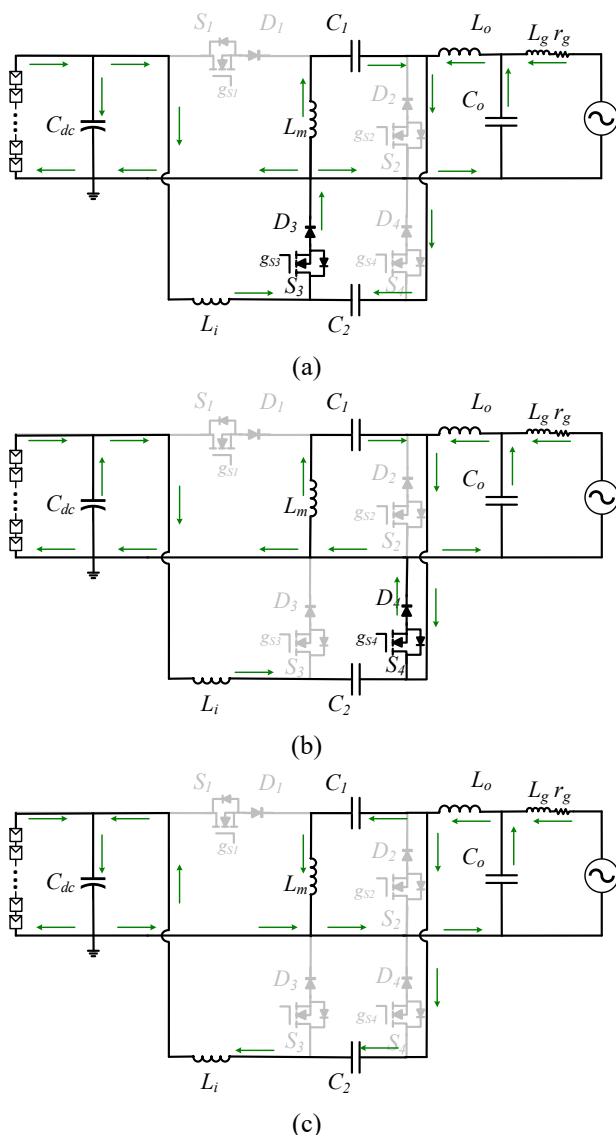


Fig. 4. Operation stages of the Ćuk mode: (a) First, $D_{c1}T_s$; (b) Second, $D_{c2}T_s$; (c) Third, $D_{c3}T_s$.

The energy accumulated in the inductors L_m and L_i are transferred to the capacitors C_1 and C_2 , respectively, and the voltages across these inductors are the same as the capacitors C_1 and C_2 , where $v_{Lm} = -v_{C1}$ and $v_{Li} = -v_{C2}$. The current through the capacitor is the same as the inductor L_i . Fig. 4 (b) presents this operation stage.

Similarly, in the Zeta mode, the third operation stage occurs when the sum of the inductor currents through the diode D_4 is insufficient to keep it forward-biased. Thus, the energy flows only through the passive element. Fig. 4 (c) presents this operation stage of the HIZC.

C. Main Theoretical Waveforms

The main theoretical waveforms for the HIZC converter can be obtained by considering ideal components, making it easier to understand the structure. The insertion of non-ideality and parasitic components causes a more complex understanding without a significant gain. For the same reason, the HIZC modeling also considers all components as ideal.

The current flows through each group formed by a switch and a diode only into an operation stage during a switching period. In the other stages, the group presents distinct voltage levels, which can be through the switch or diode. The current through these groups has the same peak, i_{SP} . The peak current depends on the duty cycle D_{z1} or D_{c1} . Fig 5 shows the theoretical voltages and currents for the switch S_1 , S_2 , and the diodes D_1 and D_2 . The currents and voltages into the switches S_3 and S_4 , besides the diodes D_3 and D_4 , reach the same levels in distinct operation stages.

The voltages across the three inductors are ideally the same level during a switching period. In the first operation stage, the voltage is the same as the PV array voltage. During the second operation stage, the voltage is the same as the power grid, and in the third operation stage, the voltages across all inductors are ideally null.

The current through the inductor L_m is positive during the whole positive power grid half-cycle. On the other hand, during the negative grid half-cycle, the current through the inductor L_m assumes positive and negative levels. The inductor L_i presents positive and negative current levels during the positive grid half-cycle and negative current during the negative grid half-cycle. The output inductor, L_o , presents currents synchronized with the power grid. Fig. 6 (a) exhibits the theoretical waveforms for the inductors during a switching period during the positive grid half-cycle, and Fig. 6 (b) shows the voltages and currents of the inductors during the negative power grid half-cycle.

The positive and negative half-cycles of the power grid determine when the HIZC operates in the Zeta or the Ćuk mode, changing the switches' gate signals. Fig. 7 (a) shows the ideal and theoretical signals for each switch employed in the HIZC. For the positive half-cycle, the gate signal for switch S_1 uses a sinusoidal pulse width modulation (SPWM). Similarly, the gate signal for switch S_3 employs an SPWM during the negative half-cycle. On the other hand, S_2 and S_4 are commuted by the grid frequency, where S_2 is turned on during the positive half-cycle, whereas S_4 is turned on during the negative half-cycle.

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Currents through inductors present distinct waveshapes during the positive and negative half-cycles. According to those mentioned earlier, the input inductor L_i presents the same current as the coupling capacitor C_2 during the positive half-cycle. Thus, the average current is zero for each switching period. However, this inductor is magnetized and demagnetized, presenting a significant current ripple and RMS value.

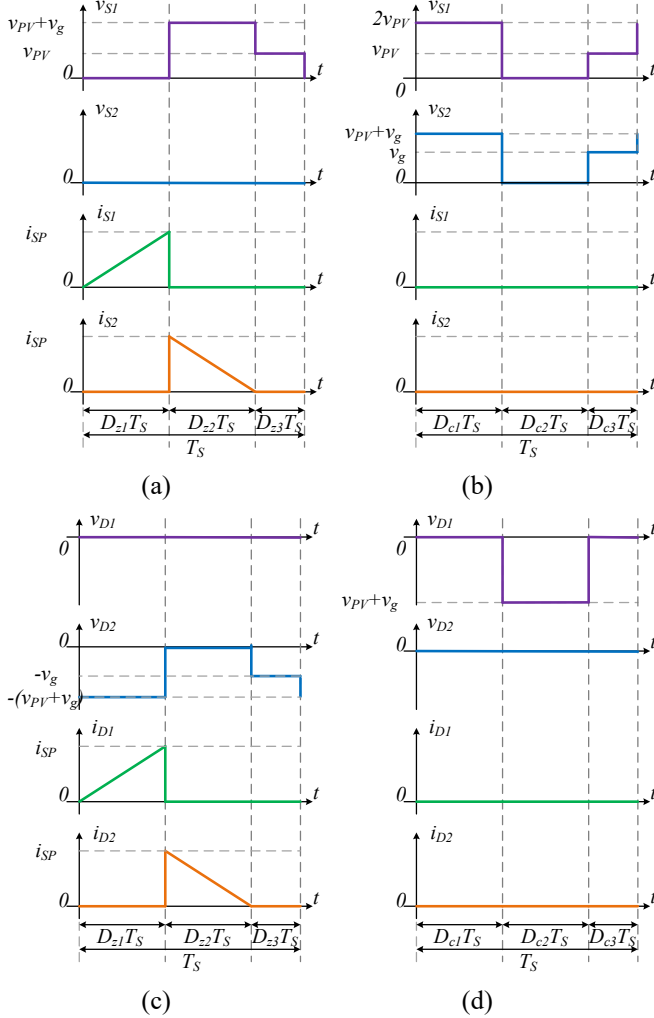


Fig. 5. Theoretical waveforms for the HIZC during a switching period: (a) S_1 and S_2 switches during the grid positive half-cycle; (b) S_1 and S_2 switches during the grid negative half-cycle; (c) D_1 and D_2 diodes during the grid positive half-cycle; (d) D_1 and D_2 diodes during the power grid negative half-cycle.

The voltage across the coupling capacitors C_1 and C_2 presents distinct values. The C_1 voltage is near the grid voltage, introducing a high-frequency ripple, while the voltage across the capacitor C_2 exhibits the grid voltage with an offset of the PV array voltage. Therefore, the average, RMS, and maximum voltages for the capacitor C_2 are higher than the C_1 .

The output capacitor C_o acts by filtering the high-frequency ripple. Thus, the voltage across this capacitor is almost the utility grid voltage.

All inductors present the same voltage during each operation stage if the voltage ripples are neglected. Each switching period

is divided into three subintervals, where during the first, the voltage is the same, independent of the grid voltage condition. The voltage across all inductors during the second subinterval is approximately the power grid voltage, and during the third subinterval, the voltages across all inductors are ideally zero. Fig. 8 shows voltages across the capacitors and inductors.

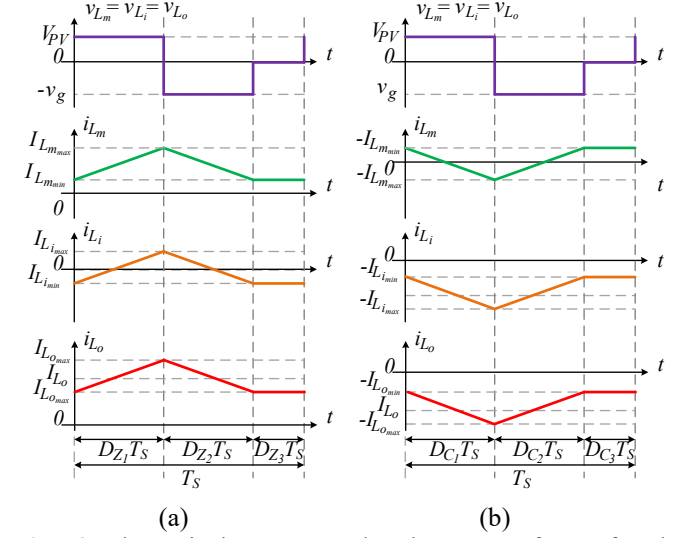


Fig. 6. Theoretical current and voltage waveforms for the inductors of the HIZC during a switching period: (a) During the positive power grid half-cycle; (b) During the negative power grid half-cycle.

If the input and magnetization inductance are the same, both inductors will have equal current ripples. Thus, the magnetization inductor L_m also presents the highest ripple at the peak of the grid voltage, exhibiting a sinusoidal shape during the positive half-cycle.

On the other hand, the current through the output inductor L_o presents a sinusoidal shape with a low ripple at high frequency caused by the switching. Fig. 7 (b) shows the current waveforms for the three inductors for the HIZC.

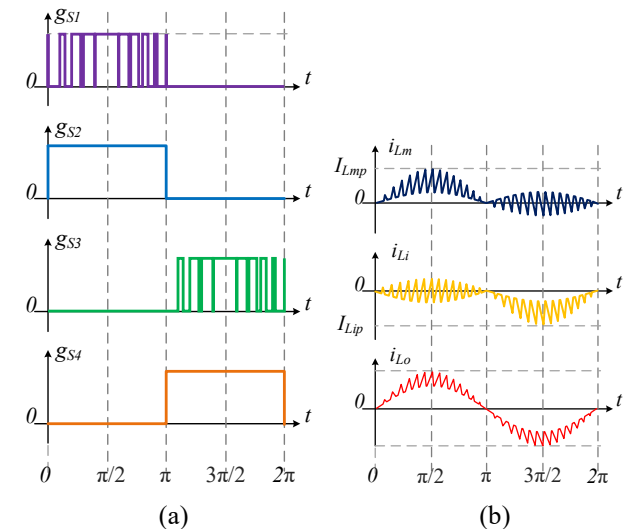


Fig. 7. Theoretical waveforms for the HIZC during a period of the utility power grid: (a) Gate signals; (b) Inductors currents.

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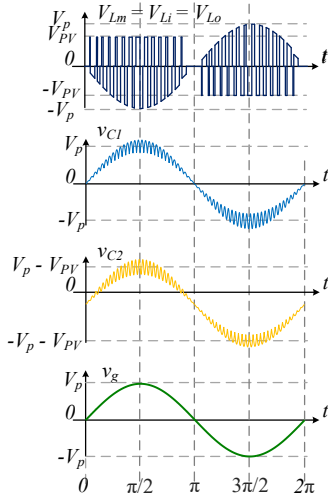


Fig.8. Theoretical voltage waveforms for the HIZC during a period of the utility power grid.

D. Main Equations and Static Gain

This section presents the main equations related to the steady-state analysis in order to obtain the HIZC static gain. Hence, by analyzing the HIZC operation mentioned in Section II. A and II.B, the equations are derived for a single switching period.

As is well-known, the average inductor voltage is null in a steady state. Thus, analyzing the voltage across the L_m inductor in Zeta mode, the following relation is obtained:

$$v_{Lm} = v_{PV}D_{z1} - v_{C1}D_{z2} + (v_{PV} + v_{C1} - v_{C2} + v_{Li})D_{z3} = 0. \quad (1)$$

The voltage across the inductor L_i , in the Zeta mode, is given as:

$$v_{Li} = (v_{C2} - v_{C1})D_{z1} + (v_{PV} - v_{C2})D_{z2} + (v_{PV} + v_{C1} - v_{C2} + v_{Lm})D_{z3} = 0. \quad (2)$$

The output inductor, L_o , presents the average voltage related by:

$$v_{Lo} = (v_{PV} + v_{C1} - v_g)D_{z1} - v_gD_{z2} + (v_{C1} - v_g + v_{Lm})D_{z3} = 0. \quad (3)$$

Some relations are established when equating (1)-(3), such as the voltage relation $v_{C2} = v_{C1} + v_{PV}$. The average voltage across the coupling capacitor C_2 is higher than the C_1 voltage. This response is expected because of characteristics from the Zeta and Ćuk converters. The C_1 average voltage during each switching period is near the grid voltage, $v_{C1} = v_g$.

Evaluating the voltages during the third operation stage, $D_{z3}T_s$, the sum of the L_m and L_i is an equal relation between the PV array voltage and the coupling capacitors voltages, $v_{Lm} + v_{Li} = v_{PV} + v_{C1} - v_{C2}$. As mentioned before, $v_{C2} = v_{PV} + v_{C1}$, resulting in $v_{Lm} + v_{Li} = 0$. Additionally, during this operation stage, the voltage across the output inductor can be expressed using the

L_m or L_i voltage. Thus, the voltages across the three inductors are ideally null in the third operation stage.

Considering the null voltage during the third operation stage, from (1), the HIZC static gain is obtained as per:

$$G_s = \frac{v_g}{v_{PV}} = \frac{D_{z1}}{D_{z2}}. \quad (4)$$

According to the indicated voltages, all inductors are charged and magnetized with nearly the PV-array voltage during the first operation stage, reaching the maximum value at the end of the first operation stage, $D_{z1}T_s$.

During the first operation stage, the current through switch S_I is the sum of the three inductors' currents. In the second operation stage, the current through semiconductors starts at the maximum value and decreases to zero. Thus, the current peak in semiconductors is obtained as follows:

$$i_{SP} = v_{PV}D_{z1}T_s \left(\frac{1}{L_m} + \frac{1}{L_i} + \frac{1}{L_o} \right) = \frac{v_{PV}D_{z1}T_s}{L_{eq}}, \quad (5)$$

where L_{eq} is the parallel association between the three HIZC inductances.

The switch S_I presents current only during the first operation stage. Thus, its average current can be determined as follows:

$$i_{Sav} = \frac{v_{PV}D_{z1}^2T_s}{2L_{eq}}. \quad (6)$$

[16] presents an approach to modeling the system in which the available power in the converter's input transfers to the switch when it is commuted on. An effective resistance, R_e , processes this power. The effective resistance for the HIZC topology, using (6), is calculated as per:

$$R_e = \frac{v_{PV}}{i_{Sav}} = \frac{2L_{eq}}{D_{z1}^2T_s}. \quad (7)$$

Disregarding the power losses, the input power is equal to the output power. Thereby, the available energy in the PV array is injected into the power grid as a sinusoidal and controlled current. The ideal power balance is related as follows:

$$P_{in} = P_{out} = \frac{v_{PV}^2}{R_e} = \frac{v_g^2 P_{out}}{v_g^2}. \quad (8)$$

The HIZC maximum static gain is obtained considering the inverter operation at the peak voltage of the utility grid, V_p . Hence, by manipulating (7) and (8), the static gain is determined as follows:

$$G_s = \frac{V_p D_{z1}}{\sqrt{4L_{eq}P_{out}f_s}}, \quad (9)$$

where f_s is the HIZC switching frequency, and V_p is the voltage peak of the utility grid. From (4) and (9), the subinterval D_{z2} is calculated as:

$$D_{z2} = \frac{\sqrt{4L_{eq}P_{out}f_s}}{V_p}. \quad (10)$$

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The same analysis can be performed for the Ćuk mode, which generates the same results. This equality between Zeta and Ćuk modes is necessary for the HIZC correct operation.

E. Average and RMS Current Equations

Due to the DCM characteristics, RMS current values are higher when compared with the CCM operation for the same power rate. However, the efficiency of a converter operating in DCM can be as high as that of a converter operating in CCM or higher once other characteristics improve the efficiency, such as the zero current switching (ZCS), intrinsic in DCM operation [17].

Analyzing a utility grid period, inductors L_m and L_i present the same average and RMS values. The computing of the average current through these inductors using a half-cycle of the power grid is found as:

$$I_{Lm, i_{av}} = \frac{I_1 + I_2}{8\pi V_p}, \quad (11)$$

where V_p is the peak of the utility grid, I_1 and I_2 are calculated as follows:

$$I_1 = \left(\frac{2V_{PV}D_{z1}T_s}{L_m} - I_{Lomin} \right) \pi D_{z1} V_p - I_{Lomin} \pi D_{z1} V_p. \quad (12)$$

$$I_2 = -8I_{Lomin}(V_p - V_p D_{z1} - V_{PV} D_{z1}). \quad (13)$$

The quantity I_{Lomin} is the lowest value for the output inductor at the voltage peak of the power grid and can be expressed by:

$$I_{Lomin} = \frac{2P_{out}}{V_p} - \frac{v_{PV}D_{z1}T_s(D_{z1} + D_{z2})}{2L_o}. \quad (14)$$

The integral for each period obtains the RMS value for the current through the input and magnetization inductors expressed as follows:

$$I_{Lm, i_{rms}} = \frac{2}{3} \sqrt{\frac{I_3 + I_4 + I_5}{L_m^2 \pi}}, \quad (15)$$

where

$$I_3 = \frac{24\pi T_s^2 V_{PV}^3 D_{z1}^3 - 18I_{Lomin} L_m \pi T_s V_{PV}^2 D_{z1}^2}{V_p}, \quad (16)$$

$$I_4 = 36T_s^2 V_{PV}^2 D_{z1}^3 - 48I_{Lomin} L_m T_s V_{PV} D_{z1}^2, \quad (17)$$

$$I_5 = 9I_{Lomin}^2 L_m^2 \pi. \quad (18)$$

Using the peak current for the semiconductors (5), the respective average and RMS currents through the switches S_1 and S_3 that occur only during the first operation stage (D_{z1} and D_{c1}), can be obtained as follows:

$$I_{S1,3,av} = \frac{D_{z1} i_{SP}}{8}, \quad (19)$$

$$I_{S1,3,rms} = \frac{\sqrt{2}}{3} \sqrt{\frac{D_{z1}(I_6 + I_7 + I_8)}{L_m^2 \pi}}, \quad (20)$$

where:

$$I_6 = D_{z1} T_s V_{PV} (4D_{z1} T_s V_{PV} + 3I_{Lomax} L_m), \quad (21)$$

$$I_7 = 3I_{Lomax}^2 L_m^2 - D_{z1} T_s V_{PV} (6I_{Lomin} L_m), \quad (22)$$

$$I_8 = 3I_{Lomin}^2 L_m^2 - 6I_{Lomax} I_{Lomin} L_m^2. \quad (23)$$

Similarly, during a utility power grid period, the average and RMS currents for the switches S_2 and S_4 can also be achieved using (5), as follows:

$$I_{S2,4,av} = \frac{V_{PV} D_{z1} i_{SP}}{2\pi V_p}, \quad (24)$$

$$I_{S2,rmsCA} = \frac{\sqrt{3}}{6} \sqrt{\frac{V_{PV} D_{z1} (I_6 + I_7 + I_8)}{L_m^2 \pi V_p}}. \quad (25)$$

III. MODELING AND CONTROL

This section introduces the main small-signal equations related to the dynamic system operation to provide bases for obtaining the HIZC transfer functions.

A. Control Design

The control of the HIZC aims to perform the power transference from the PV array to the utility grid through a sinusoidal and synchronized active current, harvesting the maximum available PV array power.

The HIZC is synchronized to the power grid by an adaptive filter AF- $\alpha\beta$ -pPLL, which obtains the angle of the utility grid (θ) used in a sine function. The AF- $\alpha\beta$ -pPLL is based on the instantaneous active power theory and designed to operate with voltage disturbances, such as sags and frequency variations, according to the results obtained in [18].

The P&O algorithm is used to perform the MPPT. Initially, the PV array voltage and current are measured to calculate the voltage reference (v_{PV}^*), which is used to reach the maximum power.

The P&O causes small perturbances on the voltage reference and analyzes whether there is an improvement or decrement in the PV array voltage and power. Thus, the P&O updates the voltage reference [19-22].

A Proportional-Integral (PI) controller compares the reference to the PV-array voltage. This control generates a current peak (I_p) multiplied by a synchronized sine vector, resulting in the current reference.

An inner PI controller compares the reference current to the output inductor current (i_{Lo}). The PI response multiplied by a PWM gain (K_{PWM}) generates a duty cycle (d) combined with a switching logical control, which drives the power switches. The switching logic uses the PLL information to determine if the switches S_1 and S_2 operate (Zeta mode) or S_3 and S_4 (Ćuk mode) Fig. 9 (a) shows the block diagram, and Fig. 9 (b) represents the adopted switching logic.

B. Equivalent Circuit

The HIZC topology operates similarly to the Zeta and the Ćuk converters. In each switching period, only two switches and two diodes present current. However, the current flows in

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all passive components during both modes. Two equivalent circuits can be obtained, the first for the operation like the Zeta converter and another for the Ćuk.

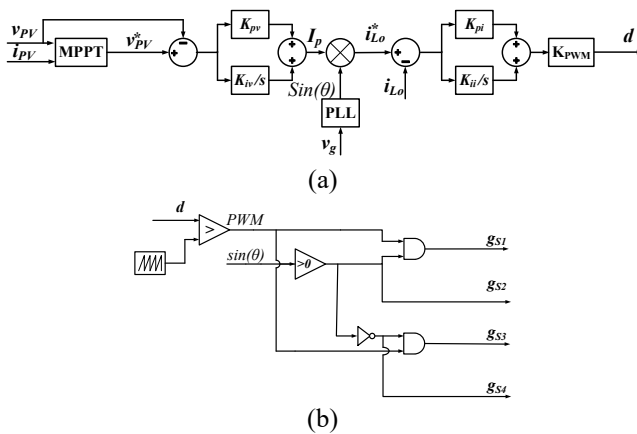


Fig. 9. Control structure: (a) Block diagram; (b) Switching control logic.

As mentioned before, the three stages of the operation for the Zeta and Ćuk modes are equivalent. By the topology design, the magnetization and demagnetization of the inductors L_m and L_i present the same intensity. Thus, the HIZC modeling can be simplified using an equivalent circuit from the Zeta or one other from the Ćuk mode. The response from both equivalent circuits must be similar to guarantee the adequate operation of the HIZC.

A representation of the inductors L_m and L_i is employed in the equivalent circuits and named L_e , calculated by the parallel association of the L_m and L_i inductors, $L_e = (L_m + L_i)/L_m L_i$. Additionally, these inductances present the same value so that the L_e inductance can be expressed as $L_e = L_m/2 = L_i/2$.

The coupling capacitors, C_1 and C_2 , also present current flow during the entire HIZC operation. Thus, an equivalent capacitance, named C_a , is adopted. This capacitance is the parallel association between C_1 and C_2 , $C_a = C_1 + C_2$. Fig. 10 (a) represents the Zeta mode equivalent circuit, and Fig. 10 (b) represents the Ćuk mode.

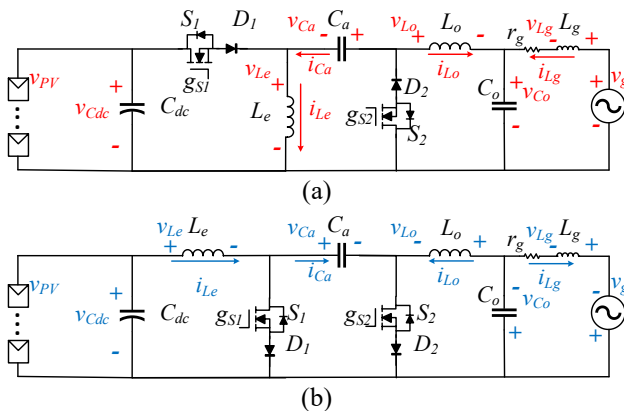


Fig. 10. Equivalent circuit: (a) Zeta mode; (b) Ćuk mode.

C. Inner Loop Modeling

State-space averaging (SSA) is widely employed in modeling linear systems. Commonly, the currents through inductors and the voltages across capacitors are chosen as state

variables in electrical systems, while the voltages and current sources are adopted as system inputs [23].

Static converters can be modeled using the SSA method in both CCM and DCM operation modes. When a static converter operates in CCM, the SSA presents a satisfactory representation, where each subinterval has its matrices related, and the average model is quickly obtained from the pondered meaning. On the other hand, when a static converter operates in DCM, the pondered meaning in the SSA method presents errors caused by the differences between the RMS and average values, mainly in the inductors' currents.

In [24], a correction matrix called M adequates the state's matrix, presenting good results for second-order converters, such as Buck, Boost, and Buck-Boost. However, the approach presented in [24] is inadequate for fourth-order converters. On the other hand, [17] proposes a generalized method for fourth-order power converters, which is used in [9] to model an integrated inverter based on Zeta topology. This approach results in good modeling for fourth-order converters, such as Zeta, Ćuk, and SEPIC. Thus, the proposed HIZC can be modeled similarly.

Using the correction approach for DCM operation and the SSA method initially, the modeling of the HIZC is described as per:

$$\dot{\bar{x}} = M A_m \bar{x} + B_m \bar{u}, \quad (26)$$

$$y = C \bar{x}. \quad (27)$$

The vector $\bar{x}$ represents the average states variables (inductors currents and capacitor voltages), A_m is the average states matrix during the three operation stages, B_m is the average input matrix, and $\bar{u}$ vector represents the input system, in this case, PV array and utility grid voltages.

The M matrix is expressed as [17]:

$$M = \begin{bmatrix} \frac{1-D_b}{D_a} & 0 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 & 0 \\ 0 & 0 & 1 & 0 & 0 \\ 0 & 0 & 0 & 1 & 0 \\ 0 & 0 & 0 & 0 & 1 \end{bmatrix}. \quad (28)$$

From the HIZC equivalent circuit during Zeta mode [see Fig. 8 (a)] and its operation presented in Section II and in Fig. 1 and Fig. 3, the SSA model considering the correction approach is determined as follows:

$$\begin{bmatrix} \dot{\bar{i}}_{Le} \\ \dot{\bar{i}}_{Lo} \\ \dot{\bar{v}}_{Ca} \\ \dot{\bar{v}}_{Co} \\ \dot{\bar{i}}_{Lg} \end{bmatrix} = \begin{bmatrix} 0 & 0 & a_{13} & \frac{D_{z3}}{L_e + L_o} & 0 \\ 0 & 0 & a_{23} & a_{24} & 0 \\ \frac{D_{z2} - D_{z2}^2}{C_a D_a} & \frac{D_{z2} - 1}{C_a} & 0 & 0 & 0 \\ 0 & \frac{1}{C_o} & 0 & 0 & \frac{-1}{C_o} \\ 0 & 0 & \frac{1}{L_g} & 0 & \frac{-r_g}{L_g} \end{bmatrix} \begin{bmatrix} \bar{i}_{Le} \\ \bar{i}_{Lo} \\ \bar{v}_{Ca} \\ \bar{v}_{Co} \\ \bar{i}_{Lg} \end{bmatrix}$$

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$$+ \begin{bmatrix} \frac{D_{z1}}{L_e} & 0 \\ \frac{D_{z1}}{L_o} & 0 \\ 0 & 0 \\ 0 & 0 \\ 0 & \frac{-1}{L_g} \end{bmatrix} \begin{bmatrix} \bar{v}_{PV} \\ \bar{v}_g \end{bmatrix}, \quad (29)$$

$$y = [0 \quad 1 \quad 0 \quad 0 \quad 0] \begin{bmatrix} \bar{i}_{Le} \\ \bar{i}_{Lo} \\ \bar{v}_{Ca} \\ \bar{v}_{Co} \\ \bar{i}_{Lg} \end{bmatrix}, \quad (30)$$

where y represents the output vector; $a_{13} = \frac{-(L_e+L_o)D_{z1}-L_eD_{z3}}{L_e(L_e+L_o)}$, $a_{23} = \frac{(L_e+L_o)D_{z1}-L_oD_{z3}}{L_o(L_e+L_o)}$, and $a_{24} = \frac{-(D_{z1}+D_{z2})(L_e+L_o)-L_oD_{z3}}{L_o(L_e+L_o)}$.

If the converter acts in CCM, the third subinterval is eliminated. However, eliminating this operation stage (29) will be adequate for the average model, and (30) will not be altered.

When HIZC acts in the Ćuk mode, its functionality is equivalent to the Zeta mode. The average voltage across the capacitor C_a is distinct because of characteristics from the Zeta and Ćuk converters. The other states' variables and inputs are unaltered.

In the equivalent circuit of the Zeta mode, the PV array supplies energy for HIZC only during the first operation stage. However, in the equivalent circuit of the Ćuk mode, the PV array provides energy for HIZC during the whole structure functionality. Thus, each case's input matrix, B_m , must be distinct.

Equalizing the operation stages, i.e., $D_{z1}T_s = D_{c1}T_s$, $D_{z2}T_s = D_{c2}T_s$, and $D_{z3}T_s = D_{c3}T_s$, and using the equivalent circuit for this mode [see Fig. 10(b)], a SSA representation can be found as follows:

$$\begin{bmatrix} \dot{\bar{i}}_{Le} \\ \dot{\bar{i}}_{Lo} \\ \dot{\bar{v}}_{Ca} \\ \dot{\bar{v}}_{Co} \\ \dot{\bar{i}}_{Lg} \end{bmatrix} = A_m \begin{bmatrix} \bar{i}_{Le} \\ \bar{i}_{Lo} \\ \bar{v}_{Ca} \\ \bar{v}_{Co} \\ \bar{i}_{Lg} \end{bmatrix} + \begin{bmatrix} b_{11} & 0 \\ \frac{D_{c3}}{L_o} & 0 \\ 0 & 0 \\ 0 & 0 \\ 0 & \frac{-1}{L_g} \end{bmatrix} \begin{bmatrix} \bar{v}_{PV} \\ \bar{v}_g \end{bmatrix}, \quad (31)$$

where $b_{11} = \frac{(D_{c1}+D_{c2})(L_e+L_o)+D_{c3}L_e}{L_e(L_e+L_o)}$

The A_m matrix is the same in both HIZC modes, resulting in the same poles from (29) and (31). This conclusion indicates that Zeta and Ćuk modes have similar dynamics and comportment.

[16] proposed a generalized switch averaging (GSA) for modeling DCM converters. The GSA approach divides the converter into two subsystems: i) one linear, formed by the passive elements, which can be represented for the SSA model; ii) one non-linear, formed by the semiconductors.

[9] models an integrated inverter based on a Zeta converter for grid-tied applications using this association, presenting a high similarity between the mathematical model and a simulated circuit.

The non-linear subsystem obtains three gains: one for the duty cycle, one for the voltage across the switch, and another for the diode current [16]. In the HIZC, the voltage across the switch is considered the voltage across the association of S_l and D_l . For the current diode, the current is adopted through the diode D_2 . The three gains are presented as follows:

$$k_c = \frac{2D_{z2}}{(D_{z1}+D_{z3})^2}, \quad (32)$$

$$k_{vs} = \frac{D_{z1}D_{z2}}{v_{PV}(D_{z1}+D_{z3})^2}, \quad (33)$$

$$k_{id} = \frac{-R_eD_{z1}^2}{v_{PV}(D_{z1}+D_{z3})^2}. \quad (34)$$

The transfer function that relates the output inductor, L_o , to the duty cycle for the HIZC topology is determined as follows:

$$G_{id}(s) = \frac{i_{Lo}(s)}{\bar{d}(s)} = C \left(s - MA_m + \frac{B_d k_s M C_m}{1 - k_s E_d} \right)^{-1} \frac{B_d k_c}{1 - k_s E_d}, \quad (35)$$

where $k_s = [k_{id} \ k_{vs}]$, and the matrices B_d and E_d are defined as follows:

$$E_d = \left[C_1 - \frac{D_{z2}}{1-D_{z1}} C_2 - \frac{D_{z3}}{1-D_{z1}} C_3 \right] \begin{bmatrix} \bar{i}_{Le} \\ \bar{i}_{Lo} \\ \bar{v}_{Ca} \\ \bar{v}_{Co} \\ \bar{i}_{Lg} \end{bmatrix} + \left[E_1 - \frac{D_{z2}}{1-D_{z1}} E_2 - \frac{D_{z3}}{1-D_{z1}} E_3 \right] \begin{bmatrix} \bar{v}_{PV} \\ \bar{v}_g \end{bmatrix}, \quad (36)$$

$$B_d = \left[A_1 - \frac{D_{z2}}{1-D_{z1}} A_2 - \frac{D_{z3}}{1-D_{z1}} A_3 \right] \begin{bmatrix} \bar{i}_{Le} \\ \bar{i}_{Lo} \\ \bar{v}_{Ca} \\ \bar{v}_{Co} \\ \bar{i}_{Lg} \end{bmatrix} + \left[B_1 - \frac{D_{z2}}{1-D_{z1}} B_2 - \frac{D_{z3}}{1-D_{z1}} B_3 \right] \begin{bmatrix} \bar{v}_{PV} \\ \bar{v}_g \end{bmatrix}, \quad (37)$$

where the matrices A_1, A_2, A_3, B_1, B_2 , and B_3 are the states' and inputs' matrices for the SSA during the three operation stages $D_{z1}T_s, D_{z2}T_s$, and $D_{z3}T_s$. Matrices C_1, C_2 , and C_3 are the output matrices for the GSA, while E_1, E_2 , and E_3 are the direct transition matrices. The matrix C_m is obtained by the operation averaging, i.e., $C_m = C_1D_{z1} + C_2D_{z2} + C_3D_{z3}$.

Using the modeling of the equivalent circuit for the Ćuk mode gets a close response. The transfer function exhibits the same structure shown in (20), with only some distinct matrices.

The high similarity between both models is corroborated by plotting the frequency response for the transfer functions and the switched converter, as demonstrated in Fig. 11.

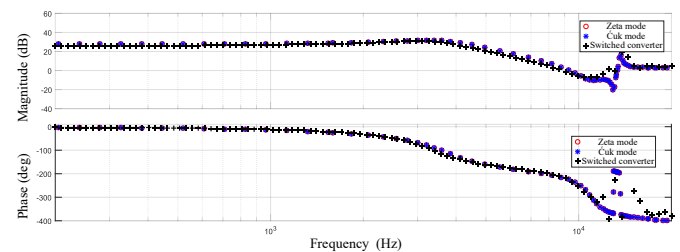


Fig. 11. Frequency responses for nominal operating values.

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D. Components design

The design of the passive elements guarantees that the HIZC operates correctly and in DCM. The output inductor presents a low ripple and can be projected as the output inductor for the Zeta or Ćuk conventional converter operating in CCM.

$$L_o = \frac{V_{PV} D_{z1} T_s}{\Delta I_{Lop} I_{Lop}} \quad (38)$$

where I_{Lop} is the current through the output inductor during the peak of the power grid.

The inductor project guarantees the HIZC operation into DCM, and each inductance can be limited to:

$$L_{m,i} < \frac{2V_{PV} L_o (1 - 2D_{z1} + D_{z1}^2)}{4P_{out} L_o f_s - V_p^2 (1 - 2D_{z1} + D_{z1}^2)} \quad (39)$$

The output capacitor acts as a filter, and its project is equal to conventional converters such as Buck, Ćuk, SEPIC, and Zeta converters.

$$C_o = \frac{\Delta I_{Lop} I_{Lop}}{8f_s \Delta V_{C_o} V_{C_o}} \quad (40)$$

The coupling capacitors can be determined by the resonance formed between these capacitors and inductors. A range of capacitances can be determined using two distinct frequencies defined as one decade above the power grid frequency and another defined as one decade below the switching frequency.

$$\frac{1}{2(0.2\pi f_s)^2 (L_e + L_o)} < C_{1,2} < \frac{1}{2(20\pi f)^2 (L_e + L_o)} \quad (41)$$

where f is the power grid frequency.

IV. EXPERIMENTAL RESULTS

The HIZC prototype processes 432 W and uses SiC MOSFETs IPW65R037C6 (Infineon), SiC Schottky diodes FFSP2065B-F085 (OnSemi). Gate drivers DRO100S25A (Supplier) commute the MOSFETs. MPPT algorithm, PLL, and controllers are embedded into a DSP TMS320F28335 (Texas Instruments). A controlled source, ITC6012C-800-50 (Itech), emulates the PV array under different climate conditions, generating the PV curves. The digital oscilloscope RTH1004 (Rohde&Schwarz) obtains the results. The Power Quality Analyzer 43B (Fluke) measures the power factor (PF) and the total harmonic distortion (THD). The Precision Power Analyzer WT3000 (Yokogawa) calculates the HIZC efficiency. Fig. 12 shows the HIZC prototype. A small RC ($R = 100 \Omega$ and $C = 1.5 \text{ nF}$) circuit is employed in parallel to each switch to avoid problems with spike voltages.

A. Waveforms

The emulated PV array uses three irradiance conditions: the first at 500 W/m^2 , the second at Standard Test Conditions (STC: 1000 W/m^2), and the third at 750 W/m^2 , the test temperature was kept at 25°C .

The harvested power from the PV array, the current, and the voltage PV array are presented in Fig. 13.

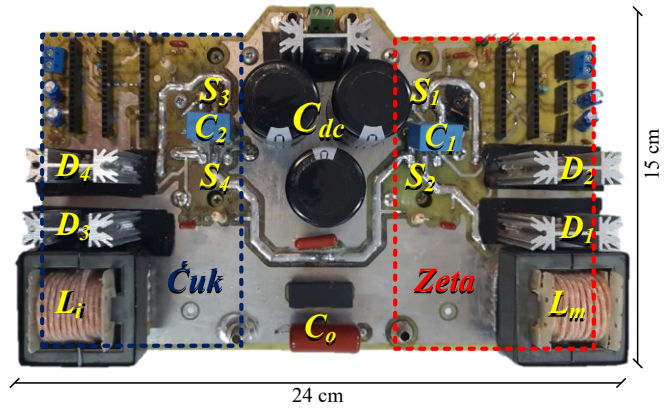


Fig. 12. HIZC prototype.

These results present a low-frequency oscillation, 120 Hz, in the current and, consequently, in the power. Fig. 14 shows in detail these oscillations. However, these oscillations are not transferred to the output current. The PV-array voltage remains near the V_{MPP} described in Table I.

Table I organizes the main parameters used in the experimental tests using the HIZC topology.

TABLE I
MAIN HIZC PARAMETERS

Parameter	Value
The nominal utility RMS voltage	$V_o = 127 \text{ V}$
Nominal utility frequency	$f = 60 \text{ Hz}$
Switching frequency	$f_s = 50 \text{ kHz}$
Sampling frequency A/D converter	$f_a = 60 \text{ kHz}$
Input DC-Bus capacitance	$C_{dc} = 4500 \mu\text{F}$
Input inductive filter	$L_m = L_i = 105 \mu\text{H}$
Output inductive filter	$L_o = 1.5 \text{ mH}$
Coupling capacitances	$C_1 = C_2 = 1.0 \mu\text{F}$
Output capacitance	$C_o = 1.5 \mu\text{F}$
Nominal Power	$P = 432 \text{ W}$
Inner PI controller gains	$K_{pi} = 13.3757;$ $K_{ii} = 1.0756 \times 10^6$
Outer PI controller gains	$K_{pv} = 0.0843;$ $K_{iv} = 2.1856$
PWM Gain	$1/2999$
Phase margin of the inner current control	$f_{ei} = 72.1^\circ$
Crossover frequency of the inner current control	$P_{mi} = 1620 \text{ Hz}$
Phase margin of the outer current control	$f_{eo} = 5 \text{ Hz}$
Crossover frequency of the outer current control	$P_{mo} = 88^\circ$
PLL PI controller gains	$K_{PPLL} = 423.4;$ $K_{IPLL} = 32234$
Adaptive filter step size parameter (AF-pPLL)	$\mu_{AF} = 0.007$
Sampling time (AF-pPLL)	$f_{smp} = 60 \text{ kHz}$
Adaptive filter gain (AF-pPLL)	$K_{AF} = 420$
MPP voltage	$V_{MPP} = 139.2 \text{ V}$
MPP current	$I_{MPP} = 3.11 \text{ A}$
Open-circuit voltage	$V_{oc} = 173.6 \text{ V}$
Short-circuit current	$I_{SC} = 3.31 \text{ A}$
P&O frequency	5 Hz

Fig. 13 and Fig. 14 present values near to expected in Table I. According to Table I, the PV-array voltage remains near 139.2 V , which is the voltage in the maximum power available. It can be noted that the PV array current changes more significantly due to the irradiance. However, in STC, it presents values near the I_{MPP} .

The THD of the output current from the three irradiance scenarios demonstrates a maximum of around 4.6%, lower than

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the levels established in the main standards [25, 26], validating the development and employment of the HIZC as an interface inverter between the grid-tied and the PV array.



Fig. 13. Current, voltage, and power of the PV array.



Fig. 14. Detail of the current, voltage, and power of the PV array.

During the tests, the THD of the utility grid was measured, obtaining a value of 2.6%. Fig. 15 shows the THDs for current with the irradiances and for the voltage of the utility grid.

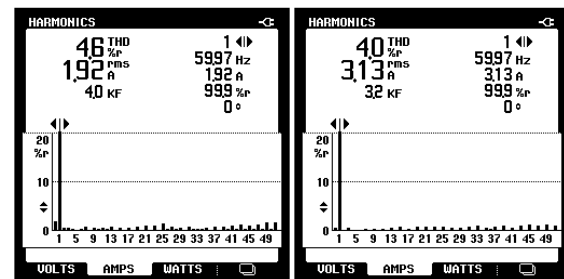
The irradiance induces changes of majority in the maximum current, consequently in the power available. The HIZC quickly updates the power levels caused by distinct irradiances.

The oscillations in the PV array side are not reflected in the current injected into the power grid. Fig. 16 presents the current and voltage utility grid for the three scenarios, where Fig. 16 (a) represents scenario I (500 W/m^2), Fig. 16 (b) shows scenario II (STC), and Fig. 16 (c) is related to scenario III (750 W/m^2). In Fig. 16, the current presents some distortion at the zero-crossing caused by the employed control, which needs to synthesize a duty-cycle near zero at these moments, turning hard the commutation by the gate-driver circuit.

The utilized PI control loop exhibits a fast dynamic response, adjusting the current injected into the power grid in a few cycles, as can be shown in Fig. 17. Fig. 17 (a) exhibits the current injected into the power grid when the irradiance is changed from 500 W/m^2 to 750 W/m^2 . In contrast, Fig. 17 (b) shows the dynamic of the injected current into the power grid when the irradiance on the PV-array changes from 750 W/m^2 to 500 W/m^2 .

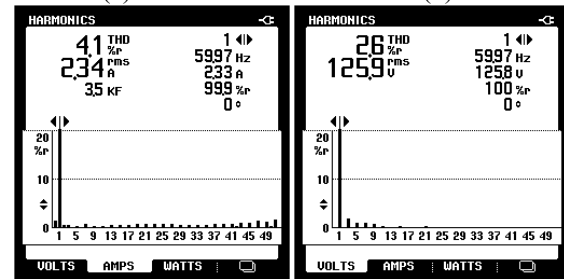
According to Section II, during the Zeta mode, the adopted control commutes the switch S_1 at a high frequency, while in the Ćuk mode, the commutation of the switch S_3 occurs at a high frequency. The maximum voltages across the MOSFETs are

relatively low, with each peak voltage near 350 V. Fig. 18 shows the voltages across the four power MOSFETs used on the HIZC.



(a)

(b)



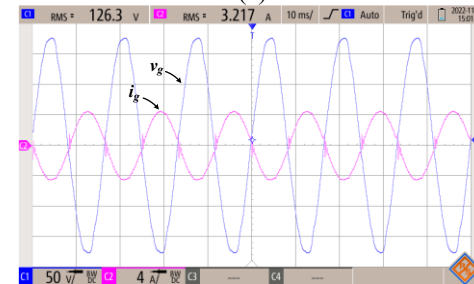
(c)

(d)

Fig. 15. THD: (a) Current in scenario 1; (b) Current in scenario 2; (c) Current in scenario 3, (d) Utility power grid voltage.



(a)



(b)



(c)

Fig. 16. Utility power grid voltage and current considering: (a) Scenario 1; (b) Scenario 2; (c) Scenario 3.

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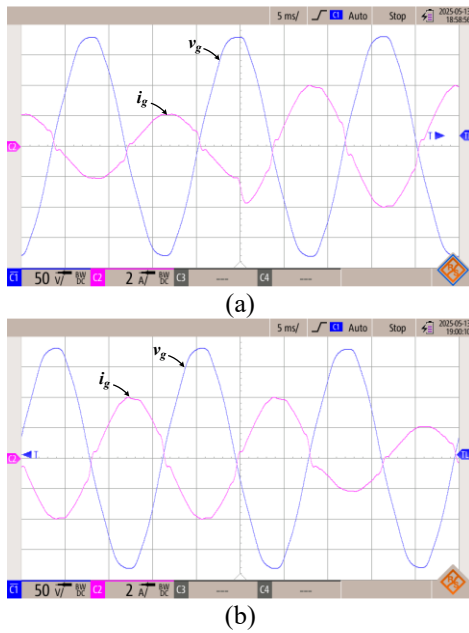


Fig. 17. Utility power grid voltage and current considering: (a) Transition from 500 W/m² to 750 W/m²; (b) Transition from 750 W/m² to 500 W/m².

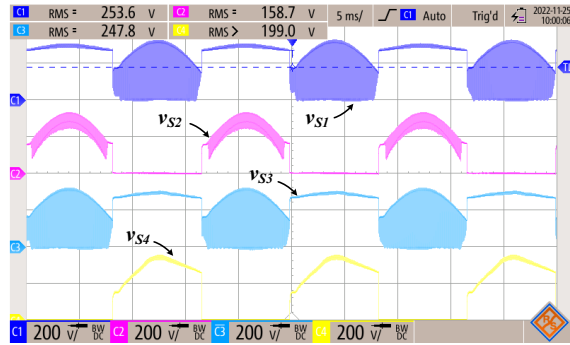


Fig. 18. Voltages across the switching power devices.

The experimental results for the current through inductors L_m and L_i show a good similarity with the theoretical waveshape presented in Fig. 7 (b), where during the Zeta mode the magnetization inductor presents the highest current peak. In contrast, during the Ćuk mode, the input inductor presents the lowest (more negative) current value. Fig. 19 presents the experimental current through the input and magnetization for the HIZC converter.

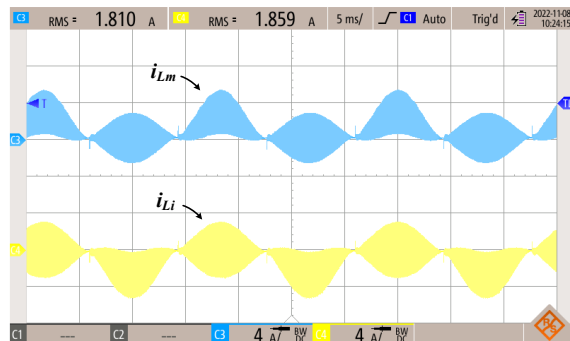


Fig. 19. Current through the inductors L_m and L_i .

The voltages across the capacitors C_o and C_l are ideally the same as the utility grid voltage. In contrast, the voltage across the capacitor C_2 exhibits the behavior of the coupling capacitor for a Ćuk, i.e., the ideal voltage for this capacitor is a combination of input and output voltages. In this case, the voltage across the capacitor C_2 combines the PV array and the grid voltages. Fig. 20 presents the voltages for the three capacitors employed in the HIZC and the output inductor current.

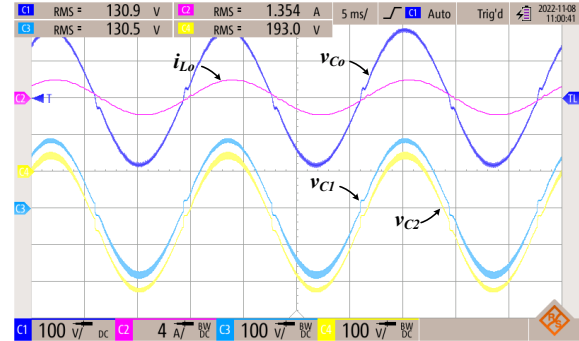


Fig. 20. Voltage across the capacitors C_o , C_l , and C_2 and current through the inductor L_o .

According to the earlier mentioned and Fig. 8, the voltages across all inductors employed in the HIZC present a good similarity and a waveform shape partly constant and partly sinusoidal. Fig. 21 (a) corroborates the theoretical analyses for a grid period, while Fig. 21 (b) proves the HIZC operation in DCM, where during a switching period, all inductors present three voltage levels, which are a positive, a negative, and in the third subinterval the voltage oscillates near to zero.

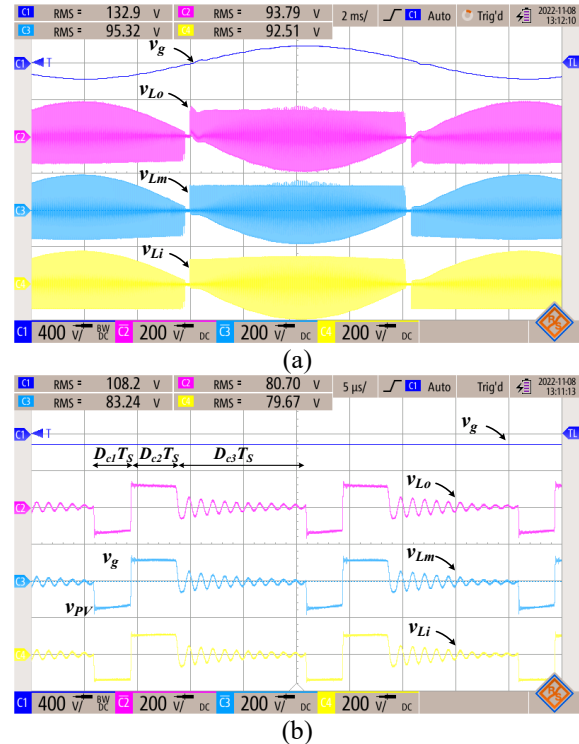


Fig. 21. Voltage across the inductors: (a) For a power grid period; (b) For a switching period.

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B. Efficiency

The HIZC efficiency is near 96% in the nominal power, employing SiC semiconductors. Fig. 22 presents efficiency curves for the HIZC, where the first is obtained for experimental measurements (red points), and the other one is estimated based on analytical estimation (green points). In low power, lower than 100 W, the efficiency values are close to 90%. In nominal power, the HIZC reaches the maximum efficiency, and the efficiency decreases for power higher than nominal power, which is second to the estimated efficiency.

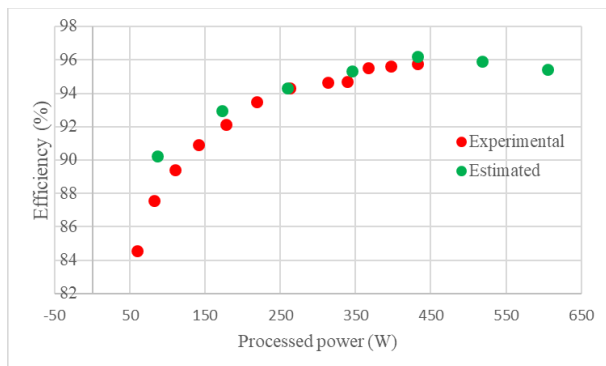


Fig. 21. HIZC experimental efficiency and comparison with the estimated efficiency.

Table II organizes the main characteristics of the HIZC operating in the nominal power. The average and RMS current parcels are obtained by (11)-(25). Additionally, the maximum voltage across the semiconductors, inductors' internal resistance, and the range of the duty cycles are presented.

TABLE II

MAIN HIZC CHARACTERISTICS AT THE NOMINAL POWER

Parameter	Value
Maximum duty cycles D_{z1} and D_{c1}	$D_{z1} = D_{c1} = 0.47$
Maximum duty cycles D_{z2} and D_{c2}	$D_{z2} = D_{c2} = 0.37$
Minimum duty cycles D_{z3} and D_{c3}	$D_{z2} = D_{c2} = 0.16$
Output inductor resistance	$r_{Lo} = 78.70 \text{ m}\Omega$
Magnetization inductor resistance	$r_{Lm} = 19.68 \text{ m}\Omega$
Input inductor resistance	$r_{Li} = 19.68 \text{ m}\Omega$
RMS magnetization inductor current	$i_{LmRMS} = 4.03 \text{ A}$
RMS input inductor current	$i_{LiRMS} = 4.03 \text{ A}$
RMS output inductor current	$i_{LoRMS} = 3.39 \text{ A}$
Maximum diodes D_1 and D_3 voltages	$V_{D1} = V_{D3} = 40 \text{ V}$
Maximum diodes D_2 and D_4 voltages	$V_{D2} = V_{D4} = 320 \text{ V}$
Semiconductor peak current	$i_{SP} = 26 \text{ A}$
Average S_1, D_1, S_3 , and D_3 currents	$i_{S1av} = i_{S3av} = 1.56 \text{ A}$
Average S_2, D_2, S_4 , and D_4 currents	$i_{S2av} = i_{S4av} = 1.53 \text{ A}$
RMS S_1, D_1, S_3 , and D_3 currents	$i_{S1RMS} = i_{S3RMS} = 4.83 \text{ A}$
RMS S_2, D_2, S_4 , and D_4 currents	$i_{S2RMS} = i_{S4RMS} = 4.83 \text{ A}$
Maximum switches S_1 and S_3 voltages	$V_{S1} = V_{S3} = 320 \text{ V}$
Maximum switches S_2 and S_4 voltages	$V_{S2} = V_{S4} = 320 \text{ V}$

Table III shows the characteristics of the semiconductors employed in the HIZC. The losses can be estimated using the parameters from Tables II and III with the knowledge of the HIZC operation.

Fig. 23 exhibits the main parcels of losses in the HIZC topology. The conduction losses for the power switches S_1 and S_3 represent 13% of the total losses, with a value of 2.20 W. The

commutation losses for switches S_1 and S_3 present a value of 1.80 W, 11%. Losses related to switches S_2 and S_4 , present only conduction losses, with a value of 1.97 W, 12%. Using the SiC MOSFETs, the conduction losses for the HIZC are higher than the conduction losses.

TABLE III

SEMICONDUCTORS CHARACTERISTICS EMPLOYED

Parameters	Values
Forward D_1, D_2, D_3 , and D_4 voltages	$V_f = 1.2 \text{ V}$
ON D_1, D_2, D_3 , and D_4 resistances	$R_{on} = 46.15 \text{ m}\Omega$
Capacitance charges for D_2 and D_4	$Q_c = 50 \text{ nC}$
ON S_1, S_2, S_3 , and S_4 resistances	$R_{dson} = 37 \text{ m}\Omega$
Rise time	$R_t = 32 \text{ ns}$
Fall time	$F_t = 7 \text{ ns}$

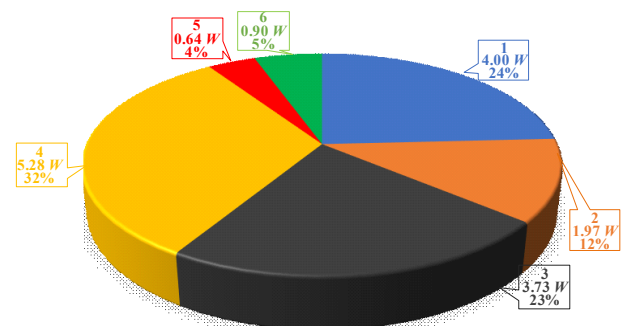


Fig. 23. Losses distribution: 1 - Switches S_1 and S_3 ; 2 - Switches S_2 and S_4 ; 3 - Diodes D_1 and D_3 ; 4 - Diodes D_2 and D_4 ; 5 - Inductors L_m and L_i ; 6-Inductor L_o .

The diodes D_1 and D_3 together show the conduction losses as 3.74 W, 23% of the total losses, as can be observed in Fig. 23. The losses in diodes D_2 and D_4 are divided into conduction and switching losses. The conduction losses for diodes D_2 and D_4 are higher than their switching losses, showing a value of 3.68 W, 22% of the total, while the switching losses represent 1.60 W, 10%, as shown in Fig. 23.

Inductor losses are considered as the conduction losses on the windings and the core losses, represented by parcels 5 and 6 in Fig. 23, where parcel 5 illustrates the input inductor losses (L_m and L_i), and parcel 6 is related to the output inductor losses. For the input inductors, the total losses are 0.64 W, which is 4% of the total losses. Meanwhile, the output inductor exhibits 0.9 W, which is 5% of the total losses.

C. Comparison Between other Integrated Inverters

Considering other single-phase integrated inverters, Table IV compares the main parameters in each work. The works addressed in Table IV are single-phase, such as the HIZC, and present a processed power between 200 W and 500 W.

The topologies presented in [6] and [9] operate similarly to the proposed inverter. However, these papers do not give information about the efficiency. Furthermore, these papers use half of the PV voltage in each operation stage, which probably results in losses. The HIZC uses the total voltage.

The topologies in [5] and [29] employ a high-frequency transformer, where the transformer ratio directly affects the maximum voltages across the switches, needing a distinct power switch, which must be able to operate with elevated voltages.

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TABLE IV
COMPARATIVE ANALYSIS INVOLVING HIZC AND OTHER PV SYSTEMS

	[a]	[b]	[c]	[d]	[e]	[f]	[g]	[h]	[i]	[j]	[k]	[l]	[m]
HIZC	4	4	3	4	0	$V_{PV} + V_p$	432 W	139.6 V	50 kHz	127 V	60 Hz	4.0%	95.8%
[5]	5	0	1	3	1	$nV_{PV} + V_p$	300 W	40-50 V	50 kHz	220 V	60 Hz	1.7%	94.7%
[6]	4	4	3	4	0	$V_{PV} \left(2 + \frac{D_1}{D_2}\right)$	432 W	139.6 V	50 kHz	127 V	60 Hz	2.9%	-
[9]	4	4	3	5	0	$0.5V_{PV} + V_p$	432 W	139.6 V	50 kHz	127 V	60 Hz	3.1%	-
[14]	4	2	2	2	0	$2V_{PV} + V_p$	320 W	54 V	50 kHz	110 V	500 Hz	3.0%	94.0%
[27]	9	1	3	2	0	$> V_p$	220 W	70 V	20 kHz	56 V	50 Hz	2.9%	94.9%
[28]	7	3	5	6	0	$\frac{V_{PV}D(2-D)}{(1-D)^3}$	300 W	35 V	100 kHz	120 V	60 Hz	-	93.9%
[29]	5	1	3	3	1	$nV_{PV} + V_p$	500 W	60 V	40 kHz	220 V	60 Hz	2.0%	96.6%
[30]	5	0	2	1	0	$V_{PV} + V_p$	440 W	60 V	20 kHz	110 V	50 Hz	4.2%	96.0%
[31]	5	1	3	4	0	$> V_p$	110 W	34.8 V	20 kHz	36 V	50 Hz	-	88.6%

where: [a] number of switches; [b] number of diodes; [c] number of inductors; [d] number of capacitors; [e] high-frequency transformer; [f] semiconductors voltage stress; [g] nominal power; [h] input voltage; [i] switching frequency; [j] RMS output voltage; [k] output frequency; [l] THD; [m] efficiency.

The integrated inverter in [27] uses a voltage grid lower than the conventional. Additionally, the topology needs to employ a secondary DC input, and the sum of the DC inputs must be higher than the grid's peak.

Converters presented in [29] and [30] offer higher efficiency than the HIZC. [29] uses a topology based on the Ćuk inverter, which operates in CCM mode. However, the converter presented in [29] uses more switches than the HIZC, consequently, more gate drivers and communication circuits, which increases the topology cost. In [30], only the theoretical losses are presented. Thus, the experimental efficiency should be lower.

[31] investigates a double-stage single-phase grid-connected system, using a DC-DC converter cascaded with a full-bridge

inverter. The double-stage configuration presents the worst efficiency in Table IV, once the system efficiency is obtained by the product of the DC-DC converter and full-bridge efficiency, 90.9% and 97.5%, respectively.

Table V estimates the costs for each topology exhibited in Table IV. Table V shows the price per unit (pu), and the HIZC acts as the base for the costs, i.e., the cost for the HIZC assumes the unitary value and all the other converters are compared to the HIZC cost. The voltage and current measurement boards, besides the gate-driver circuits, were considered the same for each structure.

TABLE V
ESTIMATED COSTS INVOLVING HIZC AND OTHER PV SYSTEMS

	Capacitors	Inductors	Transformer	Diodes	Switches	Gate-drivers	Voltage sensors	Current sensors	total
HIZC	0.0345	0.0620	0.0000	0.0535	0.0987	0.2540	0.3617	0.1356	1.0000
[5]	0.0831	0.0869	0.0328	0.0000	0.1445	0.3810	0.3617	0.1356	1.2256
[6]	0.0664	0.0748	0.0000	0.0127	0.0350	0.2540	0.5425	0.1356	1.1209
[9]	0.0660	0.0406	0.0000	0.0127	0.0350	0.2540	0.5425	0.1356	1.0864
[14]	0.0049	0.1088	0.0000	0.0453	0.1248	0.2540	0.3617	0.1356	1.0351
[27]	0.0156	0.1440	0.0000	0.0153	0.1005	0.6349	0.5425	0.2034	1.6563
[28]	0.0379	0.0346	0.0000	0.0100	0.4247	0.5079	0.7233	0.1356	1.8740
[29]	0.0196	0.0454	0.0325	0.0136	0.1150	0.3810	0.3617	0.1356	1.1044
[30]	0.0010	0.0797	0.0000	0.0000	0.0558	0.3810	0.3617	0.1356	1.0148
[31]	0.0345	0.1959	0.0000	0.0134	0.1234	0.3810	0.5425	0.2034	1.4941

On the other hand, the capacitors, inductors, transformers, switches, and diodes consider the particularity of each work. Furthermore, when a semiconductor is obsolete, another semiconductor with similar characteristics is considered, e.g., the IGBT IGW40N60H3FKSA1 was used as an alternative to the IRGP4650D employed in [6] and [9].

Often, the inductors are built to guarantee the expected inductance for the current, voltage, and power required. Therefore, the estimated costs for the inductors are based on

the inductance and current since these parameters determine the core size and the quantity of wire used.

The inverter employed in [30] does not present information about the semiconductors employed. So, based on the inverter behavior and operation description, the switch IGW40N60H3FKSA1 and the diode 30ETH06 can be used for the cost estimations.

The inverters [27] and [28] present elevated costs due to the high component count, mainly switches and gate drivers

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associated. The inverter in [30] presents a low cost, but the semiconductors are assumed and may not reflect the same efficiency reported.

The costs of the double-stage configuration are high, and the system employs bulky inductors. The double-stage PV system needs three voltage sensors and three current sensors, which increases the costs compared to single-stage topologies, such as the HIZC.

V. CONCLUSIONS

This paper proposed a novel integrated inverter topology derived from a combination of Zeta and Ćuk modules, called Hybrid Inverter Zeta-Ćuk (HIZC). The topology presents two operation modes, one for the positive half-cycle and another for the negative, named Zeta and Ćuk modes.

The HIZC operates in discontinuous conduction mode (DCM), presenting three operation stages in each switching period, and more complex modeling than topologies operating in continuous conduction mode (CCM). The HIZC modeling has shown a great similarity between the switched converter, Zeta, and Ćuk modes, demonstrating the close dynamic between these modes.

The proposed HIZC topology was evaluated by experimental results, demonstrating high efficiency and the ability to inject a sinusoidal current (with low THD) into the power grid. In addition, the voltages across the power switches employed in the HIZC are reduced, contributing to the improvement of the overall system performance and safety operation.

Additionally, the linear characteristics of the HIZC allow a simple control strategy to be used, with only a few sensors required (two voltage sensors and two current sensors).

The HIZC uses only four PWM signals: two in a high frequency and two in a low frequency and complementary. Thus, the HIZC does not need complex commutation circuits for its operation.

Usually, a convex shape is expected for the efficiency of a converter, reaching a peak value near the nominal power and decreasing to higher power levels. The estimated efficiency shows that this behavior is expected for the HIZC. Furthermore, the DCM operation limits the processing power of the HIZC converter. When the power crosses the limit of the DCM operation, the converter is forced to operate in CCM. However, only in DCM operation, the HIZC presents a linear gain.

The comparative analysis involving the HIZC converter and others with similar characteristics, presented in the literature review, shows that the proposed converter is a good choice for grid-tied PV applications. In this way, the proposed inverter can advantageously replace conventional double-stage PV systems built by the cascade association of a step-up converter and a voltage source inverter.

Additionally, the HIZC presents the lowest estimated cost, even using SiC components, due to the small number of switches, consequently, fewer gate-driver circuits, and the small number of sensors, when compared to other topologies also used for operation as an interface converter between the PV array and the utility power grid.

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