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Power Supply and Distribution Unit Design for a Scientific Exobiology Facility in the ISS

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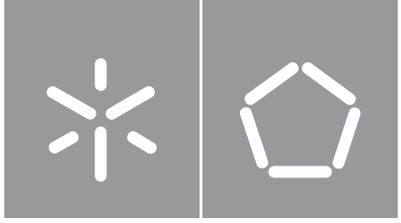
UMinho | 2022



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Power Supply and Distribution Unit Design for a Scientific Exobiology Facility in the ISS

Dissertação de Mestrado
Mestrado em Engenharia Eletrónica Industrial e Computadores
Instrumentação e Microssistemas Eletrónicos

Trabalho efetuado sob a orientação do
Professor Doutor Luís Miguel Valente Gonçalves
Rodolfo Manuel Maia da Cruz Martins

junho de 2022

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STATEMENT OF INTEGRITY

I hereby declare having conducted this academic work with integrity. I confirm that I have not used plagiarism or any form of undue use of information or falsification of results along the process leading to its elaboration.

I further declare that I have fully acknowledged the Code of Ethical Conduct of the University of Minho.

Resumo

Bartolomeo é a primeira plataforma comercial instalada no exterior da Estação Espacial Internacional (ISS), e tem o intuito de simplificar o acesso a experiências comerciais à estação. Cada uma das empresas ou instituições que se propôs a realizar experiências nesta plataforma terá de ver os seus equipamentos alimentados por uma unidade de fornecimento e distribuição de energia que assegure performance contínuo, fiável e duradouro. Assim, este documento analisa os requisitos elétricos do sistema e a arquitetura da unidade de fornecimento e distribuição de energia que será alojada na instalação de ciência exobiológica. Esta fonte irá lidar com a proteção contra sub e sobretensões e contra correntes de *inrush* e também com diferentes limitações de corrente, filtragem e regulações de tensão. Também irá incluir vários sensores de temperatura, que irão permitir monitorizar os pontos de temperatura mais críticos do dispositivo, e circuitos de condicionamento de sinal para efetuar as medições da tensão e corrente na entrada. A unidade foi desenhada com o intuito de controlar o estado das saídas, efetuar as medições dos níveis de tensão e de corrente em todas os equipamentos, e da temperatura tanto no lado de fornecimento como no lado de distribuição da energia e ainda comunicar via porta série com a estação espacial para efeitos de controlo. Como é obrigatório em todas as atividades espaciais europeias, o equipamento tem de estar em conformidade com os requisitos presentes em normas internacionais bastante exigentes. Por esta razão, esta dissertação apresenta duas análises elétricas que foram efetuadas para aumentar a probabilidade de sucesso e maximizar a segurança do sistema. Inicialmente foi realizada uma *Worst Case Analysis*, de modo a ser possível averiguar sobre a *performance* do circuito em condições de operação extremas. Posteriormente, foi efetuada uma *Part Stress Analysis* que examina o *stress* máximo aplicado a cada componente. Para demonstrar que a unidade de fornecimento e distribuição de energia dimensionada cumpre com os requisitos foram simulados todos circuitos tanto individualmente como em conjunto. Os resultados obtidos permitiram preparar os próximos passos de integração, teste e validação que antecedem a produção do modelo de voo da unidade.

palavras-chave: PSDU, PSU, PDU, WCA, PSA

Abstract

Bartolomeo is Europe's first commercial platform on the exterior of the International Space Station (ISS), intended to give commercially motivated experiments quick and simplified access to the station. Any instruments that are going to be installed to perform the experiments require a power supply and distribution unit (PSDU) to ensure continuous, reliable and long lasting performance. Thus, this document analyses the electrical requirements of the system and the design architecture of the PSDU to be deployed in the scientific exobiology facility of the platform. The power supply unit deals with over and under-voltage protection, inrush current protection, current limitation, filtering, and voltage regulation. It also includes temperature sensors to monitor the most critical temperature points in the device and a signal conditioning circuit for voltage and current measurements from the input. The power distribution unit was designed to be responsible for the output state control, the voltage and current measurements at all internal instruments, and the serial communication for control purposes. As mandatory for all European space activities, the equipment must be compliant with standard requirements. For that reason, this dissertation presents two electrical analyses that were performed to increase the probability of success and maximize the safety of the system. First, a Worst Case Analysis was performed to determine the performance of the circuit under extreme operating conditions. Then, a Part Stress Analysis was produced to examine the maximum stress applied to each part. The simulations of the electrical analysis show that the PSDU meets the analysed requirements. Based on the results obtained, it was possible to propose the next steps in the analysis and preparation for the integration, testing and validation phase before the production of the Flight Model.

keywords: PSDU, PSU, PDU, WCA, PSA,

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List of Abbreviations

AD	applicable documents
ADC	analog-to-digital converter
CM	common module
COTS	commercial off-the-shelf
DC	direct current
ECSS	european cooperation for space standardization
EEE	electrical, electronic, electromechanical
EM	engineering model
EPS	electrical power system
ESA	european space agency
ESD	electrostatic discharge
DIR	fault detection, isolation, and recovery
HW	hardware
HK	housekeeping
ISS	international space station
IC	integrated circuit
LCL	latched current limiter
LED	light-emitting diode
LDO	low-dropout regulator
MCU	microcontroller unit
OVP	over-voltage protection
OTP	over-temperature protection

PA	product assurance
PCB	printed circuit board
PDU	power distribution unit
PSDU	power supply and distribution unit
PSU	power supply unit
PSA	part stress analysis
PMAD	power management and distribution system
SM	science module
SPF	single point failure
SPI	serial peripheral interface
UART	universal asynchronous receiver/transmitter
VCD	verification control document
VDC	volts direct current
UVP	under-voltage protection
WCA	worst case analysis

Chapter 1: Introduction

The work presented in this dissertation is a small part of a much broader space mission aimed at raising the opportunity to all Member States of United Nations and developing countries to accommodate and operate payloads on the Airbus Bartolomeo external platform on the International Space Station (ISS). Where the particular focus here is on the power supply and distribution unit that will manage and deliver power to these payloads. In this first chapter, the introduction to this dissertation is presented through the contextualization, motivation and objectives of the work developed. The contextualization outlines the space mission within which the thesis is developed. Building on this, the motivations for developing this project are presented, supporting the author's choice of this topic, and giving prominence to its relevance to current paradigms. With the aim of reach a well-founded outcome, the objectives are specified and explained to structure the work and lead to the desired result. Since this project was conducted in a business context, there is a section introducing the company that set the author on this path. To guide the reader through the text, this chapter ends with the structure of the present document.

1.1. Contextualization

The International Space Station consists of pressurized modules, external trusses, solar arrays, and many other components. It serves as a microgravity and space environment research laboratory in which crewmembers conduct experiments in numerous scientific disciplines: astronomy, biology, physics, and numerous microgravity research disciplines. It may also be utilized for the testing of spacecraft systems and equipment required for missions to the Moon and Mars. Since November 2000, the ISS has been continuously occupied, which is the longest continuous human presence in space. It is a joint project among five participating space agencies: NASA, State Space Corporation (Roscosmos), JAXA, ESA, and the Canadian Space Agency (CSA), as depicted in Figure 1.1 [1]. However, space is hard for most organisms, and thanks to a series of exposure facilities outside the station, researchers know how hard it is by analysing organic samples that have been exposed to solar and cosmic rays over time. Researchers have already found life that can survive space flight. Both lichens and small organisms called tardigrades

or 'water bears' have spent months outside the International Space Station and returned to Earth alive and well [2].

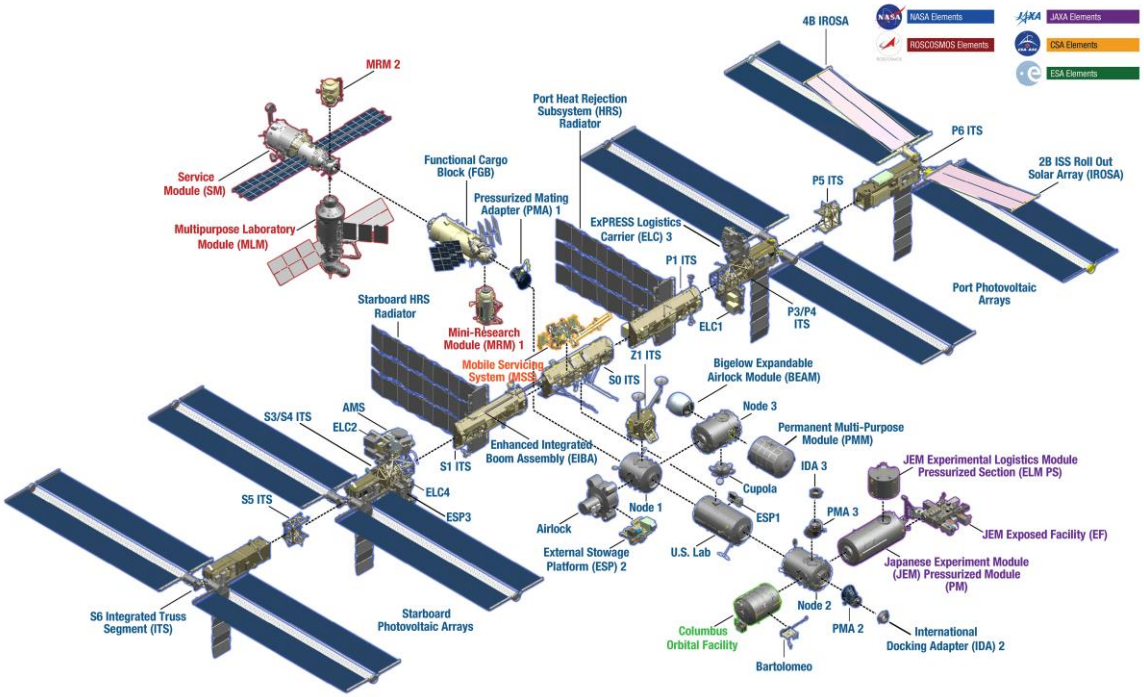


Figure 1.1 – International Space Station expanded view [1]

Now the European Space Agency (ESA) is looking to take exobiology, the study of life in space, to the next level with a new experimental facility, the ESA's Exobiology Platform (EXPO). This facility is going to be the first commercial platform to be installed on the *Bartolomeo* payload hosting platform outside the European Columbus module on the ISS, as shown in green in Figure 1.1 and amplified in Figure 1.2. Is intended to give commercially motivated experiments quick and simplified access to the station. Researchers from a great variety of fields and small and medium-sized enterprises (SMEs) will benefit from this new platform since there are unique possibilities that cannot be achieved in any laboratory on Earth. The experiments they can do in the platform payloads will be considerably more cost-effective to conduct on Bartolomeo than it would be on satellites, as they do not require their own rocket launch but rather are accommodated on routine supply flights to the ISS. The platform offers its users an unobstructed view of Earth, direct control over experiments from the ground and the possibility of retrieving samples [3].

ESA's exobiology platform is equipped with a series of radiation experiments aimed at better understanding the evolution of organic molecules and organisms in space. Placed in a slot facing Zenith, the point in the sky directly above the observer's head, the facility will connect two science modules (SM) to Bartolomeo. These modules will house everything needed for the experiments, including science

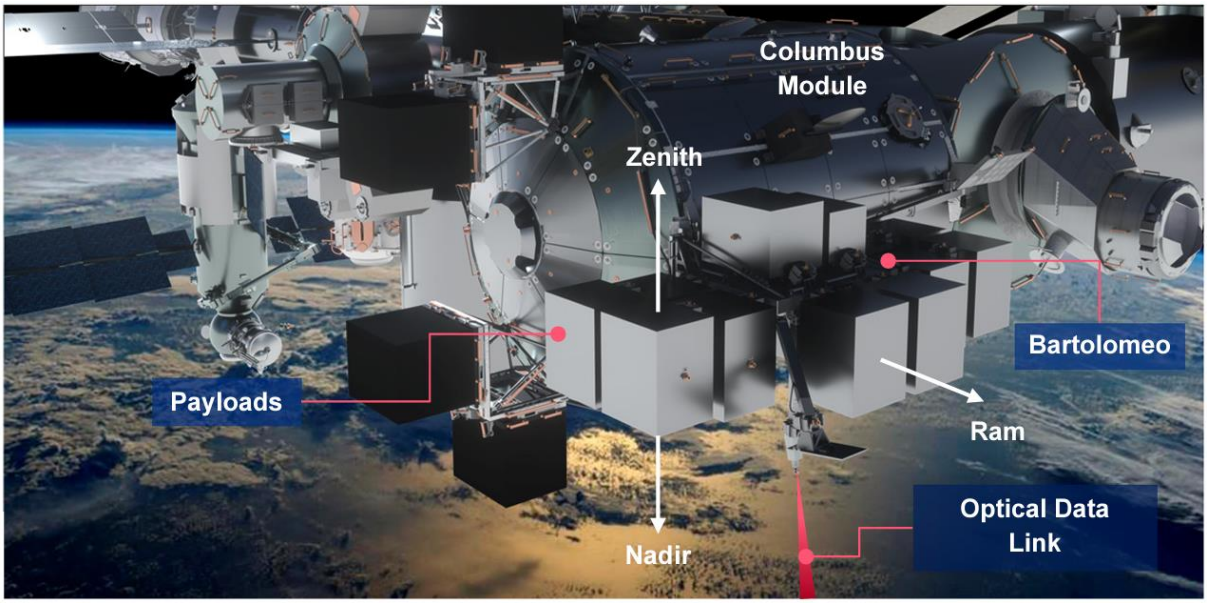


Figure 1.2 – Bartolomeo located on the ram-side of the Columbus module at the front of the International Space Station [3]

sample containers, fluidic systems, and sensors for the experiments [4]. At the end of the three-year mission, the samples will return to Earth for in-depth study and analysis. Although, the unprotected stay in space is characterized by an intense radiation field, high vacuum, extreme temperatures, and microgravity. So, there are numerous challenges that electronic components must withstand without compromising their performance.

1.2. Motivation

Space and the development of technologies associated with it are now recognized by several nations as a national driver essential to the advancement of a country's social and economic progress and to international security. More than 15 years after joining the European Space Agency, Portugal is considered a success due to its rapid adaptation and integration into space programmes. The national prestige already achieved requires Portugal to position itself in the near future as a true space nation, capable of taking on the new challenges of the sector [5].

Some of the greatest scientific challenges in this area are understanding our own origins and evolution, and more reliably assessing the possibility of life outside our solar system. The intellectual impact of these discoveries is likely to be as great as that of molecular biology. The science of exobiology seeks to reconstruct the natural history of the processes and events involved in the transformation of biogenic

elements from their origins in nucleosynthesis to their participation in Darwinian evolution in the solar system on planet Earth. This reconstruction will make it possible to develop a general theory for the evolution of living systems from inanimate matter.

Despite the demanding nature, engineers operating in this field are intrinsically highly motivated, due to the nature of the task, the mission they are involved in, and the idea that their accomplishments can one day make a difference to society. The acceptance of these engineering challenges led the author to EVOLEO and consequently to the choice of this project to obtain the master's degree.

1.3. Objectives

The goal is to analyse a power supply and distribution unit that will convert, manage, and distribute power from the Bartolomeo platform to the different payloads and ensure its correct performance throughout the mission. To achieve this, there are some clear objectives to pursuit:

- **System specification**

This objective is achieved by analysing the main system requirements of the downstream and upstream sides of the PSDU to ensure that the product is developed to meet the project needs. These requirements are divided into electrical, mechanical, and embedded software, but only the ones that involve electrical concepts are analysed. To conclude the preliminary analysis, it is important to analyse the European Cooperation for Space Standardization (ECSS) standards and the ISS requirements that should be shared by management, engineering, product assurance, and sustainability teams in space projects and applications. Based on the results of the previous objective, a general overview of first top level system definition is done. The electrical design of the PSDU follows a building-block approach so that each step forms the foundation for the subsequent design step on the path of least resistance to the desired outcome. The power supply is divided into distinct blocks that are described in a modular fashion, so the result is a coherent, logical design flow where the unknows are minimized.

- **Detailed design**

In order to make a proper electrical analysis of the entire system and check that all parts fit and are correctly sized, time must be allowed in learning and understanding each block of the PSDU. To

summarise all the concepts learned, a detailed description of each circuit is made as well as some representative diagrams of the circuit.

- **Electrical analysis**

By considering component variability, a Worst Case Circuit Performance Analysis (WCCA) is presented to determine the performance of the circuit under extreme environmental or operating conditions. Following the above goal, to increase the probability of success of the system, a Parts Stress Analysis (PSA) is performed. This analysis involves examining the electrical circuits to determine the maximum stress on each part when all applied voltages or currents are maximised and when all variations of other parts in the circuit are set to the combination of minimum and maximum values that yields the worst-case maximum stress. Besides the execution of these analysis, the methods and requirements followed to perform them are also covered.

1.4. Contributions of this Dissertation

The project was developed while working in the Portuguese branch of the company EVOLEO Technologies, Lda. (logo in Figure 1.3) for a client company. As the author has meet confidential information of high commercial value, which the company wishes to protect in order to keep the competitive advantage on its side, a non-disclosure agreement has been signed. For these reasons, the author is not allowed to publish some points of his work. In this work, the PSDU was designed by Rodolfo Martins, the CEO (Chief Executive Officer) of the company and an experienced electrical engineer, who gave the author of this work, the opportunity and responsibility to perform the full electrical analysis of the entire circuit.

Figure 1.3 – EVOLEO Technologies logo

1.5. Document Structure

The work developed in this dissertation is organized into six different chapters to facilitate the understanding and progression of the project.

The Introduction of the thesis is the first chapter, here the circumstances that led to the reliability analysis of the power supply and distribution unit developed are presented, as well as the contextualization, the motivations, and the objectives. Chapter two presents the State of The Art, where an overview of Small Spacecraft Power Systems is presented, along with some theoretical concepts about Dependability Requirements for Space Systems, Worst Case Analysis and Part Stress Analysis. The System Specification is on the third chapter, it refers the Main System Requirements and the Preliminary Design of the System. Chapter four describes the Detailed Design of the PSDU and is divided into the PSU Detailed Description and the PDU Detailed Description. The Electrical Analysis performed are explained on chapter five, the Worst Case Circuit Analysis and the Part Stress Analysis. Finally, the chapter six ends this dissertation with the Conclusions of the developed work and the description of the Future Work of this project.

Chapter 2: State of the Art

In this chapter, several key aspects of the proposed implementation are presented, starting with more general concepts such as the power systems that have been marketed for space projects in recent years, and then move down to the heart of the problem which is the application of analysis and design methods to ensure that the reliability goals of a space project are met.

2.1. Small Spacecraft Power Systems

Since 94 % of all spacecraft launched in 2020, were small spacecraft, weighing less than 600 kg, most of the current open literature on electrical power systems for space applications relates to small satellites, or SmallSat for short [6]. Yet, the overall electrical system required for such small devices has some similarities to that of a larger spacecraft. For this reason, the goal of this section it to assess and provide an overview of the state of the art in small spacecraft technologies with focus on the engineering requirements and processes for choosing a device.

Although the location of the equipment is not familiar, an electrical power system (EPS) for a spacecraft encompasses the usual, electrical power generation, storage, and distribution. Being the most important and fundamental subsystem, it usually occupies a large part of the volume and mass of any spacecraft. The technologies commonly used for power generation in space include solar energy through photovoltaic cells, panels, and arrays, as would be expected, but may also involve radioisotope or other thermonuclear power generators. The generated power is typically stored in batteries; either single-use primary batteries, or rechargeable secondary batteries. Since the manage and distribution of the power is the subject of this dissertation, the focus of this section will also be the state-of-the-art technologies for this purpose.

To facilitate the control of the power supplied to the loads, the power management and distribution (PMAD) system of a SmallSat is often custom designed to meet specific mission requirements. However, it is important to note that there are fundamental differences when designing it with commercial-off-the-shelf components (COTS) or with space qualified parts. While military or space (MIL/QML) parts need to pass a great variety of meticulous tests, and, for example, be qualified to survive from -55°C to 125°C,

COTS usually go through a more flexible test package, requiring operational function for a small temperature range, -40°C to 85°C. Unlike what happens with the PSDU for the Bartolomeo module, subject of this dissertation, most of these small satellites do not need to be prepared for the harsh environments that the military parts are designed to endure. Despite of not having to pass, for example, radiation or reliability tests that the MIL/QML qualification process involves, COTS parts, typically perform better than space rated parts, being several generations in advance, more available and having a faster revision timeline. COTS make sense for SmallSats also because the missions they are involved in have more flexible qualification standards, require a lower Technology Readiness Level (TRL) and typically happen for shorter periods of time, in more favourable environmental conditions.

2.1.1. Power Management and Distribution

The information described below is not intended to be exhaustive but provides an overview of current state-of-the-art technologies and their development status for a specific small satellite subsystem, the power management and distribution system.

Despite sometimes being custom designed for specific power requirements, several manufacturers have introduced in the market some PMAD devices for inclusion in small spacecraft missions. Besides distributing the power from energy sources, they also condition energy, mitigating harmful transient disturbances and failures from propagating downstream and harming the connected loads.

Some of the most popular PMAD systems manufacturers, that produce these systems for small spacecraft, are Pumpkin[7], AAC Clyde Space [8]–[10], GomSpace [11] and ISISPACE [12]. Although not intended to be exhaustive, a list, with some of the products these companies sell, is presented in Table 2-1 and shown in Figure 2.1. All of these companies have flight heritage, which means that they produced

Table 2-1 – Description of products from Pumpkin [7]*, AAC Clyde Space* [8]–[10]*, GomSpace* [11] *and ISISPACE* [12] *of power management and distribution systems*

Company	Product	Mass (kg)	Volume (cm^3)	Peak Power Output (W)	Input Voltages (VDC)	Output Voltages (VDC)	Max Efficiency
Pumpkin	ESPM 1	0.300	250	160	8 – 55	3.3 – 50	98.5
ACC Clyde Space	Starbuck Micro	2.45	3968	120	28	28/5	97
	Starbuck Mini	5.90	13133	1200	*	22 – 34 / 5 / 8 / 12 / 15	*
	Starbuck Nano	0.086	140	*	*	3.3 / 5 / 12	*
GomSpace	P31U	0.100	127	30	0 – 8	3.3 / 5	96
ISISPACE	iEPS Type C	0.360	14.13	13	12.8 – 16	3.3 / 5 / Unreg	95

*Available with Inquiry to Manufacturer

components and systems that have already successfully been employed in a low-Earth orbit (LEO) mission.

When analysing the available options of PMAD in the market there are some critical metrics to consider for a good design, such as input/output voltage range, conversion efficiency, output power capabilities, and size, weight and power (SWaP). The designer has to leverage the benefits and risks to the mission when choosing PMAD, yet it must be noted that there is no single COTS solution that can meet all the requirements of a mission at hand, since most devices sacrifice specific features that can impact important metrics for SmallSats.

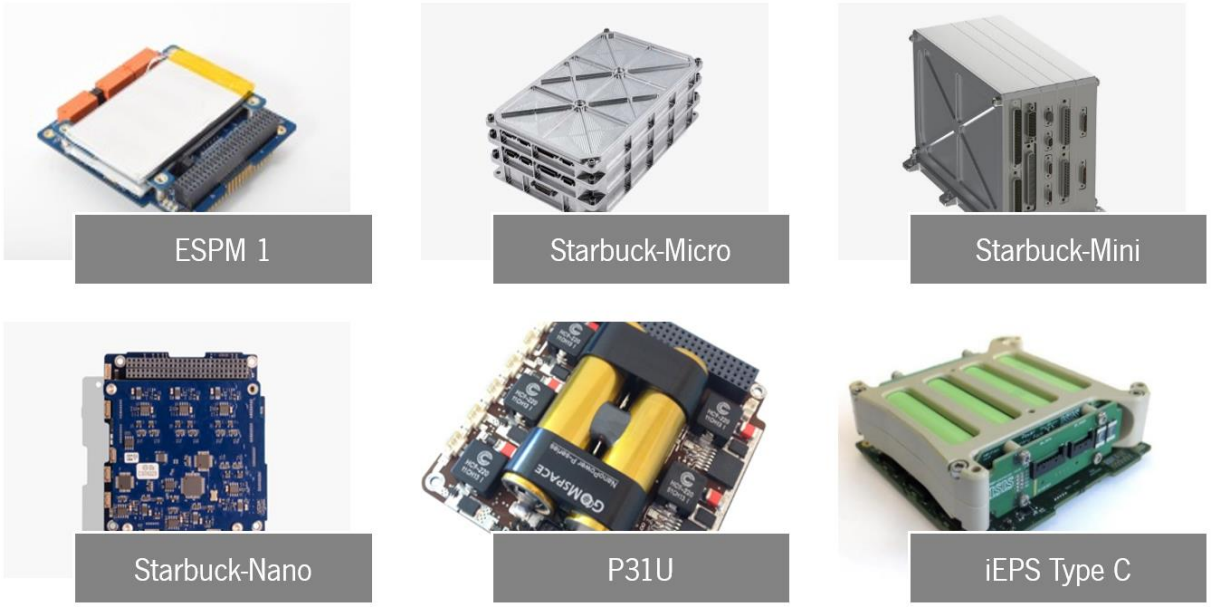


Figure 2.1 – Photographs of products from Pumpkin [7], AAC Clyde Space [8]– [10], GomSpace [11] and ISISPACE [12] of power management and distribution systems

2.2. Space Concepts

To provide a framework for the work developed, this subsection explains the dependability requirements for space systems, defined by the European Cooperation for Space Standardization (ECSS) [13] and some theoretical concepts about the electrical analyses that are presented in chapter 5.

A continuous and iterative dependability assurance process must be carried out throughout the project lifecycle.

The ECSS dependability policy for space projects comprises the optimization of the schedule and overall cost of the project ensuring that:

- the risk reducing actions, design rules and dependability analyses are adapted with respect to an appropriate severity categorisation,
- and that since the beginning the project, continuously implementation of risk reducing actions are taken.

The dependability assurance programme also includes the identification of all technical risks concerning the functional requirements that might cause non-compliance, and the application of the analysis and design methods that ensure that the dependability targets are met which end up being the inputs to the serial production activities.

Some of the terms commonly used in electrical analysis, like the ones presented in chapter 5, are introduced below. The definitions of terms used herein are in accordance with the definitions used in the "ECSS: Glossary of terms" standard [14]:

- **criticality:** classification of a failure or failure mode according to a combination of the severity of the consequences and its likelihood or probability of occurrence;
- **derating:** action when designing a product to limit the component stresses to specified levels that are below their ratings in order to increase its reliability;
- **detection:** likelihood of not detecting a root cause before a failure can occur;
- **failure effect:** adverse consequence of a failure in terms of the operation, function or status on a system. It can be addressed from two points of view: the first one is local, in which the failure is isolated and does not affect anything else so that it is considered the impact on a system element under consideration; the second one is global, in which the entire system is considered for the effect analysis;
- **failure mode:** manner in which a failure occurs; the way in which a component could fail to perform a required function;
- **payload:** A spacecraft payload is a set of instruments or equipment which performs the user mission;
- **protoflight model:** flight model on which a partial or complete protoflight qualification test campaign is performed before flight;

- **severity:** classification of a failure or undesired event according to the magnitude of its possible consequences.
- **single point failure:** part of a product that, if it fails, will result in the unrecoverable failure of that product
- **worst case:** highest or lowest boundary value of a given control parameter established in a validation or qualification exercise

The identification of the critical areas of the design and the assessment of the severity of the failure consequences must be interpreted by the level at which the analysis is made. In the design approach, the designer has to confirm that the design was built with reliability using fault tolerance and margins. In order to identify weaknesses, the fault characteristics of the system must also be analyzed, and corrective solutions must be proposed.

2.2.1. Worst Case Analysis

According to the European Cooperation for Space Standardization (ECSS), the Worst Case Analysis (WCA) is a performance prediction of the circuit under worst case conditions. It refers to the highest or lowest limits of a particular control parameter determined in a validation or qualification exercise, without considering the effects of failures or single events [29].The worst case analysis is used to demonstrate sufficient operating margins for all operating conditions in electronic circuits.

The following basic tasks were performed:

- partitioning of large circuits into smaller circuits which are better manageable (functional blocks);
- selection of critical circuit attributes;
- mathematical simulations of circuit behaviour;
- application of a worst case numerical analysis technique.

The flow diagram of a worst case circuit analysis performance is shown in Figure 2.2.

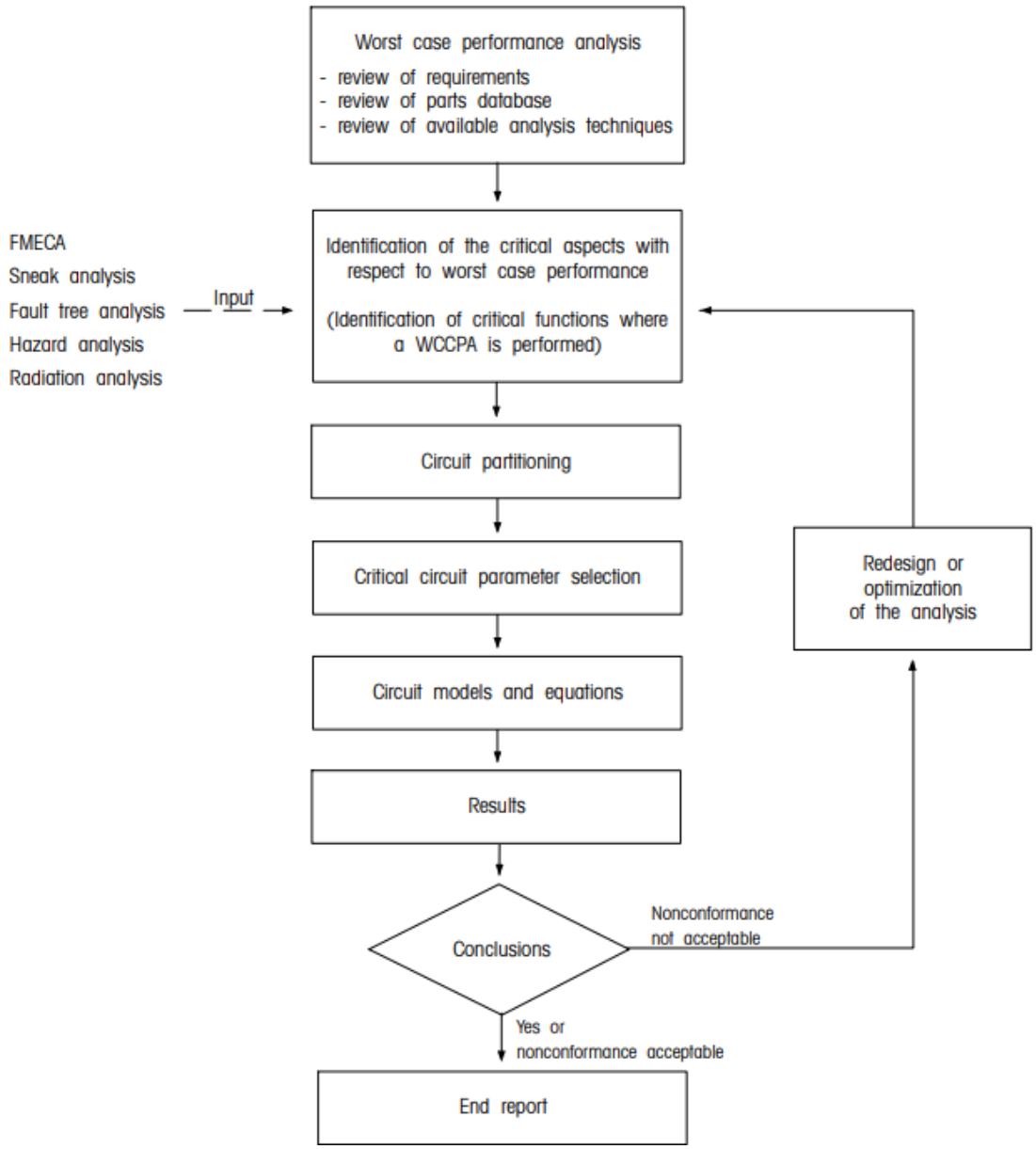


Figure 2.2 – Flow diagram of worst case circuit performance analysis [29]

2.2.2. Parts Stress Analysis

The part stress analysis (PSA) method is a prediction method used in the detailed design stage when there are few or no assumptions necessary about the parts used, their stress derating, quality factors, operating stress, or environment in order to determine part failure rates. These should be all known factors or capable of being determined based upon the state of hardware definition for which the PSA is applicable.

The PSA procedure is the most accurate method of reliability prediction prior to the measurement under actual or simulated usage conditions and assumes that the time of failure of every part is exponentially distributed.

In this method, electrical circuits are analysed to determine the maximum stress on each part when all applied voltages or currents are maximised and when all variations of other parts in the circuit are set to the combination of minimum and maximum values that produce worst case maximum stress. This requires a new selection of "other" part combinations in the circuit each time the stress on a new part is determined.

Heavily stressed parts are identified for possible replacement with more robust parts or circuit modification. The final design was confirmed with part-level thermal, voltage and current analysis derived from either specification limits or worst case circuit analysis results.

This standard applies to all components, selected for space applications, that are used for a significant duration. One of the most important aspects and a long-standing practice for spacecraft components of the PSA is the derating. The benefits of this practice are now proven, but for competitiveness reasons it is necessary to find an optimal reliability. Excessive derating can lead to unnecessarily complex designs, excessive cost, and component oversizing, which in turn leads to too much volume and weight.

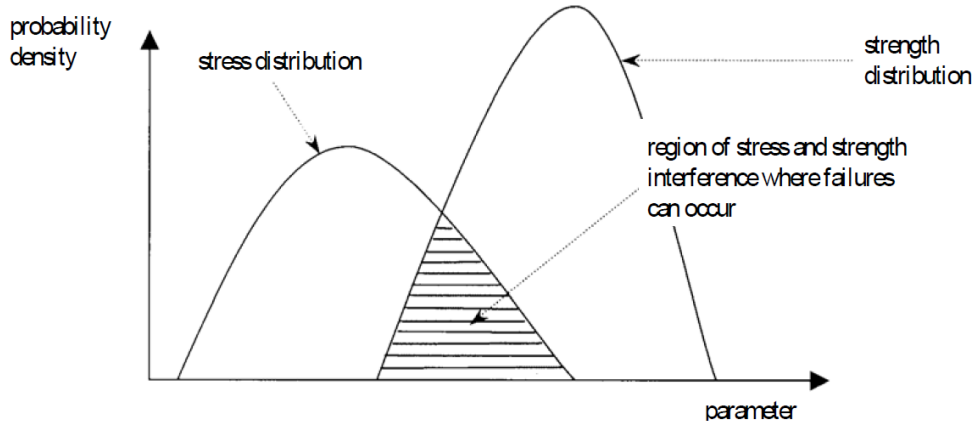


Figure 2.3 – Parameter stress versus strength relationship (extracted from [30]*)*

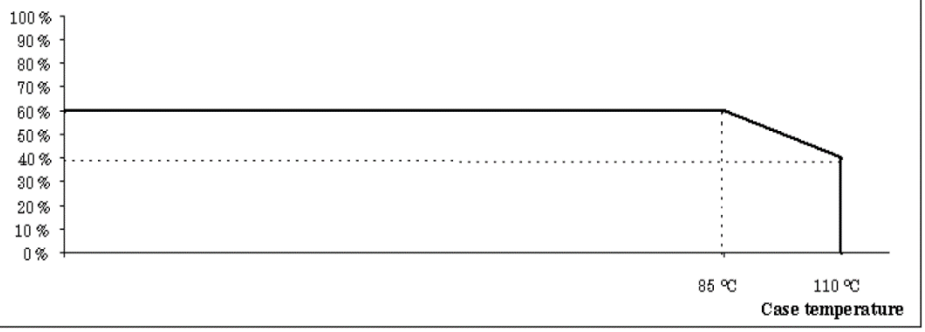
The ECSS standard entitled “Derating – EEE components” [30], identifies the derating constraints applicable to electronic, electrical, and electromechanical (EEE) components to reduce its stress-to-strength ratio. Derating pulls the stress distribution to the left while the selection processes employed to the components for space applications pushes the strength distribution to the right, as per Figure 2.3.

Derating requirements are provided for each component family and depend on their type. For each category, there are specific parameters to be derated, the main ones include:

- junction or case temperature,
- power (rating, dissipation),
- voltage,
- current.

For example, a ceramic capacitor from family-group code 01-01 and 01-02, shall be derated as Table 2-2 in this case the only parameters that need to be derated are the voltage and case temperature.

Table 2-2 – Derating of parameter for capacitor family-group code 01-01 and 01-02 [30]

Parameters	Load ratio or limit
Voltage	

If the component to be analyzed is a MOSFET transistor, there are much more parameters to derate (Table 2-3), but the method is the same.

Most often, the designer performs this analysis while selecting a component for a particular job and finds ways to reduce the parameters that need to be derated for that component, to avoid future work.

.

Table 2-3 – Derating of parameters for Transistors family-group code 12-05 and 12-06 [30]

Parameters	**Load ratio or limit**
Drain to source voltage (V_{DS})	80 % of rated, or the SEE safe operating area (VDS versus VGS), whichever is lower
Gate to source voltage (V_{GS})	75% of rated, or the SEE safe operating area (V_{DS} versus V_{GS}), whichever is lower
Drain current (I_{DS})	75 %
Power dissipation (P_D) max	65 % max
Junction temperature (T_j)	110 °C or $T_{j\,max}$ - 40 °C (whichever is lower) Exception: 125 °C, providing: 1. that the specified maximum rating Tjmax ≥ 150 °C, and 2. that Devices or Processes are supported by ESCC 226500 and 226900 evaluation program or equivalent and that the related evaluation reports are available (see NOTE).
NOTE: It is important that test results include the evidence of an equivalent operation life time covering the mission application.	

Chapter 3: System Specification

As mentioned in the introductory chapter of this document the Exobiology facility is designed with a modular fashion and equipped with an array of instruments. The facility has a common module (CM), which includes the interfaces with the external platform and the power, data and thermal control systems, and a scientific module (SM), which contains the biological samples and the necessary scientific instruments. The scientific module operates four experiments, namely OREO cube, ExocubeBio, Exocube-Chem and IceCold.

The part that is the subject of this dissertation is the power supply and distribution unit, which, together with a main control unit developed by another company, forms the electronics box of the scientific module. The initial architecture of the Electrical Power System (EPS), which was made as a requirement is shown in Figure 3.1.

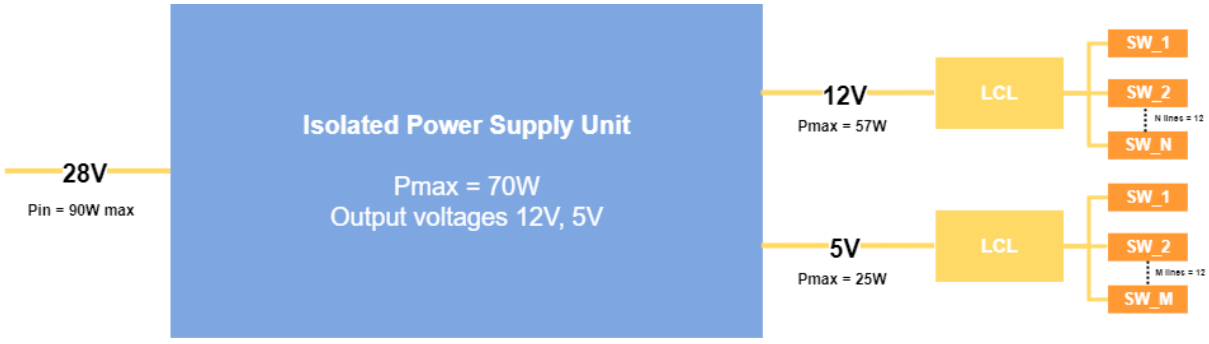


Figure 3.1 – Potential electrical power system architecture

In the first phase of this project, the project initiators elaborated the mission concept in terms of identifying and characterising the mission requirements, mentioned in this chapter, the expected performance, the reliability and safety objectives, and also the operational constraints of the mission in terms of the physical and operational environment.

As a first response, EVOLEO produced a top-level design of the power supply and distribution unit, which was adapted and summarized by the author to be inserted and described later in this chapter. Accompanying the design, a general overview of the diagram was made, as well as a description of the power supply area and the power distribution area separately.

3.1. Main System Requirements

When the project initiators provided the mission concepts, they also sent a list of applicable documents to be analysed together with the project-specific requirements. Some of the applicable documents are confidential and cannot be mentioned here. However, others, such as the European Cooperation for Space Standardization (ECSS) standards, are public and available online to reduce the risk of costly problems during development and operation; these are presented below.

- Space Product Assurance: Failure modes, effects (and criticality) analysis (FMEA/FMECA) [15]
- Space Project Management: Risk management [16]
- Space Engineering: System engineering general requirements [17]
- Space Engineering: Verification [18]
- Space Engineering: Thermal control general requirements [19]
- Space Engineering: Structural general requirements [20]
- Space Engineering: Structural design and verification of pressurized hardware [21]
- Space Engineering: Materials [22]
- Space Engineering: Software [23]

Due to the length of these documents, only the requirements that the client considered most important are mentioned this chapter. However, they have all been analysed to produce a compliance matrix containing the actual information on the compliance of the requirement, i.e. whether the requirement is met or not and, in case of deviations, the justification.

In addition to the ADs, as mentioned earlier, a list of project-specific requirements was also created, divided into five major technical areas: electrical engineer, embedded software engineer, mechanical engineer, product assurance and systems engineer. Some of the requirements can be part of two domains at the same time, so due to the nature of this dissertation, only the requirements that relate to electronic concepts will be analysed.

3.1.1. Electrical Requirements

The electrical requirements are listed below, but for ease of understanding, this list has been compiled.

1. The unit shall be able to provide an overall power of 70 W.

2. The unit shall be designed for a nominal input voltage of 28V (+1%/ -10%).
3. The input filter charge time shall be lower than 80% of the LCL (latching current limiter) class minimum trip off time. The upstream LCL is class 4.
4. The converter shall provide outputs compliant with the Table 3-1:

Table 3-1 – Output voltages and power

	Voltage (V)	Maximum Power (W)
Va	12	57
Vb	5	25

5. The output voltages shall provide power to the loads according to Table 3-2 and Table 3-3.

Note: The output switches shall have an inrush/soft start control.

Table 3-2 – Output current in Va

Va			
Outputs	**LCL Group and Class**	**Switch**	**Current (A)**
A1...A5	1 LCL class 2	Yes	1,5
A6...A10	1 LCL class 4	Yes	5,5

Table 3-3 – Output current in Vb

Vb			
Outputs	**LCL Group and Class**	**Switch**	**Current (A)**
B1...B6	1 LCL class 3	Yes	3,3
B7...B12	1 LCL class 2	Yes	2,7

6. The scientific module (SM) shall not generate primary power reverse current.
7. Primary power input lines (28VDC hot and return lines) shall have an insulation resistance ≥ 1.0 MΩ between each line and between the PSDU and the common module (CM).
8. The LCL design shall be compliant with the ECSS-E-ST-20-20C – Space engineering: Electrical design and interface requirements for power supply.

9. The generated secondary voltages (hot and return lines) shall have an insulation resistance ≥ 1.0 MΩ between each line and 28Vdc lines provided by the common module.

10. The broadband voltage emission at the SM power inlet (28 Vdc) shall meet the requirement number 4.1.5.2 in the standard Columbus EMC & Power Quality Requirements [24]. This requirement states the following: "Equipment/assembly generated broadband voltage ripple on primary DC power buses shall not exceed 300 mVpp/A. The limit is adjustable, depending on I(A). The conversion rule for voltage emission limits in (mVpp) is: $300\ \mathrm{m\ Vpp} * \sqrt{\mathrm{I(A)}}$ or $2\ \mathrm{Vpp}$ whichever is lower.".

11. The load transients at power inlet (28 Vdc) shall meet the requirement number 4.1.5.3 in [24] that states the following: "Both positive and negative transients on primary DC power buses shall not exceed the envelope defined in Figure 3.2 with maximum Pulse Repetition Rate P.R.R. = 10 Hz. Higher P.R.R. must be covered by limit in requirement 4.1.5.2. Time duration of the pulse is evaluated at 10% of transient amplitude.

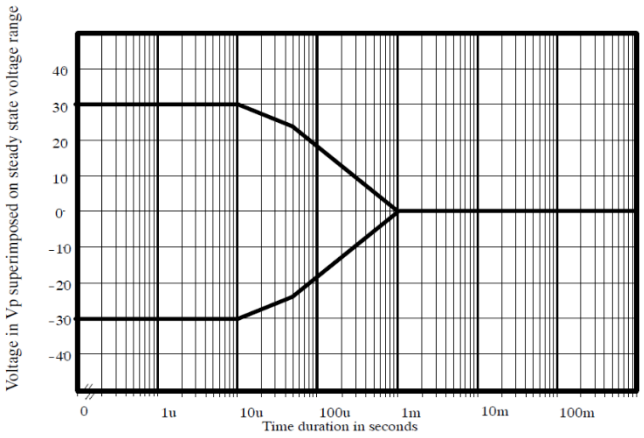


Figure 3.2 – Transient Emission Limit (Equipment & Primary Power Bus) [16]

12. The inrush current at power inlet (28 Vdc) shall meet the requirement number 4.1.5.4 in [24], that states the following: "The rate of change of current surges shall not exceed 0.1 A/μs.

Note: The inrush current requirement is not fulfilled by standard power outlets (requirement: > 10 ms and capability: > 1.5 ms)."

13. The unit shall be able to sustain without incurring permanent damages the sine wave injection at primary power inlet (28 Vdc) as requested by the requirement 4.1.7.1 in [24] which states: "The equipment/assembly shall not exhibit any malfunction, degradation of

performance or deviation from specified parameters beyond tolerances given by the corresponding specification when a sine voltage is injected into the primary DC power lines with amplitudes as indicated in Figure 3.3.".

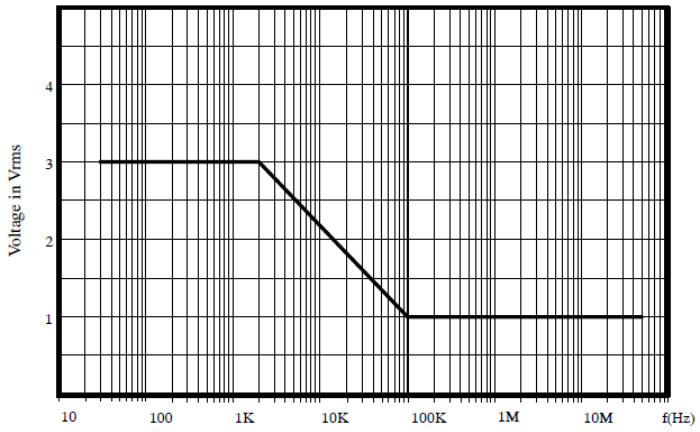


Figure 3.3 – Conducted sine wave susceptibility (equipment & system) [16]

14. The unit shall be able to sustain without incurring permanent damages the sine transient injection on SM1 primary power inlet (28 Vdc) as requested by the requirement 4.1.7.2 in [24], which states: "The equipment/assembly shall not exhibit any malfunction, degradation of performance or deviation from specified parameters beyond tolerances given by the corresponding specification when levels of Figure 3.4, plus 6 dB (or minus 6 dB if negative) are injected into the primary power lines.

The width of the pulses, to be injected shall be at least, T = 10 μs and T = 0.15 μs

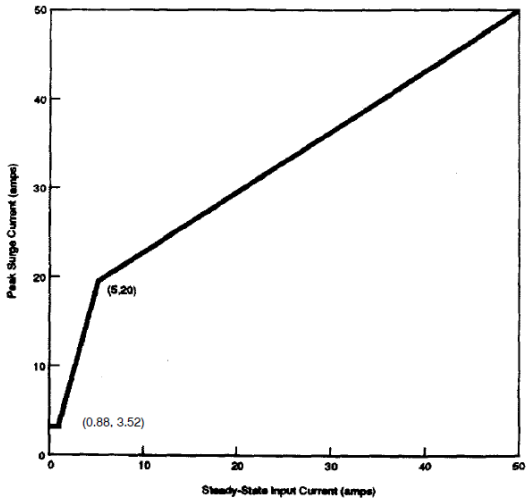


Figure 3.4 – Peak surge current amplitude versus steady-state input current [16]

15. The unit shall comply with requirement number 4.1.9 in [24], that says: "No malfunction, degradation of performance or deviation from specified parameters beyond tolerances given by the corresponding specification shall occur when equipment and interface lines are

exposed to a repetitive electrostatic arc discharge of at least 5.6 mJ energy/ 15kV. The test must be performed with conducted and radiated ESD sources".

16. All internal electrical wires shall be made of polyimide insulation as per European Space Components Coordination [25].

3.1.2. Mechanical Requirements

1. The power distribution unit (PDU) shall operate and fulfil all performance requirements within a temperature range from -25 to +60°C.

2. PDU shall survive in non-operational mode within a temperature range from -30 to +80°C.

3.1.3. Embedded Software Requirements

1. The supplier shall provide the telemetry/telecommand (TM/TC) interfaces.

Note: At least: Vin (Input voltage), Iin (Input current), Va, Vb and Ia, Ib (voltage and current on the single), DC-DC outlets, LCL status and trip status, status switch, inrush control, TM/TC preferred to be transmitted digitally, via RS-232 or similar.

3.2. Preliminary Design

The scope of this section is to provide a brief technical description of the system solution presented of the power supply and distribution unit (PSDU) unit to be integrated into the scientific module.

3.2.1. General Description

The PSDU receives primary power from the *Bartolomeo* facility and generates the necessary secondary voltages for the operation of the module instruments. In addition to the secondary voltage generation, the PSDU has the ability of enabling and disabling individual output lines. The block diagram of the PSDU is shown in Figure 3.5.

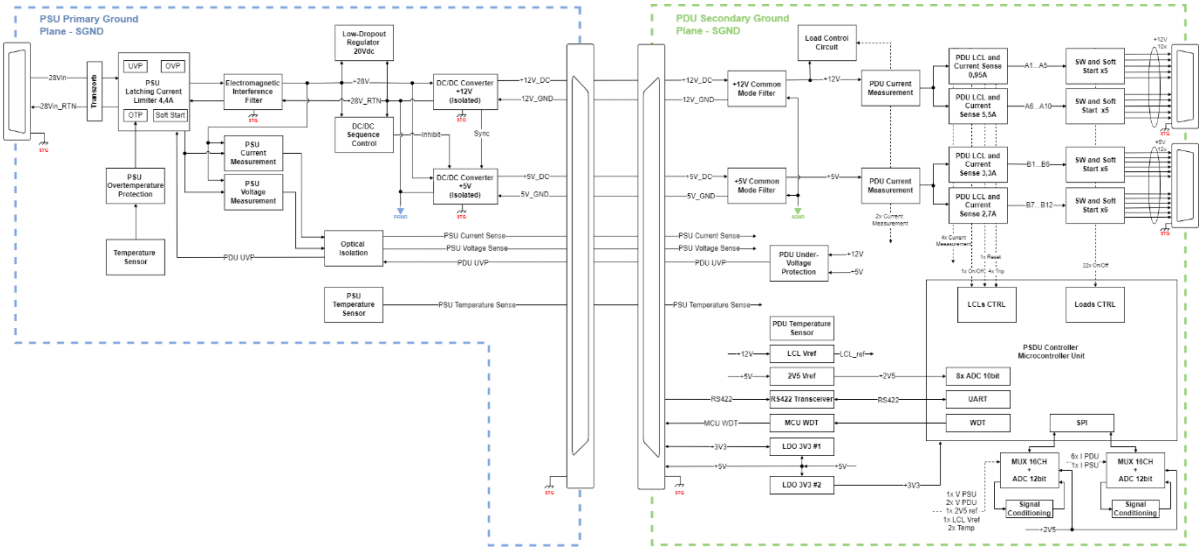


Figure 3.5 – PSDU functional block diagram

The PSDU can be split into two main blocks, the primary Power Supply Unit (PSU) and the secondary Power Distribution Unit (PDU). They are composed by the following set of features:

Primary PSU:

- Power input range: 24Vdc-32Vdc
- Input Latched Current Limiter (LCL)
- Input over-voltage protection (OVP)
- Input under-voltage protection (UVP)
- Over-temperature protection (OTP)
- High voltage transient protection
- Input soft-start
- Input isolated voltage and current measurement
- Sequenced and synchronized 2x 28V DCDC converter units

Secondary PDU:

- Load control circuit - DCDC protection
- Secondary under voltage protection (UVP)
- 10x outputs with +12V
- 12x outputs with +5V
- 2x LCL for +5V outputs
- 2x LCL for +12V outputs

- 22x switchable outputs
- PSDU housekeeping functions (include primary):
    - 3 voltages
    - 7x currents
    - 2x temperatures
- >12bit Analog-to-Digital Converter (ADC) resolution
- Microcontroller Unit (MCU)
- Serial universal asynchronous receiver-transmitter (UART) interface over RS-422

Safety and Protections:

- 28Vdc Input Power
    - protected by LCL (4,5A)
    - discrete monitoring, command & control lines optically isolated
- Secondary Output lines
    - galvanic isolated 28Vin DCDCs (single 12Vdc and single 5Vdc) with auto-current limitation
    - outputs protected by LCLs

3.2.2. PSU Functional Description

The power supply unit (PSU) part of the system was designed to serve as the interface between the *Bartolomeo* PSU and the power distribution unit (PDU) in charge of dealing with over-voltage and under-voltage protection, inrush current protection, current limitation, filtering, and voltage regulation. It also included a temperature sensor to monitor the most critical temperature point in the device and a conditioning circuit for voltage and current measurements of the input, as is shown in Figure 3.6.

More specifically, it was established that the power supply starts with a single input connector for the input power from the *Bartolomeo* power supply. Immediately after this connection, a transient absorption zener, was placed to protect the circuit from harmful transients and to shunt the excess current when the induced voltage exceeded the avalanche breakdown potential.

Also, as a protective measure, a complex latching current limiter circuit was developed to, not only limit the current to a defined threshold, but to protect against over and under-voltages as well. In addition, as required, soft-start capacitors were added to reduce inrush current by up to 70% and smooth the current limiting. Two external signals were connected to the above circuit to make use of its latching function. One was connected to an over-temperature protection circuit that works with the temperature measured

at the primary side, and the other (PDU UVP in Figure 3.6) was connected to an isolated signal from the under-voltage protection circuit that uses the voltage levels at the PDU. Additionally, the measured voltage and current values from circuits that sense the input voltage and the current after the LCL were connected to an optic isolation circuit that subsequently sends them to the microcontroller unit.

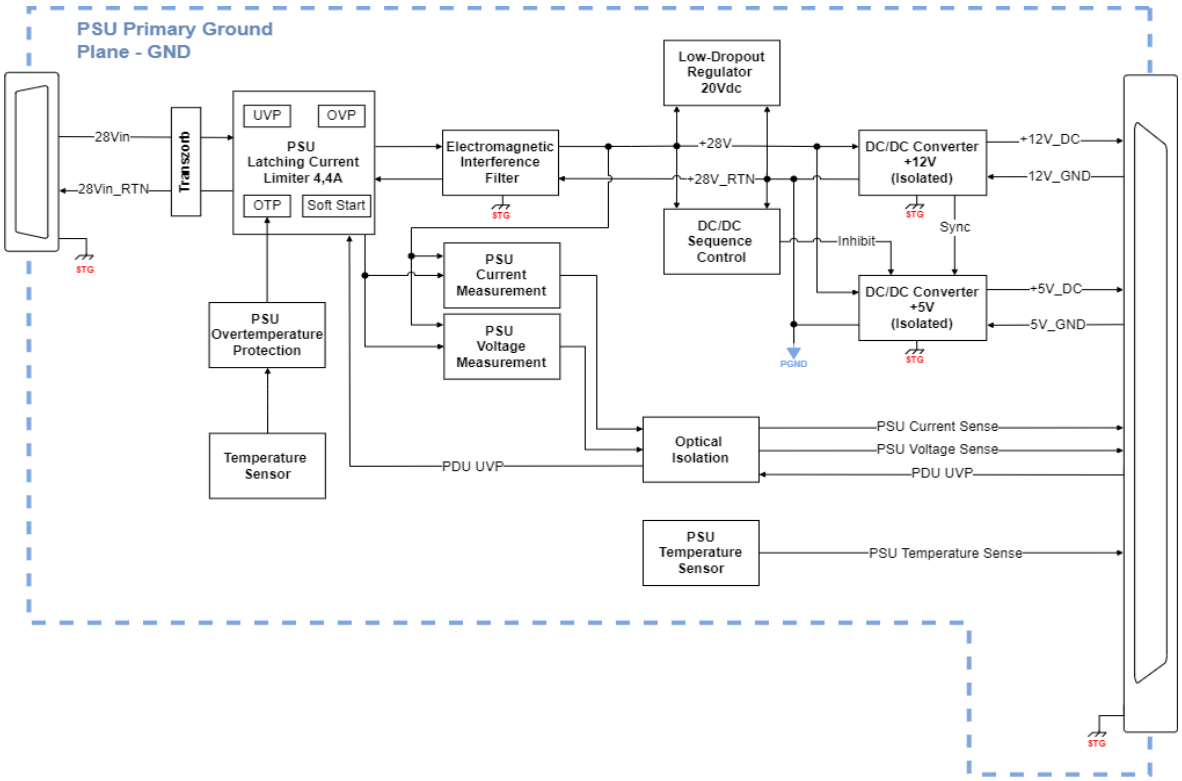


Figure 3.6 – PSU Functional Block Diagram

Upstream of the voltage regulation, an electromagnetic interference filter was connected to reduce the susceptibility of the power supply of being affected by electrical noise on the supply rails. Furthermore, it helps in reducing the propagation of conducted noise generated within the power supply back into the power rails.

Before the DC-DC converters, a linear voltage regulator of 20 V was used to provide a stable power supply voltage for them, independent of the load impedance, input voltage variations and temperature.

Because the DC-DC converters need to start at a well-defined order, a time-based control was used to deliver the enable signal to each converter. Then the converters take the nominal 28Vdc input voltage and convert it to the +5V and +12V that the PSDU outputs, which are galvanically isolated from the primary voltage source.

3.2.3. PDU Functional Description

The power distribution unit, as shown on the right side of Figure 3.5 and Figure 3.7 detailed, was designed to be responsible for the output state control, the voltage and current measurements, the connection to the external temperature sensors, and the serial communication for control purposes via the external scientific module.

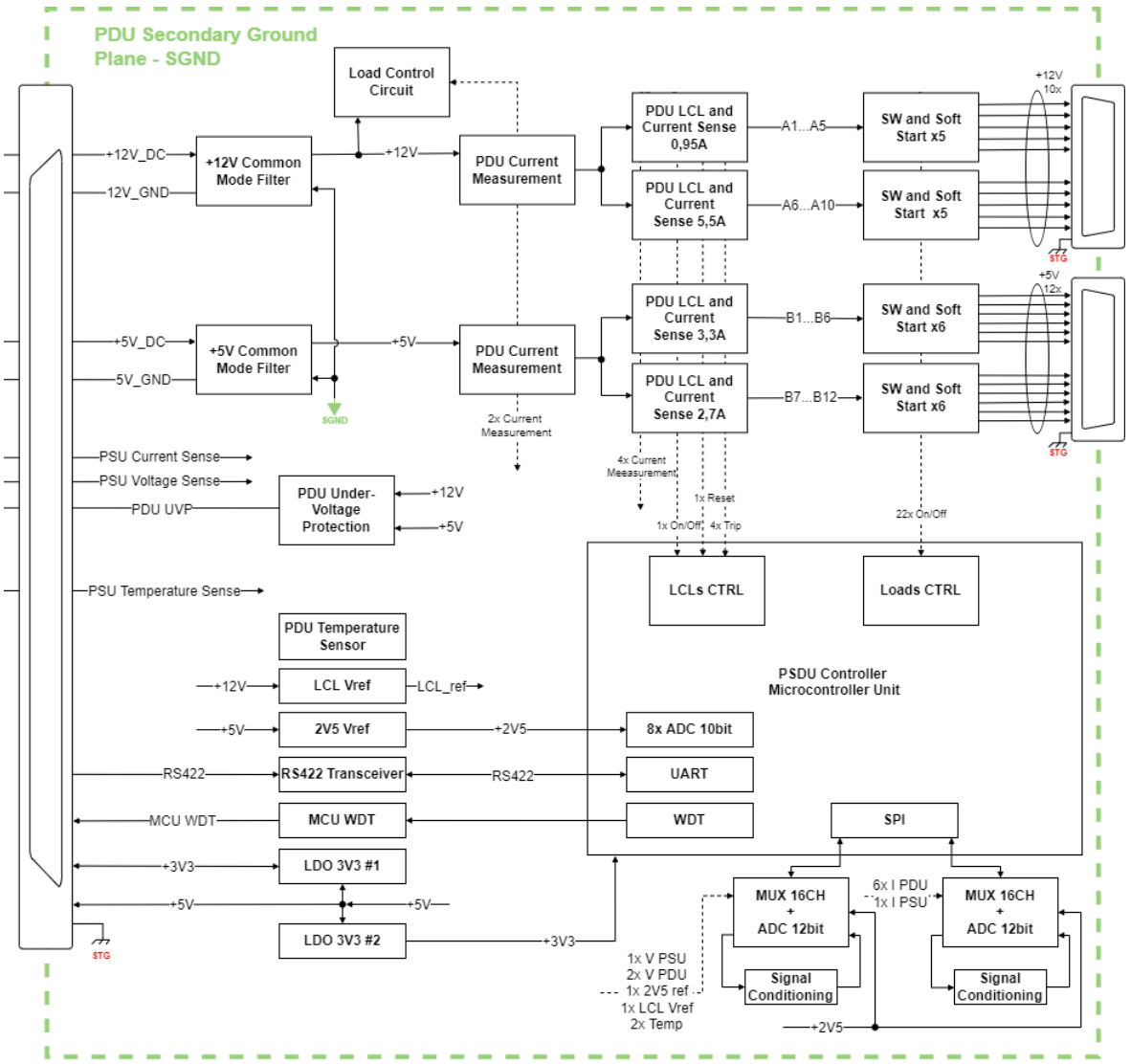


Figure 3.7 – PDU Functional Block Diagram

This unit takes the converted voltages of +12V and +5V and runs them through common mode filters to eliminate common mode noise that may have occurred on the DC-DC outputs. Since the selected DC-DC converters always require at least 10% of the power to be stable, a circuit was designed to generate a

minimum load when the power from the stand-by state is insufficient to supply this load. This load control circuit uses a power resistor that turns off a switch when the minimum threshold current is reached.

As shown Figure 3.7, after each DC-DC, in both voltage levels (Va = 12 V and Vb = 5 V) the current and voltage are measured and read on the ADC. Since the LCLs were controlled by the MCU, to reduce the number of signal conditioning circuits on the PDU, a grouping method was used, where signals with similar current values were grouped (for example from A1 to A5 the load current is 0,95 A). Each group has its own current sense amplifier and latching current limiter. An ON-OFF and reset signals, control all LCLs, so, when one of these signals is sent by the microcontroller, all of them act in accordance with the signal at the same time.

The twenty-two output switches are individually controlled by the MCU, each of them has soft-start capacitors to smooth the switching.

For added protection, an under-voltage protection circuit was designed to monitor the voltage at the output of each DC-DC converter. If an under-voltage is detected, the circuit sends a signal to the primary side LCL to turn it off.

Besides that, a temperature sensor to measure the internal temperature on the PDU side, a low-dropout regulator of 3,3 V DC to supply the internal MCU and an external, high precision and stable voltage reference integrated circuit (IC) of 2,5 V to have a common reference for all ADCs were added.

Using only two ADCs to measure all the required signals, resulted in the need to multiplex the inputs to the existing ADCs. The multiplexers used are integrated on the ADC IC with 16 analog channels, and input selection is done using the same SPI communication used for data. Signal conditioning was used to maximize the dynamic range of the ADC 1 input and buffer the signal before the ADC 2. By design, the output of this signal conditioning should be as close as possible to the range of 0 to 2,5 V.

Chapter 4: Detailed Design

Chapter 4 takes the top-level design of the system from the previous chapter and deepens it into a more detailed definition of the system. The design of this power supply and distribution unit follows a general pattern of steps, with each step forming the basis for the subsequent step. In order to carry out the electrical analysis correctly, it was necessary to have a good understanding of each block of the diagram shown in Figure 3.5 and a clear view of its role in the overall circuit. However, since the schematics of the designed circuits are property of the company, some generic diagrams were made to represent some of the circuits.

4.1. PSU Detailed Description

4.1.1. Electrostatic Discharge Protection

When two electrically charged objects, such as the human body and an electronic device, come into contact, static electricity is discharged. Static electricity is an imbalance of electrical charges within or on the surface of a material. Electrostatic discharge (ESD) is defined as "the rapid, spontaneous transfer of electrostatic charge induced by a high electrostatic field".

ESD can change the electrical characteristics of a semiconductor device, degrading or destroying it. It may also upset the normal operation of an electronic system, causing equipment malfunction or failure. Damage by an ESD event is determined by the device's ability to dissipate the energy of the discharge or withstand the voltage levels involved in the discharge. Therefore, to protect the PSDU from an ESD event and fulfil the requirement that states that the device must be ready to be exposed to a repetitive electrostatic arc discharge of at least 5.6 mJ/15kV, an ESD protection diode was used, as shown in Figure 4.1.

The protection diode chosen was a unidirectional transient voltage suppressor (TVS) placed at the beginning of the PSU, like this the abnormal voltages were supressed and the downstream components in the circuit were protected.

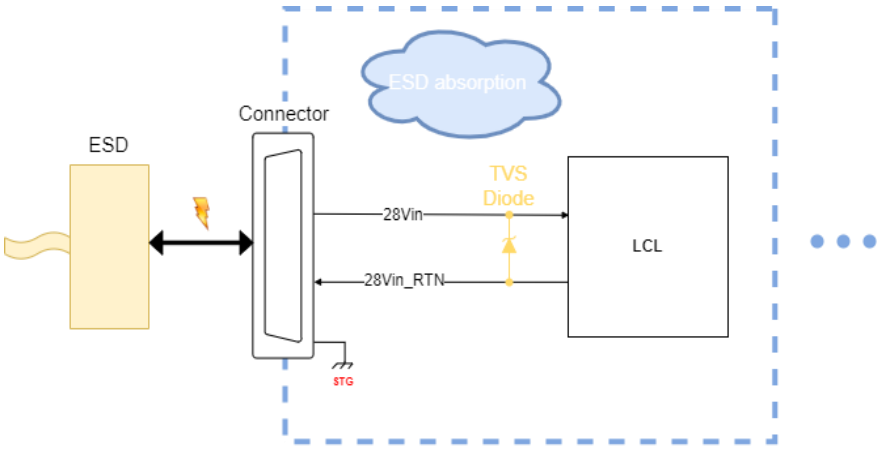


Figure 4.1 – Basic representative diagram of the ESD protection

4.1.1. Latching Current Limiter

Power distribution via latching current limiters (LCLs) has been widely used in almost all European spacecraft for several decades and is an effective method to achieve highly controlled and reliable connection and disconnection of loads from the spacecraft main bus, including power management in case of overload and load short-circuit faults.

A general architecture of the LCL designed is shown Figure 4.2. Due to confidentiality reasons, the diagram is for reference only, and that some of the functions shown in it can be implemented using components with similar functions.

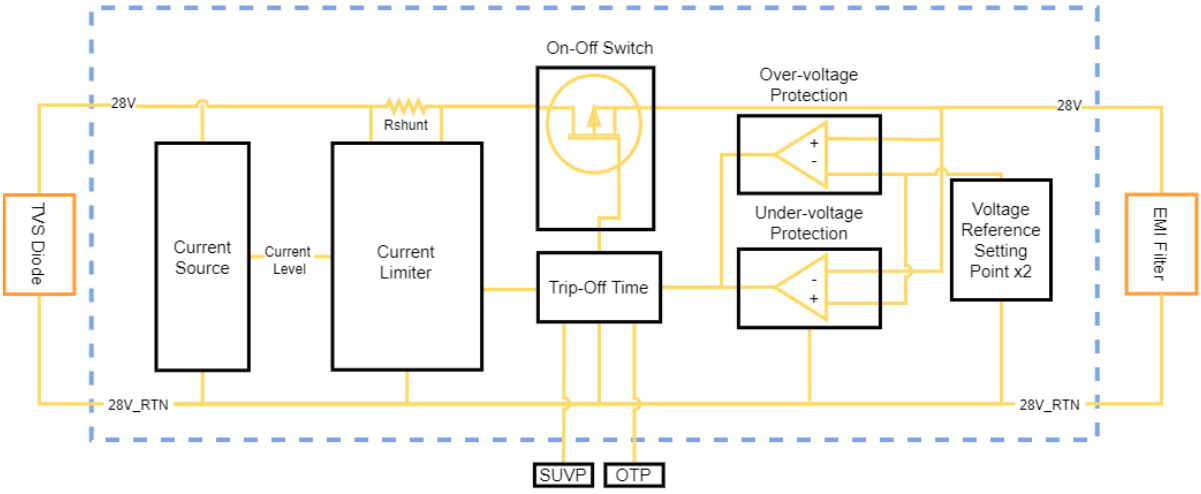


Figure 4.2 – Basic representative diagram of the LCL

In this mission, the goal was to implement an LCL for a module powered by an unregulated power bus with a voltage range from 24 V to 32 V, corresponding to the under (UVP) and over voltage (OVP) limits. Being a class 4 LCL, according to [26], the maximum operational current had to be 4 A, but the circuit could not limit the current until it reached the maximum value of 4,4 A. The trip-off time was required to be 6 ms, so the LCL should only shutdown the load if the fault was more than 6 ms long. The client also required the LCL to latch when it receives an exterior signal from an over-temperature protection (OTP) circuit at the primary side or from the under-voltage protection (UVP) circuit from the secondary side.

A typical timing diagram for the response of an LCL to an overload is shown in Figure 4.3. As can be seen, when a fault occurred (time point A), the current increased rapidly and exceeded the nominal threshold (time point B). Since the current must be limited to 4,4 A (time point C), a Wilson current mirror with a 10 mΩ shunt resistor, through which the load current flows, was designed. Because of a diode connected transistor and a connection between the bases of the transistors, typical connection in a Wilson current mirror, the voltage drop at the shunt resistor was forced to descrease, limiting the current to 4,4 A.

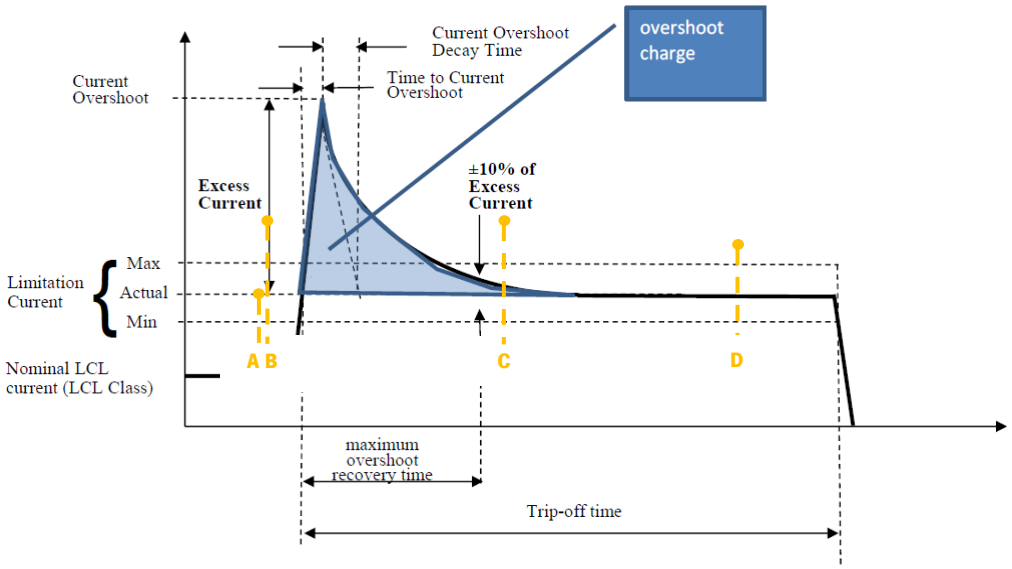


Figure 4.3 – LCL overload timing diagram extracted from ECSS-E-ST-20-20C

At point B, the LCL activates a countdown so that after the 6 ms (point D), the mosfet is switched off. To count the time that has elapsed since the load current exceeded the threshold, a RC (resistor and capacitor) low-pass filter was used. The capacitor from the RC filter begins to charge when the source voltage of the switch is higher than the drain voltage, i.e., when the mosfet begins to limit the current. A transistor was connected between the source and drain of the on-off mosfet so that, when a voltage drop

between these points occurred, the transistor begins to conduct, and the capacitor begins to charge. When the voltage drop across the capacitor reaches a certain value, another transistor begins to conduct, lowering the gate-source voltage of the mosfet and causing it to enter the cut-off region, stopping the flow of current to the load. If the load returns to normal (I_{LOAD} < 4.4 A) before the cut-off time expires, the capacitor discharges and the circuit stops limiting the current, resetting the counter and allowing it to detect another overload.

For under and over-voltage detection, two differential amplifier circuits with transistors were added to the LCL to detect whether the supply voltage was within the operating range or not. These circuits, the secondary undervoltage protection circuit and the primary over-temperature protection circuit were connected to the capacitor responsible for the shutdown time.

The final requirement for this LCL was to implement soft start, which was not represented in the diagram. This is crucial for maximising circuit performance and maintaining safe operation of the individual components. If the inrush speed were too fast, a transient current spike would occur on the input voltage, known as an inrush current. Inrush currents cause a dip in the input voltage that can negatively affect the functionality of the entire system. Likewise, inrush currents could damage the components of the load circuit or shorten the lifetime of the components. The faster the unit switches on, the higher the inrush current. This potentially damaging inrush current was reduced by controlling the load switch turn-on characteristics with the addition of capacitors. With this change, the mosfet trigger was attenuated from a period of about 12,6 µs to about 4,9 ms, which is almost 400 times slower.

4.1.2. Electromagnetic Interference Filter

Numerous governing bodies regulate the permissible levels of conducted and radiated emissions generated by an end product to maintain electromagnetic compatibility. These regulatory agencies requirements dictate that conducted and radiated emissions must be constrained below specified limits, but the unit must also pass immunity/transient requirements.

As shown in Figure 4.4, the electromagnetic interference (EMI) filter, was developed with two main purposes, filter the conducted susceptibility (CS) and the conducted emission (CE) noise.

Electromagnetic compatibility (EMC) has become an essential property of electronic equipment and one of the many EMC tests that a new product must pass before it can be released to market is conducted susceptibility testing.

The conducted susceptibility filter was designed to limit the amount of electrical energy that is conducted from the supply rails into the power supply components, that can cause interference to the normal behaviour of the system. It was developed with a pair of differential coils, RC circuits and capacitors, whose values were chosen so that the nominal current was taken into consideration, as well as the maximum input voltage of 32 V and current of 4 A.

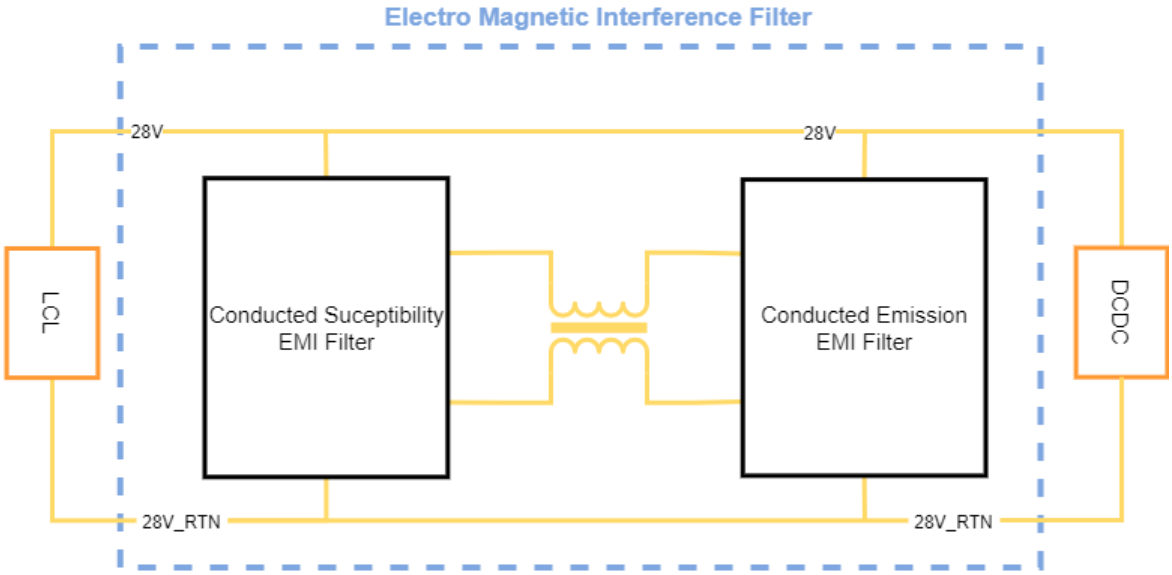


Figure 4.4 – Basic representative diagram of the input electromagnetic interference filter

An EMI filter is made up of two basic types of components, capacitors and inductors. Capacitors shunt noise current away from a load while inductors block or reduce the noise. Generally, single component filters are not very useful as their attenuation only increases at a rate of 20 dB/decade. To achieve greater attenuation, a higher-order filter consisting of two reactive components, or more is required. The value of the inductive or capacitive components is determined by the impedance of the source, load and the highest frequency to be passed (i.e., cut of frequency).

4.1.3. Low-dropout Voltage Regulator of 20V

Before implementing the DC-DC sequence control and converters there was the need to have function circuitry independent of the input voltage. To guarantee that, a linear voltage regulator was used to provide a stable power supply voltage independent of load impedance, input voltage variations, temperature, and time. A low-dropout (LDO) voltage regulator was chosen for this purpose because of its ability to maintain regulation with small differences between supply voltage and load voltage. The chosen LDO is military qualified and can be used up to a differential 40 V. Its output was regulated to 19,16 V with the choice

of resistors on the adjust pin and using capacitors on the output to aid in regulation stability. The representative diagram of this regulator and of the DC-DC sequence control circuit, can both be seen in Figure 4.5.

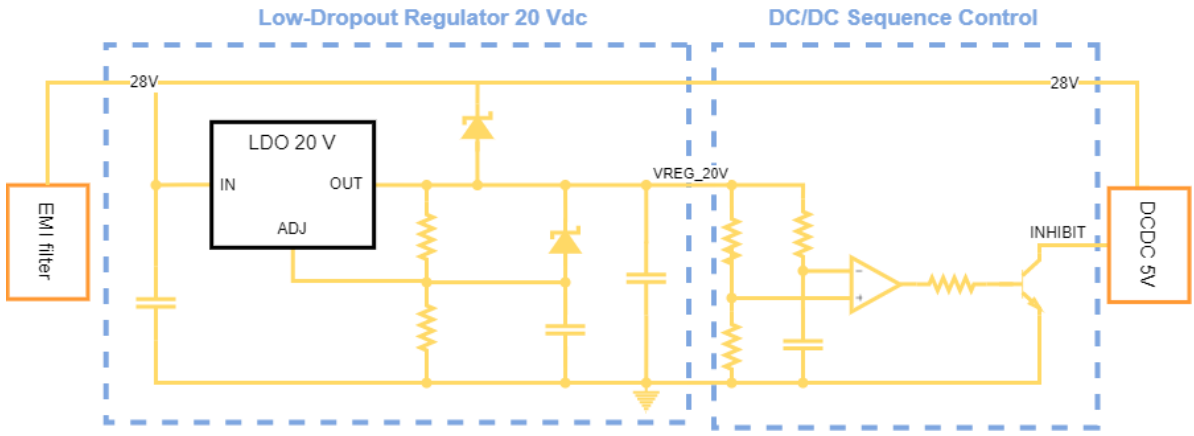


Figure 4.5 – Basic representative diagram of the low-dropout regulator and the DC-DC sequence control circuit

4.1.4. DC-DC Sequence Control

The DC-DC converters chosen, have an inhibit terminal that is used to disable the internal switching, resulting in no output and very low quiescent input current at the 5 V converter. It was implemented a timer sequencer circuit responsible for delaying the start of the 5 V DC-DC converter. This circuit is based on a high threshold and two different RC delay elements. Two individual comparator circuits and two different but well-known RC time constants, allowed to trigger two individual start signals.

4.1.5. DC-DC Converters

High voltage conversions in space applications are in majority DC-to-DC voltage converters [27]. The converters used for this project are constant frequency, pulse-width modulated switching regulators which used a quasi-square wave, single ended, forward converter design. Tight load regulation was maintained by using a wide bandwidth magnetic.

For the PSU to produce the required output voltage levels, the input voltage of 28 Vdc was so stepped down by 2 DC-DC converters that, by means of switching the input power before an internal transformer, power rectifying and filtering on the output, delivered the +12 V and +5 V with the appropriate output current. The two converters are represented in Figure 4.6. The chosen converters provided short circuit and overload protection by constant current-limit feature. This protective system senses current in the converter's secondary stage and limits it to approximately 115 % of the maximum rated output current. The switching frequency of these converters was 550 kHz, and the 12 V DC-DC provided the switching synchronization pulses to synchronize with the 5 V converter. Synchronizing the converter with the system clock allows the designer to confine switching noise to clock transitions, minimizing interference, and reducing the need for filtering. In sync mode, the converter will run at any frequency between 500 kHz and 675 kHz. The sync control operates with a quasi-TTL (transistor-transistor logic) signal at any duty cycle between 40 % and 60 %. This limited the used of pulse width modulation (PWM) to high frequencies, avoiding the *Bartolomeu* PSU critical frequencies between 1 and 3 kHz.

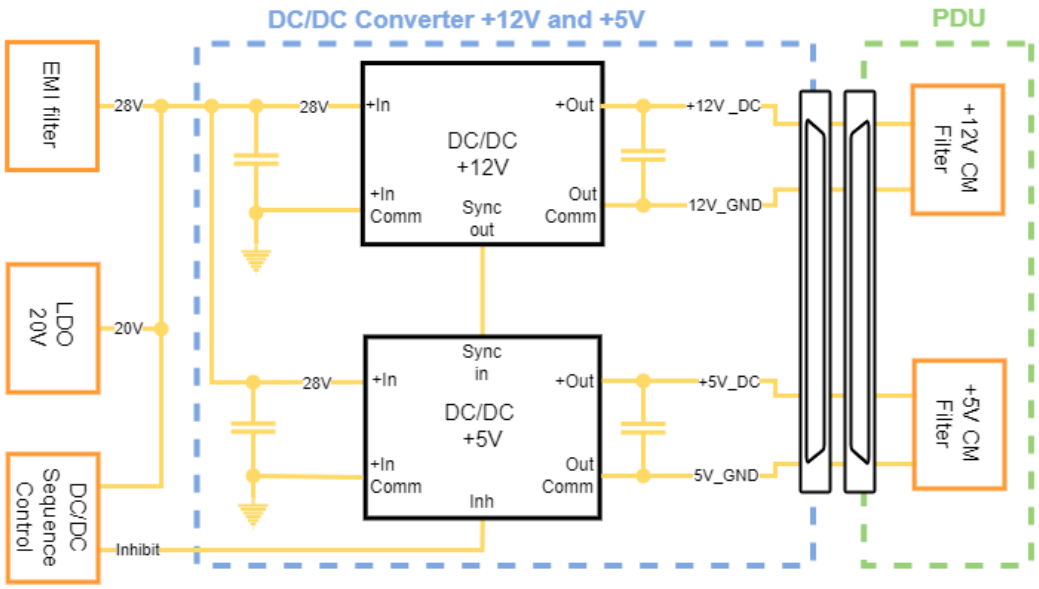


Figure 4.6 – Basic representative diagram of the DC-DC converters circuit

4.1.6. Voltage, Current and Temperature Measurement

To account for the input power being used, there were implemented circuits to measure the voltage and current at the input of the DC-DC converters. Because these measurements are read by an ADC common to many other signals, the range of the signals had to be taken into consideration, as well as the necessary resolution error.

In the case of the voltage measurement, a simple voltage divider, with the appropriate ratio was used and the range for this measurement was from 23 V to 33 V. A representative diagram of this measurement circuit is shown in Figure 4.7.

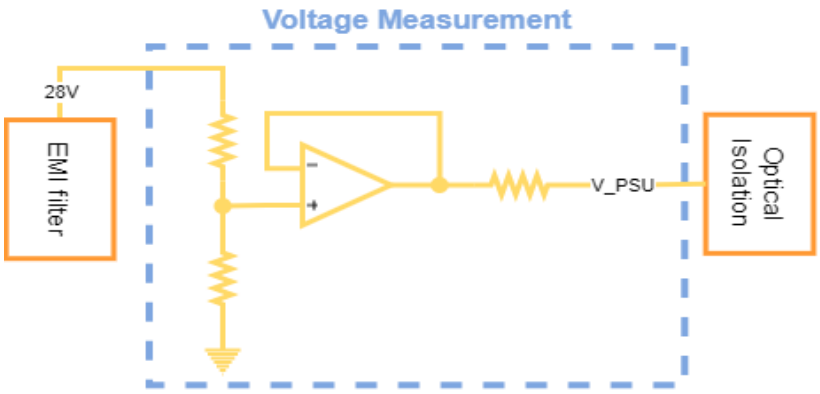


Figure 4.7 – Basic representative diagram of the input voltage measurement circuit

For the current, the measurement was made with the shunt resistor that was also used for the LCL. Because the voltage drop on this resistor is proportional to the current that the load was using, this signal is then amplified by an instrumentation amplifier, passed through a multiplexer, and then digitized on the ADC with the range for this measurement being from 0 A to 10 A on the input. It is possible to see a representation of the instrumentation amplifier in Figure 4.8.

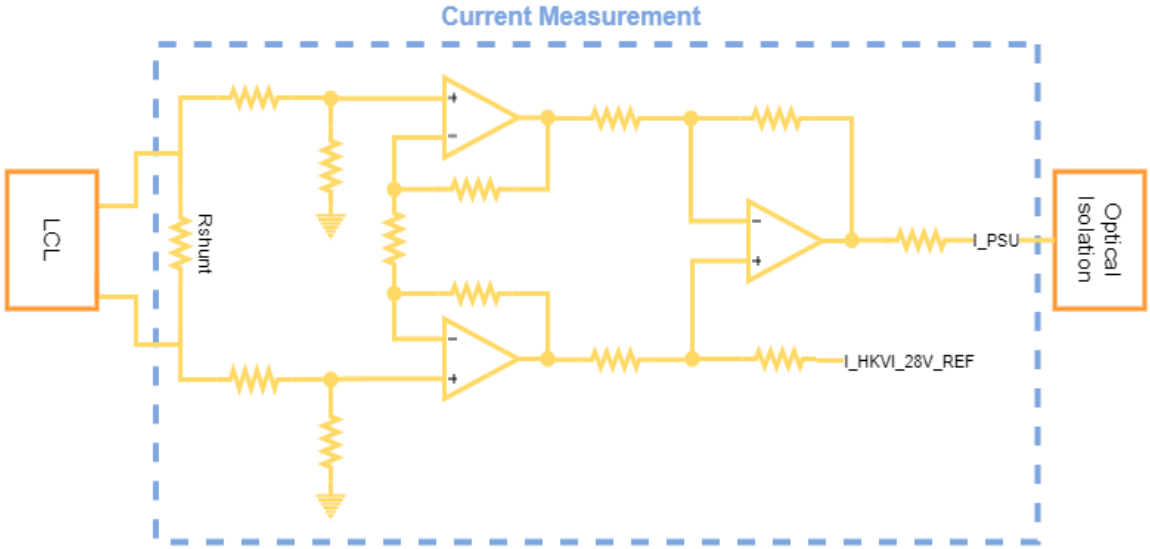


Figure 4.8 – Basic representative diagram of the input current measurement circuit

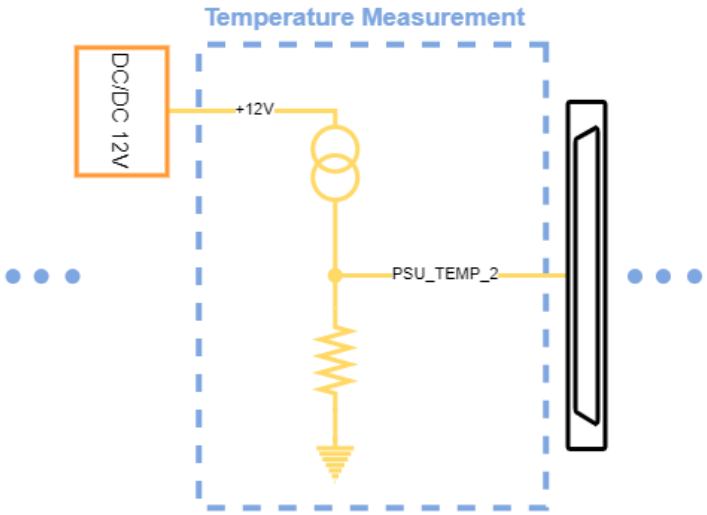


Figure 4.9 – Basic representative diagram of the PSU temperature sensor circuit

For an internal measurement of the hot spots, a temperature transducer was used, whose output is a current value proportional to the absolute temperature, with a well-known and precise temperature to current ratio. The output is afterwards converted into voltage in a precision resistor and measured on the ADC (Figure 4.9).

4.1.7. Over-temperature Protection

The over-temperature protection (OTP) circuit, responsible for triggering the LCL, is based on a circuit that compares the temperature read by a temperature sensor with the specific value set by a resistor divider.

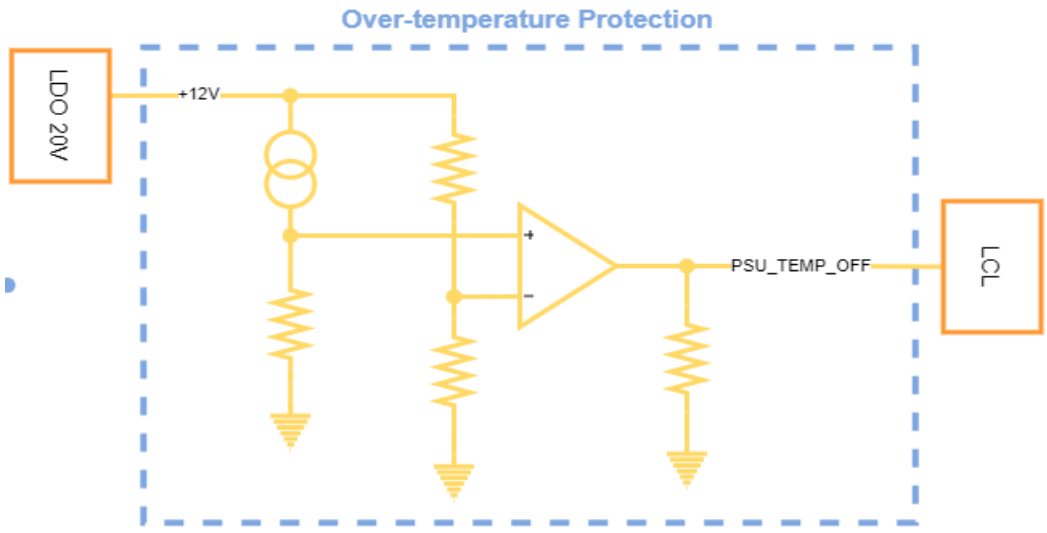


Figure 4.10 – Basic representative diagram of the over-temperature protection circuit

The thermal reference point is located between the two DC-DC converters, so that if this point reaches +95,8 °C the comparator triggers an output that trips the LCL, shutting down the PSDU. The representative diagram of the circuit can be seen in Figure 4.10.

4.1.8. Isolation Optocouplers

The PSDU specifications requires the primary and the secondary powers to be isolated from each other. This is naturally accomplished at the DC-DC converters interface.

However, it was necessary to perform voltage and current measurement on the primary side and pass the signal to the MCU on the PDU. To guarantee the proper isolation while maintaining these functionalities, optical isolators were used to condition the signals from the primary side (PSU) to the secondary side (PDU).

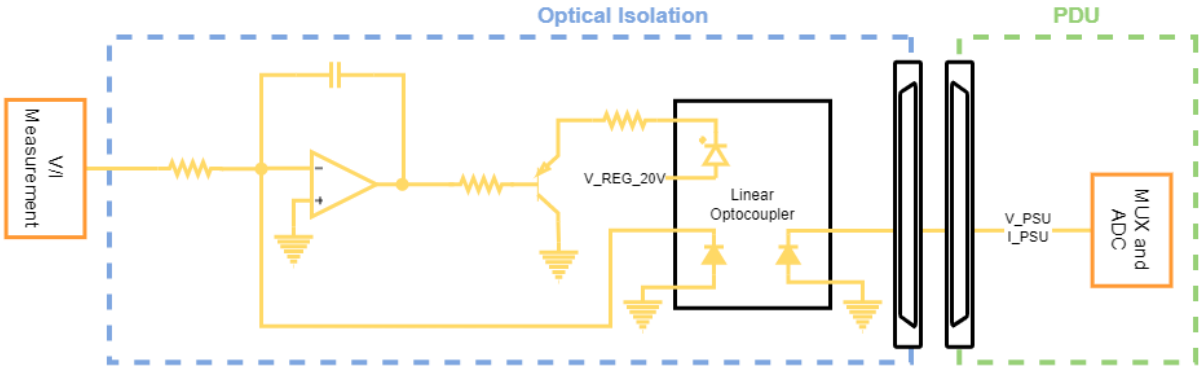


Figure 4.11 – Basic representative diagram of the isolation circuit

The optocoupler, represented in Figure 4.11, consisted of a LED optically coupled with two photodiode detectors. The photodiode on the input side of the device acted as feedback to the LED to maintain constant LED current light output. The output photodiode of the device drove the output circuit and maintained electrical isolation. This device was hermetically sealed and maintained a linear operation in input-output optically coupling. The isolation was achieved using a unity gain amplification stage for high linearity as described in Figure 4.11.

4.2. PDU Detailed Description

The power distribution board was designed to contain the processing unit for controlling the various output switches, controlling a multiplex chain and an ADC for acquiring the several measurements of voltage

and current, as well as a communication interface for the external control unit. Also, integrated into the PDU are common-mode filters for each DC-DC output voltage and a load control circuit responsible of generating the minimum voltage required by the DC-DC to operate. Similarly, circuits for measuring voltage, current and temperature, as well as a protection circuit against under-voltage, have been added to the PDU.

4.2.1. Common Mode Filters

The common-mode current is present on both signal and return paths, often in common phase to each other and is usually generated by imbalances in the circuit such as ripple or electrical noise at the output of the DC /DC converters. To filter this noise, two filters, were placed on secondary side connected to the DC-DC converters. Common-mode filtering involved capacitors to ground the high-frequency noise to the structure earth, a current compensated coil and a larger capacitor for energy storage and lower output impedance.

4.2.2. Load Control Circuit

When the LCL turns on the power to the DC-DC converters primary side, the control unit might take some time to start pulling enough current in the output. So, to achieve a stable behaviour there is the need to provide at least 10% of the sourced output on the secondary side of the converter.

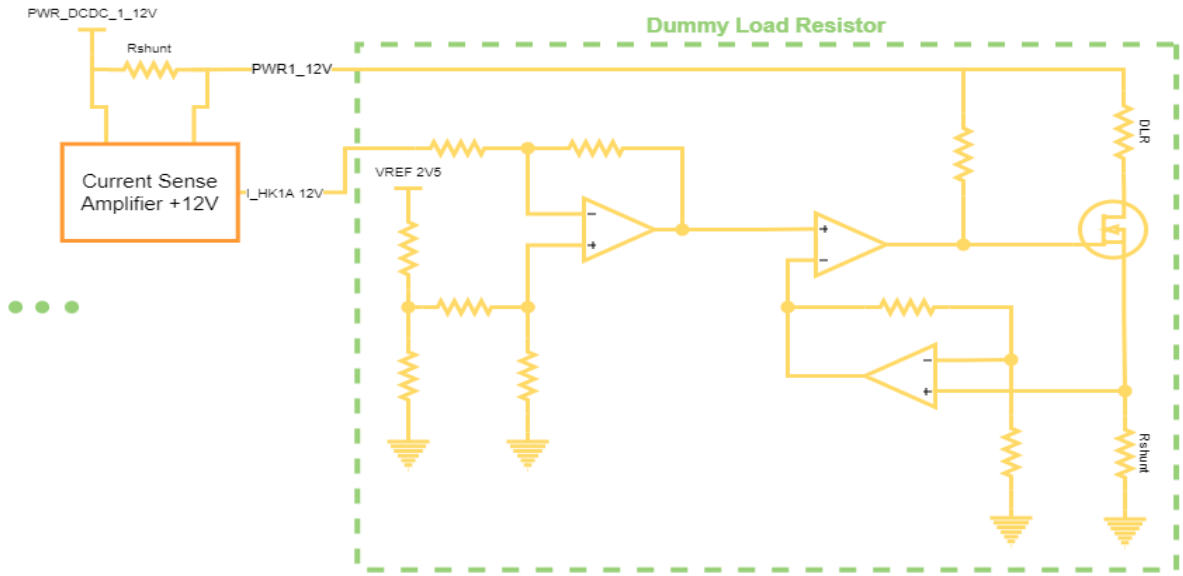


Figure 4.12 – Basic representative diagram of the load control circuit

As so, a circuit to control the value of a resistor, like the one in Figure 4.12 was used to pull current out of the first converter. When the current being pulled by the scientific instruments is enough, this circuit is switched off.

4.2.3. Voltage, Current and Temperature Measurement

Similarly, to the PSU, for the voltage measurement, a simple voltage divider with the appropriate signal conditioning was used before the multiplexer input.

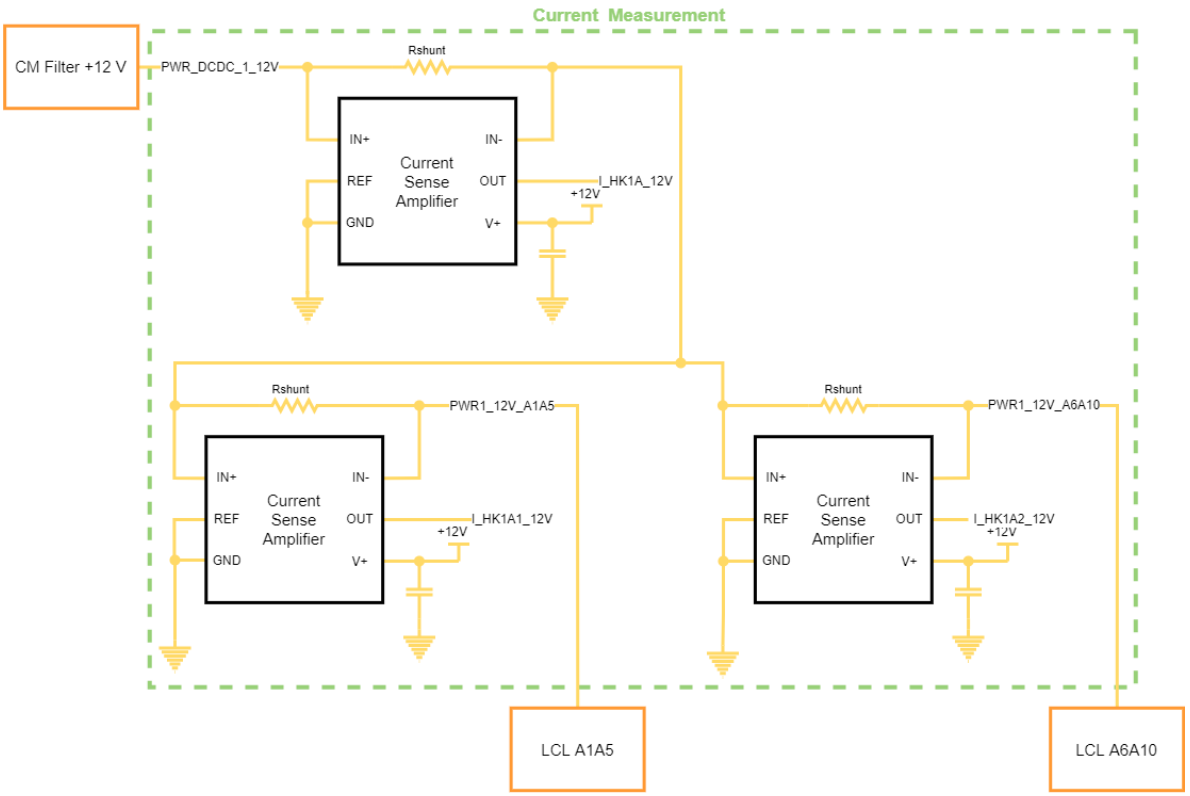


Figure 4.13 – Basic representative diagram of the output current measurements

For the temperature measurement of the internal temperature on the PDU side, a current to voltage conversion based on a temperature sensor was used with the output on the normalized range.

For the current measurement on the secondary side, a sensing resistor, and a fixed gain IC with a wide common mode voltage and external reference, for bi-directional measurement capability are used. As the

gain was 50, the output was selected by choosing the appropriate shunt resistor. The use of this simple integrated circuit saves board space while maintaining performance and accuracy of the measurements. The typical application circuit for this specific IC is depicted in Figure 4.13.

4.2.4. Low-dropout Voltage Regulator of 3,3 V

A low-dropout voltage (LDO) regulator of 3,3 Vdc was chosen to supply the internal microcontroller unit, which is a low current load. The linear regulator was the best solution, especially because the LDO can be supplied by the existing 5 V. If a DC-DC converter was chosen instead of a LDO the risk to get problems with minimum load would be higher.

4.2.5. Voltage Reference of 2,5 V

To have a common reference for all the ADCs, an external, high precision and stable 2,5 V reference IC is used. This reference voltage was also used on the signal conditioning where a shift was necessary, and enabled a reference measurement by the MCU, using a different reference of 12 V, to detect any deviation between the two references, as per the Figure 4.14.

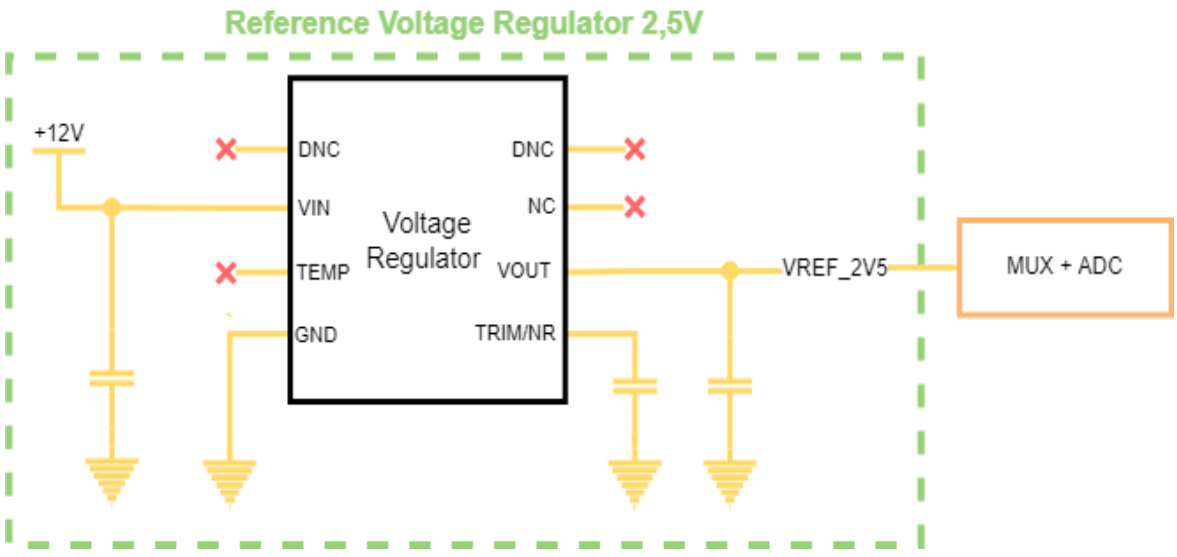


Figure 4.14 – Basic representative diagram of the voltage reference used in the PDU

4.2.6. Multiplexers and Analog-to Digital Converters

By choosing only two analog-to-digital converters (ADC) there was the need to use multiplexers integrated on the ADC IC with 15 analog channels. The input selection is done by the same SPI communication used for data. It is possible to analise the ADCs used on Figure 4.15.

To allow a lower error and high-resolution digitalization of the analog signals, a 12-bit sample and hold with a maximum of 1 MS/s was used. The data from the digitization is sent via SPI interface to the MCU that iterates the conversion data from all the ADCs on the same SPI bus.

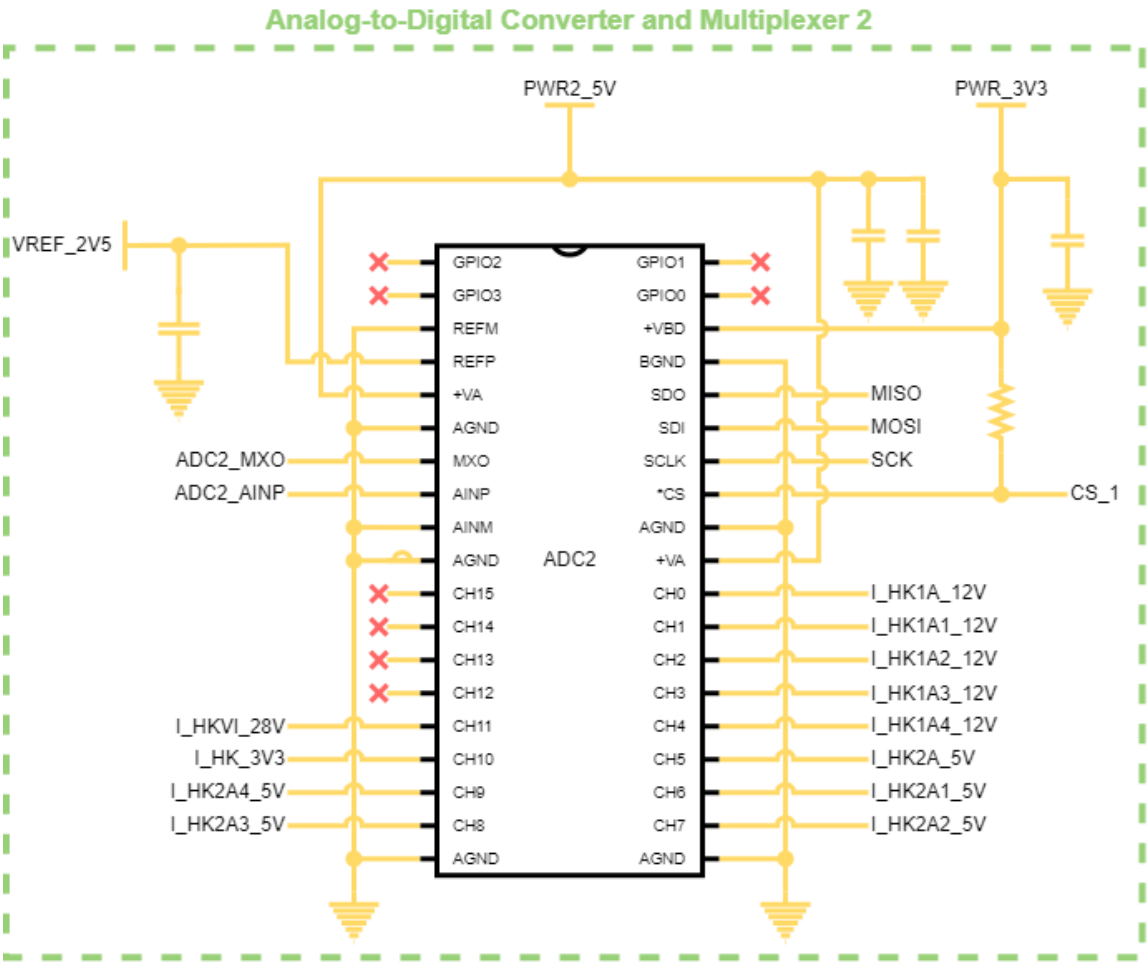


Figure 4.15 – Basic representative diagram of the multiplexer circuit with A/D converter

4.2.7. Signal Conditioning V/I/T

This signal conditioning is used to maximize the use of the dynamic range of the ADC 1 input. As per design, the output of this signal conditioning should be as close as the range of 0 to 2,5 V. It was not always possible to amplify all signals to the full range of the ADC, but the requirements for resolution and accuracy were fulfilled. The schematic of the circuit is displayed on the Figure 4.16.

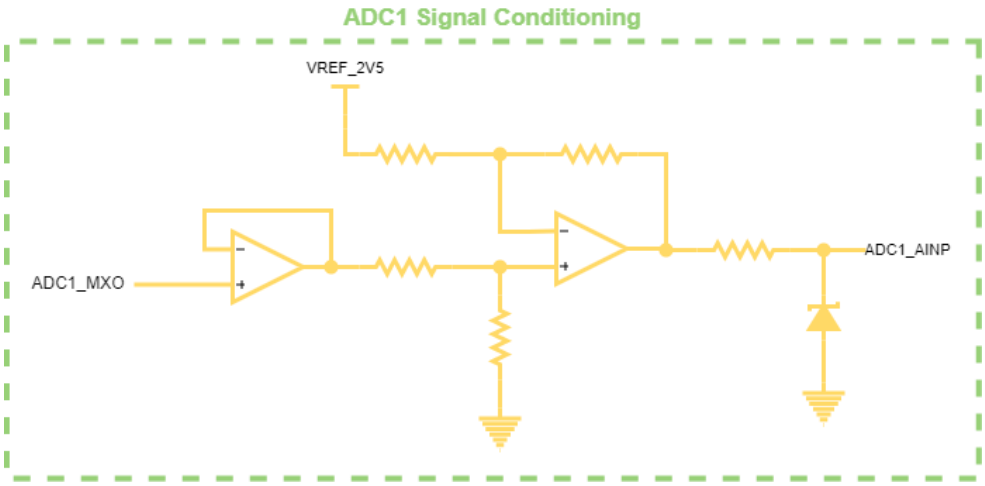


Figure 4.16 – Basic representative diagram of the ADC 1 signal conditioning circuit

For the ADC 2, depicted in Figure 4.17 responsible for the signal conditioning circuit of the current measurements, another circuit was used to buffer the signal before the ADC. The previous stage before the multiplexers should also get the use of the maximum range of the ADC 2 input of 0 to 2,5 V.

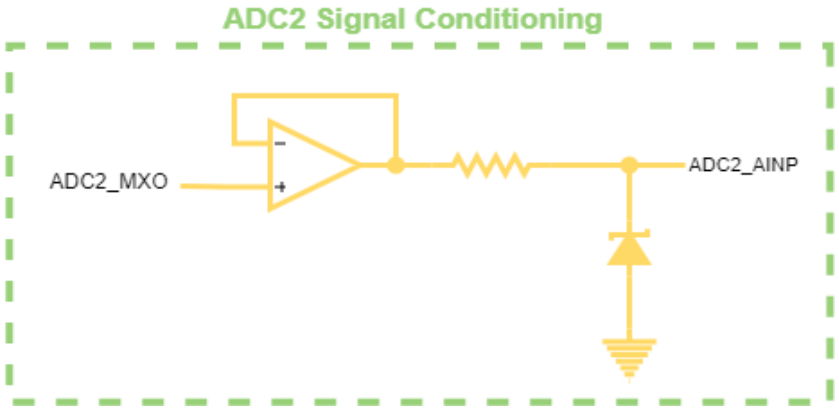


Figure 4.17 – Basic representative diagram of the ADC 2 signal conditioning circuit

4.2.8. Load Switches

The output switches for the output loads at +5 V and at +12 V are controlled by a circuit that is monitored by a flag in the microcontroller. A channel P MOSFET is used to switch on and off the load, and some bipolar transistors, controlled by the MCU output pin, were placed at his gate. If the MCU output is at high level of 3,3 V or in high impedance state, the MOSFET does not turn on the load. For the load to be turned on, the MCU pin must turn low and sink current to bias the PNP transistor and pull the MOSFET gate voltage to a value lower than the Vgs required for conduction. Besides that, all switches featured a soft start to deal with load inrush currents.

In all switchable PSDU outputs was implemented an additional filter for low ripple and noise. To aid in reducing the output ripple, three terminal capacitors are used on that output.

4.2.9. RS422 Transceiver

The MCU board is connected through one bus for the CU communication. The receiver and transmitter of the bus transceiver are always on and cannot be switched off, to assure reception. The used bus transceiver can accept voltages from -10 V to 15 V at its differential inputs without degradation and failure propagation.

4.2.10. PSDU Controller

The main task of the MCU is to communicate with the CU, answer to request commands and execute set commands. It was selected a latch-up immune microcontroller, suitable for the required radiation tolerance. The clock is generated from an external 20 MHz quartz crystal with the built-in oscillator, to allow the lowest error on the selected transmission baud rate. The MCU had a bootloader that allowed for the software to be replaceable in-flight, via the scientific module control unit.

4.2.11. Under-voltage Protection

For an added protection, the PSDU included an additional protection to ensure that a short circuit at any secondary load did not triggered instability of the DC-DCs, possibly leading to PSDU and loads damage. This circuit works for any secondary available voltage and triggers the LCL of the primary side OFF,

through an opto coupler connection. This protects the two positive outputs of the DC-DCs, by sending a signal to shut down the PSDU if at least one of the DC-DCs is not working correctly.

Chapter 5: Electrical Analysis

The evolution from the different design stages was supported by simulations, made by the author of this dissertation, using the LTspice simulator. This is a powerful SPICE software tool from Analog Devices for analysing electrical components and connections. Circuit simulation has become one of the keys to efficient circuit design, as it can be used to test circuit behaviour before an electronic device is built. Simulating the circuit at this point led to avoiding the damage of expensive materials and to replacing impractical components with better performing alternatives. It also helped in identifying technical risks with respect to functional needs, which if not made, could have led to non-compliance with the dependability requirements.

The results of the two analyses mentioned in the state of the art, Worst Case Analysis (WCA) and Part Stress Analysis (PSA) are shown in the chapter . The analyses were made almost simultaneously so it would be easier to find the worst case scenario for each component and in case of finding a non-compliance, re-select the component or redesign the circuit and simulate again.

Improving the PSDU circuit to its acceptance point was a work that took months and hundreds of simulations. However, for the purposes of this dissertation, only the most interesting results obtained are going to be analysed.

5.1. Worst Case Analysis

The Worst Case Analysis (WCA) was carried out for the electronic and electrical equipment to prove that it would function within specifications until the end of its required lifetime, despite certain deviations in the parameters of its components and the given environment [13].

5.1.1. Latching Current Limiter

As explained in chapter 4, the LCL oversees limiting the maximum current that can flow into the PSDU and respective outputs. If the maximum rated output current is reached, the LCL latches the output, after a certain trip-off time. By latching, the LCL places the output in a high-impedance state. Moreover, the

LCL incorporates an over-voltage and under-voltage protection feature, that limits the maximum and minimum allowable operating voltages to 32 and 24 V, respectively.

As can be seen in Figure 5.1 the simulation of the circuit represented in Figure 4.2 starts without any input voltage, represented by the red line labelled pwr_28_v , but as soon as the input voltage appears, the unit powers, green line 28v_lcl_out. The input voltage was simulated with an independent voltage source and a PWL (Piecewise linear) file. The PWL function is used to construct a waveform from a series of straight line segments connecting points defined by the user in a list of two-dimensional points that represent time and value data pairs.

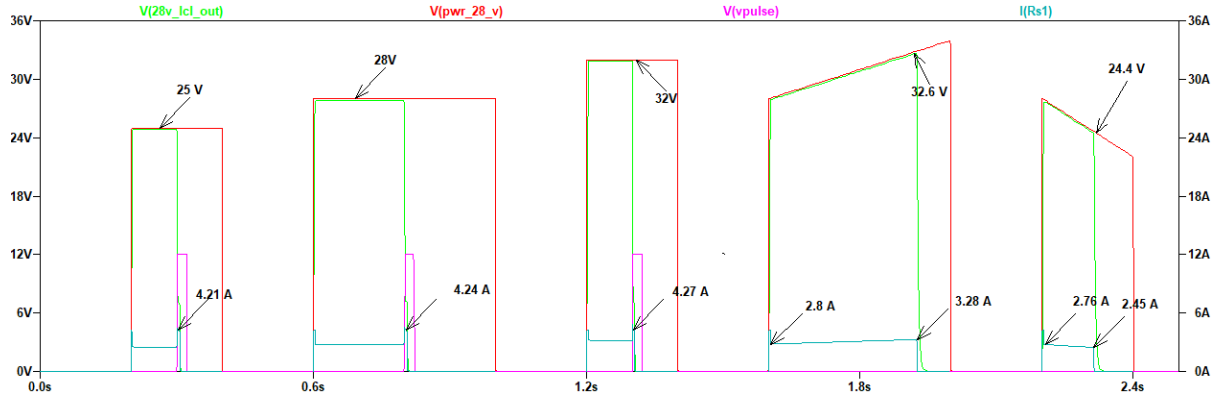


Figure 5.1 – Latching current limiter over and under voltage protection simulation

The first three time periods ([0.2s – 0.4s]; [0.6s – 1s] and [1.2s – 1.4s]) demonstrate the behavior of the circuit when the supply voltage is steady with 25 V, 28 V and 32 V and an over-current in a load of 2 Ω is pulsed for 30 ms every 0,4 s.

The overcurrent was simulated with resistor in series with a switch connected to an independent voltage source and a PWL file, the voltage source is called vpulse and is represented by the pink line. Even with a permanent load of 10 Ω and a 486 µF capacitor in parallel, which is the worst-case scenario for the LCL when powering ON, the LCL behaved as it was supposed to, allowing the input voltage and current to flow to the PSDU until the over-current pulse, the current in the sense resistor is represented by the blue line Rs1.

The LCL latches when the over-current happens, limiting the current to the maximum value during the trip-off time and switching off the PSDU once that time had elapsed.

The fourth and fifth time periods ([1.6s – 2s] and [2.2s – 2.4s]) demonstrate the effect of the over-voltage protection at the high reference point of 32,6 V and the under-voltage protection at the low reference point of 24,4 V. Once these limits are reached the LCL latches, shutting down the PSDU.

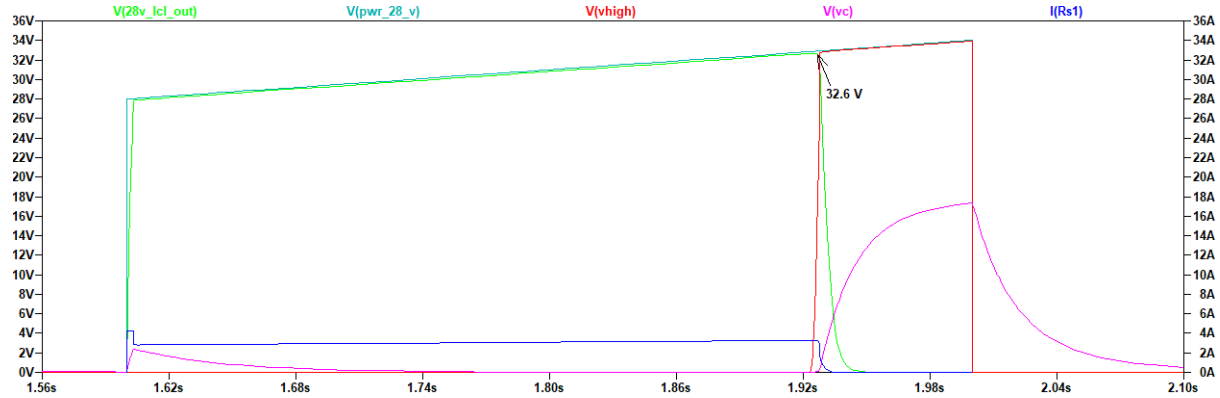


Figure 5.2 – Latching current limiter simulation with the increase of the input voltage

The fourth scenario was amplified in Figure 5.2 and shows the simulation of a supply voltage rise from 28 V to 34 V, exceeding the maximum value and making the over-voltage protection act. As it is seen, when the supply voltage became close to 32,6 V the capacitor started charging, changing the Vgs of the mosfet cutting the power to the load. The capacitor in question is connected to the gate of the mosfet and is responsible for the trip-off time of the LCL.

The fifth scenario was also amplified, in Figure 5.3 and shows the same behaviour but in terms of the under-voltage protection action. A decrease of the supply voltage from 28 V to 20 V made the circuit cut the power when input voltage got close to 24,4 V and the capacitor started charging.

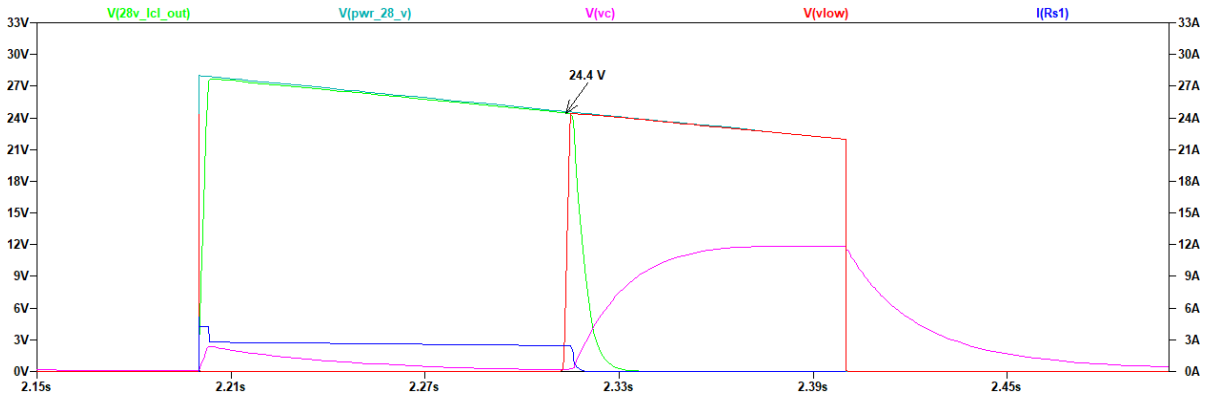


Figure 5.3 – Latching current limiter simulation with the decrease of the input voltage

The following simulation, whose result was represented in the graph of Figure 5.4, was intended to demonstrate a fast rise of Vin from 0 to 24 V in 70 ms, without any pulse being triggered so it was possible to witness both protections working.

In Figure 5.4, once Vin reached 24 V the LCL was "free" to provide current and that happened with the rise of the green line. When Vin became higher than 32 V the LCL went OFF and stayed that way. The load voltage went down slowly due to a 300 µF capacitor discharge.

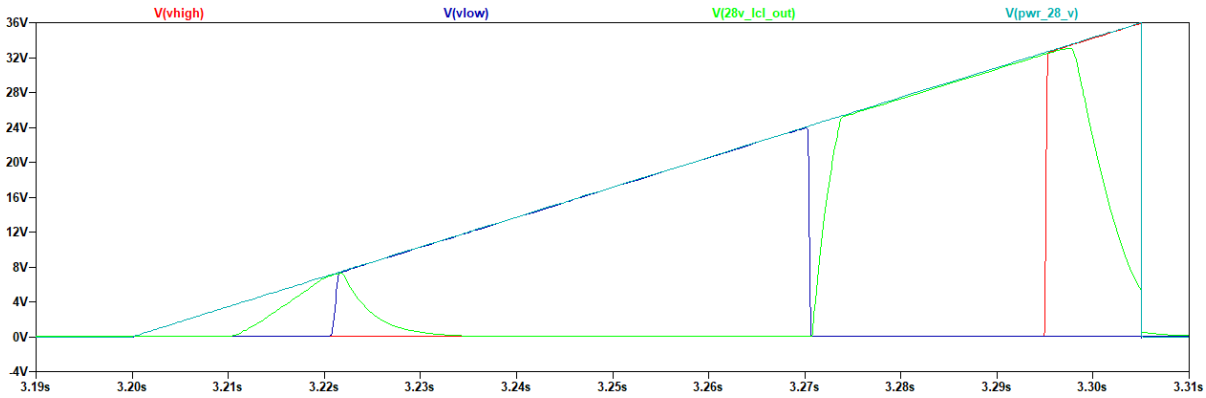


Figure 5.4 – Latching current limiter simulation with a fast rise of the input voltage

To better asses the current limitation and the trip-off times, a last simulation was done to the LCL. In Figure 5.5 and Figure 5.6 the current being provided to the PSDU is limited to approximately 4,04 A, independently of the input voltage (24V of input voltage in Figure 5.5 and 32V in Figure 5.6).

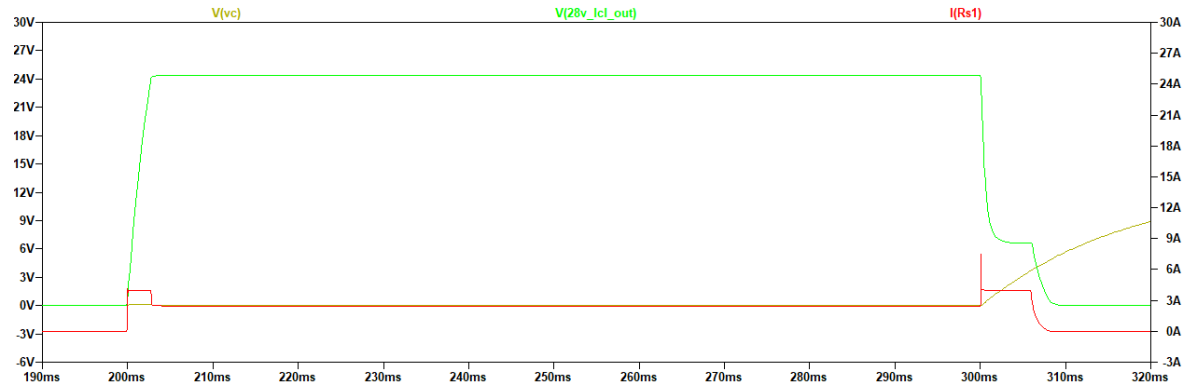


Figure 5.5 – Latching current limiter simulation with a steady input voltage of 24 V and an over-current situation

As expected, the simulations showed that the trip times do change with the input voltage. Therefore, for:

- At 24 V the trip time was approximately 5,89 ms;
- At 32 V the trip time was approximately 4,48 ms.

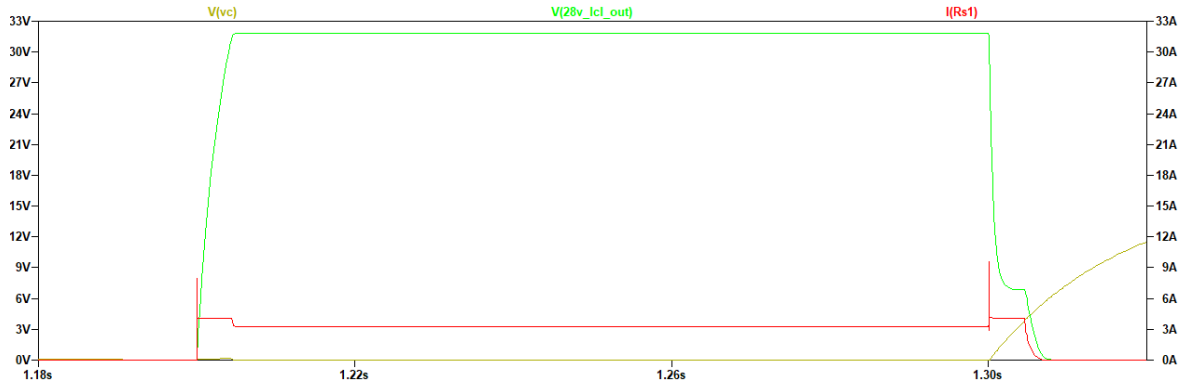


Figure 5.6 – Latching current limiter simulation with a steady input voltage of 32V and an over-current situation

5.1.2. Isolated Primary Side Current Measurement

The results of the simulation of the current measurement circuit in the PSU side, Figure 4.8 , connected to the opto isolation circuit, Figure 4.11 can be seen in Figure 5.7. An independent current source with a sine wave function was placed as a swinging 10 A load, its measurement can be seen in blue (I1) and an independent voltage source with a sine wave function was placed to simulate a swinging input voltage from 0 V to 32 V, represented in red.

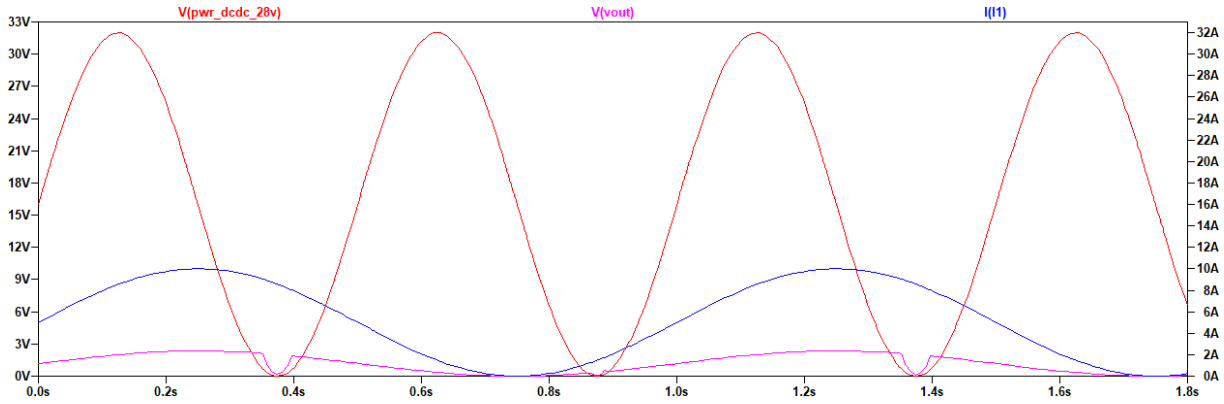


Figure 5.7 – Primary side current measurement simulation

The graphic from Figure 5.7, demonstrates that the circuit is immune to voltage variations up to the point when Vin is too low to provide a stable behaviour. After the instrumentation amplifier the output voltage, pink line, vout, is acquired by the ADC so a value of 2,45 V for a 10 A load is the expected as per equation:

$$V_o = \frac{R3}{R2} x \left(\frac{2\,x\,R1 + Rg}{Rg}\right) x \left(V_{i1} - V_{i2}\right) = 2{,}45\,V$$

5.1.3. Isolated Primary Side Voltage Measurement

The primary side voltage measurement circuit, represented in Figure 4.7 was simulated together with the isolation circuit of Figure 4.11 and the results are shown in Figure 5.8. The same independent voltage source with a sine wave function was placed to simulate a swinging input voltage from 0 V to 32 V, also represented in red.

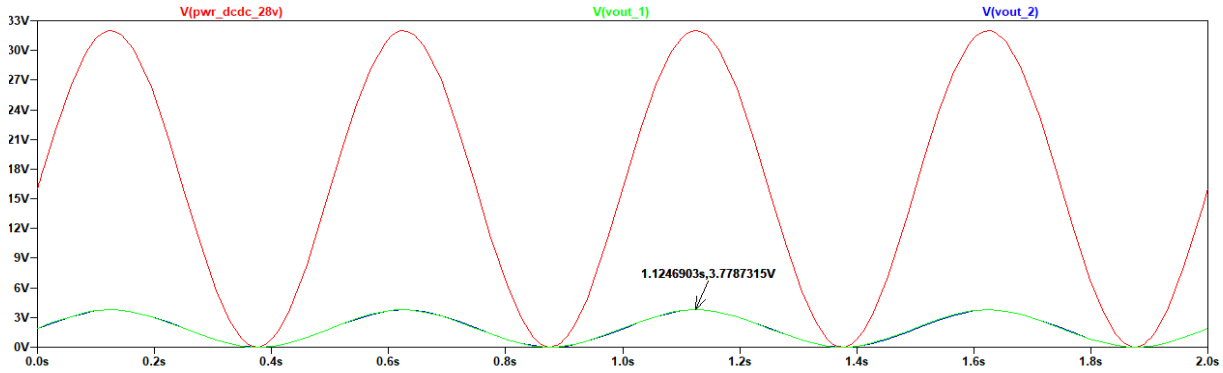


Figure 5.8 – Primary side voltage measurement simulation

The output voltage obtained before the optic isolation, Vout1 and after the optic isolation Vout2 of 3,77 V for 32 V is expected as per the equation:

$$V_o = \frac{R2}{R2 + R1} x\ 32\ V = 3{,}77\ V$$

5.1.4. DC-DC Sequence control

The simulation of the DC-DC sequence control circuit of Figure 4.5 was done together with the 20V voltage regulator to confirm that the delay at the start of the 5V DC-DC was accomplished with a value of approximately 35 ms. As can be seen in Figure 5.9, after 34.33 ms the voltages at the inputs of the operational amplifier becomes equal (vin+ = vin- = 17.80V) and so the output voltage (vout) drops to 0V enabling the DCDC.

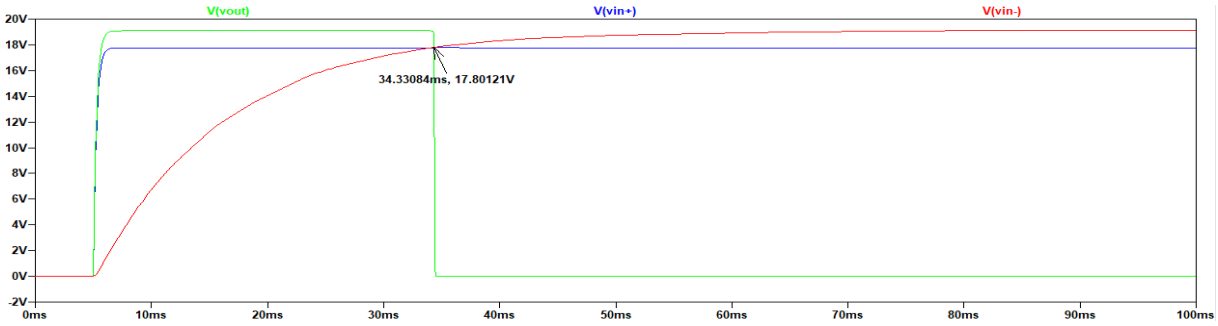


Figure 5.9 – DC-DC sequence control circuit simulation

5.1.5. Load Control Circuit

In order to protect the PSDU at power ON, from unstable DC-DCs due to less than minimum load current, a circuit, shown in Figure 4.12 was implemented to ensure a minimum of 10 % of the 12 V DC-DC actual sourced output. The minimum load the DC-DC will see at power on is approximately 1 A, accounting for the control unit and the module fans. As 10 % of 1 A is approximately 100 mA, the load control circuit accomplished the requirement, adding 100 % margin to the output load. As depicted in Figure 5.10, the circuit pulls approximately 210 mA, blue line, I(Dlr1) until the current being pulled by the load, I(Rs9) is greater than this value.

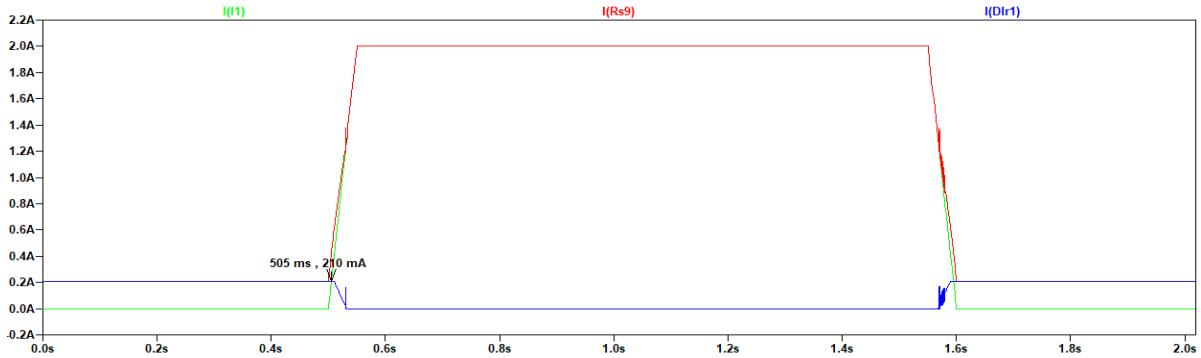


Figure 5.10 – Load Control Circuit simulation with minimum load current

Once the load reaches the 210 mA, the resistor DLR1 is gradually placed off-line by a transistor. The action of the transistor implied the dissipation of heat on it, while in transition from fully ON to OFF. So, to evaluate this, the measurement of the power dissipation on the transistor (pink line) and on the resistor DLR1 (yellow line) was performed and can be seen in Figure 5.11.

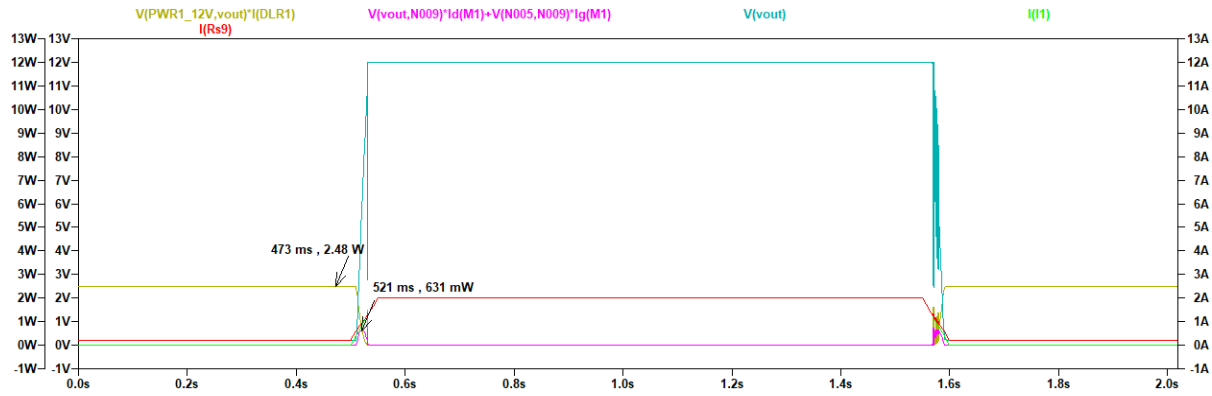


Figure 5.11 – Load Control Circuit simulation of the power dissipation in DLR and transistor

The worst scenario yields to 0,631 W in the transistor and about 2,48 W in DLR1. The duration depends on how fast the loads were turned ON to reduce the need for DLR1.

5.1.6. Secondary Undervoltage Protection

The results in Figure 5.12 evidence the moments where the output of the under-voltage protection circuit detects that one of the DC-DC is not supplying the correct voltage level, sending a high-level signal to the LCL. The simulation was performed with two independent voltage sources providing 5V (red line) and 12V (blue line) to simulate de DCDC outputs. Before the 4 s mark only the 5V DC-DC is working so so a siand after the 13 s mark only the 12 V DCDC (blue line) is supplying, so the circuit sends a signal (green line) to switch OFF the PSDU on both moments. Because both DC-DC are working between approximately the 7 to 8.5 second mark, the voltage level at the output of circuit went down and no signal was sent to the LCL, so the PSDU was not shutdown.

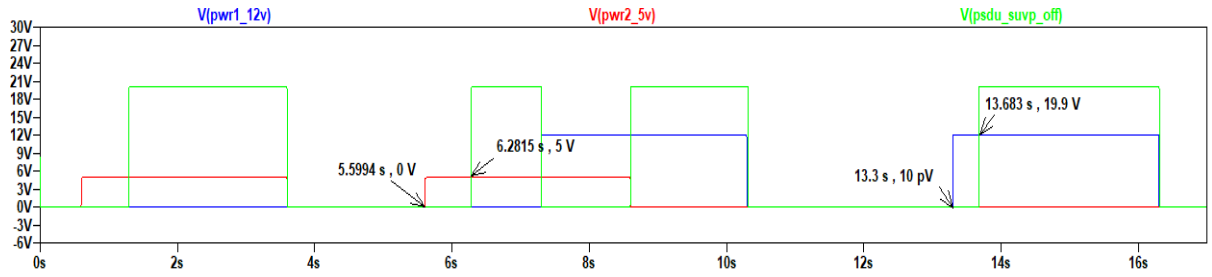


Figure 5.12 – Combinations of operation for the Secondary Under Voltage protection

As it is demonstrated in Figure 5.13, at power ON, the circuit waits approximately 332 ms before implementing the combinatory table, leaving enough time for all DC-DCs to come to a stable state. This circuit was simulated together with the LCL to be possible to witness the signal being received by the LCL and its trip-off time capacitor starting to charge, and the load being switched off. The result of this simulation is shown in Figure 5.13.

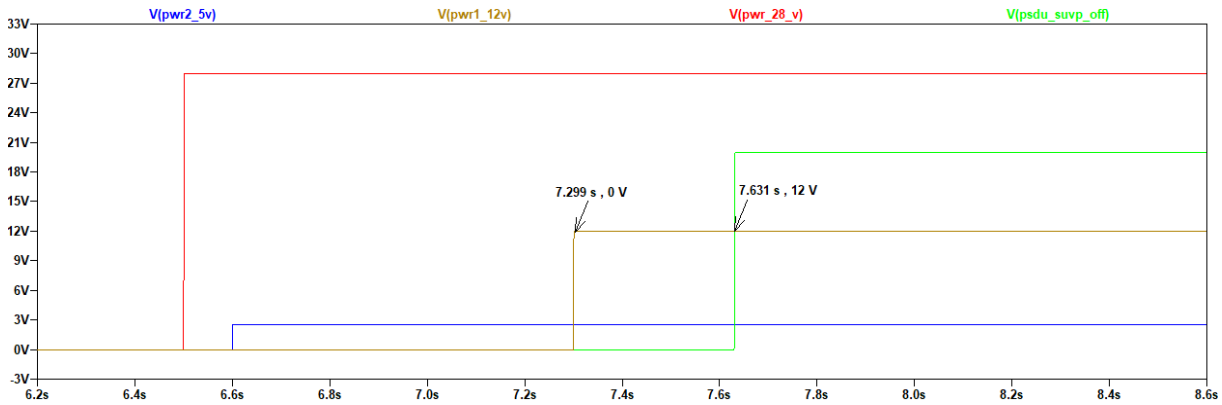


Figure 5.13 – Under-voltage protection output voltage delay time

5.2. Part Stress Analysis

The scope of this section is to explain how the analysis of the stress applied to some of the electrical parts of the Power Supply and Distribution Unit for the module was performed. The goal was to verify that no component was over stressed even under worst case situations. For confidentiality reasons, the modifications made to the circuits to reach this stage, as well the results of the complete analyses cannot be shown in here.

Some of the results of the analysis performed are shown in Table 5-1. On the first line of the first table, for example, all instances of a specific capacitor were analyzed and the one in worst conditions was selected to perform the PSA. The capacitor has a rating voltage of 50 V, and this parameter must be derated to 60% of its value, so the maximum allowed voltage that can appear at its terminals is 60% of 50 V, i.e., 30 V. By analyzing all circuits where this capacitor is present, it is possible to note that maximum possible voltage at its terminals is 20 V. Since the derated stress is the Max Stress / Max permit. i.e., 66.7% and this is less than 100%, the component is compliant.

Table 5-1 – Part stress analysis of the capacitors

Type	Description	QA level	Parameter	Units	Rating	Derating	Max. Permit.	Max Stress	Derated Stress %	Compliance
Capacitor	C CER 100nF 5% 50V X7R 0805	AUTO	Voltage	V	50	0.6	30	12	40%	YES
			Tcase	°C	125	0.88	110	85	77%	YES
Capacitor	C CER 10uF 10% 35V X7R 1206	AUTO	Voltage	V	35	0.6	21	12	57	YES
			Tcase	°C	125	0.88	110	85	77%	YES
Capacitor	C CER 18pF 5% 50V C0G 0805	AUTO	Voltage	V	50	0.6	30	12	40%	YES
			Tcase	°C	125	0.88	110	85	77%	YES
Capacitor	C CER 1nF 5% 50V X7R 0805	AUTO	Voltage	V	50	0.6	30	12	40%	YES
			Tcase	°C	125	0.88	110	85	77%	YES
Capacitor	C CER 1uF 10% 50V X7R 0805	AUTO	Voltage	V	50	0.6	30	12	40%	YES
			Tcase	°C	125	0.88	110	85	77%	YES
Capacitor	C CER 22uF 10% 35V X7R C-6053	AUTO	Voltage	V	35	0.6	21	12	57%	YES
			Tcase	°C	125	0.88	110	85	77%	YES
Capacitor	C FILT 3-terminal 100nF 20% 50V 6A 1206	AUTO	Voltage	V	50	0.6	30	12	40%	YES
			Tcase	°C	125	0.88	110	85	77%	YES
Capacitor	C CER 22uF 5% 100V X7R C-5750	AUTO	Voltage	V	75	0.6	45	32	71%	YES
			Tcase	°C	125	0.88	110	85	77%	YES

Capacitor	C CER 4.7uF 20% 100V X7S 1210	AUTO	Voltage	V	100	0.6	60	32	53%	YES
			Tcase	°C	125	0.88	110	85	77%	YES
Capacitor	C CER 4.7uF 10% 50V X7R 1206	AUTO	Voltage	V	50	0.6	30	6	20%	YES
			Tcase	°C	125	0.88	110	85	77%	YES
Capacitor	C CER 47pF 5% 50V C0G 0805	2 - Q	Voltage	V	50	0.6	30	5	17%	YES
			Tcase	°C	125	0.88	110	85	77%	YES
Capacitor	C TAN 1uF 10% 50V CWR09 2010	2 - Q	Voltage	V	50	0.6	30	18.1	60%	YES
			Tcase	°C	125	0.88	110	85	77%	YES
Capacitor	C CER 100nF 10% 100V CDR35 1825	2 - Q	Voltage	V	100	0.6	60	32	53%	YES
			Tcase	°C	125	0.88	110	85	77%	YES
Capacitor	C CER 100nF 10% 50V CDR33 1210	2 - Q	Voltage	V	50	0.6	30	19.8	66%	YES
			Tcase	°C	125	0.88	110	85	77%	YES
Capacitor	C CER 22nF 10% 100V CDR33 1210	2 - Q	Voltage	V	100	0.6	60	32	53%	YES
			Tcase	°C	125	0.88	110	85	77%	YES
Capacitor	C CER 330nF 10% 50V CDR35 1825	2 - Q	Voltage	V	50	0.6	30	19.8	66%	YES
			Tcase	°C	125	0.88	110	85	77%	YES

The following tables, Table 5-2, Table 5-3 and Table 5-4, show the same analysis applied to some of the inductors, resistors, and diodes of the circuit, respectively.

Table 5-2 – Part stress analysis of the Inductors

Type	Description	QA level	Parameter	Units	Rating	Derating	Max. Permit.	Max Stress	Derated Stress %	Compliance
Inductor	L CORE 100u MPP 28mm C055930A2	-	Min Isolation Voltage	V	600	0,5	300	40	13%	Yes
			AWG16 Wire Current	A	13	0,75	9,75	9	92%	Yes
			Core and wire max Temp.	°C	200	0,75	150	85	57%	Yes
Inductor	L CMODE 75uH AL1488 13mm ZJ41303TC	-	Min Isolation Voltage	V	600	0,5	300	40	13%	Yes
			AWG16 Wire Current	A	13	0,75	9,75	9	92%	Yes
			Core and wire max Temp.	°C	200	0,75	150	85	57%	Yes
Inductor	L CORE 20u MPP 18mm C055377A2	-	Min Isolation Voltage	V	600	0,5	300	40	13%	Yes
			AWG16 Wire Current	A	13	0,75	9,75	9	92%	Yes
			Core and wire max Temp.	°C	200	0,75	150	85	57%	Yes
Inductor	L CM CHOKE 14uH 6A 900R 100V	AUTO	Maximum operating voltage	V	100	0,5	50	12	24%	Yes
			Hot spot temperature	°C	125	20	105	85	81%	Yes
Inductor	L CM CHOKE 6uH 10A 400R 100V	AUTO	Maximum operating voltage	V	100	0,5	50	12	24%	Yes
			Hot spot temperature	°C	125	20	105	85	81%	Yes

Table 5-3 – Part stress analysis of the Resistors

Type	Description	QA level	Parameter	Units	Rating	Derating	Max. Permit.	Max Stress	Derated Stress %	Compliance
Resistor	R 100k 1% 100ppm 1/8W 50V 0805	AUTO	Voltage	V	50	0.8	40	5	13%	Yes
			Power Dissipation	mW	125	0.5	62.5	0.25	0%	Yes
			Tcase	°C	125	1	125	85	68%	Yes
Resistor	R 100mR 1% 75ppm 1/8W 0805	AUTO	Voltage	V	0.112	0.8	0.089	0.05	56%	Yes
			Power Dissipation	mW	125	0.5	62.5	25	40%	Yes
			Tcase	°C	125	1	125	85	68%	Yes
Resistor	R 10k 1% 100ppm 1/8W 50V 0805	AUTO	Voltage	V	50	0.8	40	12	30%	Yes
			Power Dissipation	mW	125	0.5	62.5	14	22%	Yes
			Tcase	°C	125	1	125	85	68%	Yes
Resistor	R 10mR 1% 75ppm 1W 2010	AUTO	Voltage	V	0.1	0.8	0.08	0.05	63%	Yes
			Power Dissipation	mW	1000	0.5	500	250	50%	Yes
			Tcase	°C	125	1	125	85	68%	Yes
Resistor	R 1k 1% 100ppm 1/8W 50V 0805	AUTO	Voltage	V	50	0,8	40	5	13%	Yes
			Power Dissipation	mW	125	0,5	62,5	25	40%	Yes
			Tcase	°C	125	1	125	85	68%	Yes
Resistor	R 120R 1% 100ppm 1/8W 50V 0805	AUTO	Voltage	V	50	0.8	40	12	30%	Yes
			Power Dissipation	mW	125	0.5	62.5	12	19%	Yes
			Tcase	°C	125	1	125	85	68%	Yes
Resistor	R 12k 1% 100ppm 1/8W 50V 0805	AUTO	Voltage	V	50	0.8	40	12	30%	Yes
			Power Dissipation	mW	125	0.5	62.5	0.85	1%	Yes
			Tcase	°C	125	1	125	85	68%	Yes
Resistor	R 25mR 1% 75ppm 1/2W 1206	AUTO	Voltage	V	50	0,8	40	0,05	0%	Yes
			Power Dissipation	mW	500	0,5	250	100	40%	Yes
			Tcase	°C	125	1	125	85	68%	Yes
Resistor	R 14mR 1% 75ppm 1/2W 1206	AUTO	Voltage	V	50	0.8	40	0.05	0%	Yes
			Power Dissipation	mW	500	0.5	250	171.5	69%	Yes
			Tcase	°C	125	1	125	85	68%	Yes
Resistor	R 16mR 1% 75ppm 1/2W 1206	AUTO	Voltage	V	50	0.8	40	0.05	0%	Yes
			Power Dissipation	mW	500	0.5	250	144	58%	Yes
			Tcase	°C	125	1	125	85	68%	Yes
Resistor	R 18k2 1% 100ppm 1/8W 50V 0805	AUTO	Voltage	V	50	0.8	40	10	25%	Yes
			Power Dissipation	mW	125	0.5	62.5	3.21	5%	Yes
			Tcase	°C	125	1	125	85	68%	Yes
Resistor	R 1k 1% 100ppm 1/8W 50V 0805	AUTO	Voltage	V	50	0.8	40	5	13%	Yes
			Power Dissipation	mW	125	0.5	62.5	25	40%	Yes
			Tcase	°C	125	1	125	85	68%	Yes
Resistor	R 22k 1% 100ppm 1/8W 50V 0805	AUTO	Voltage	V	50	0,8	40	12	30%	Yes
			Power Dissipation	mW	125	0,5	62,5	6,54	10%	Yes
			Tcase	°C	125	1	125	85	68%	Yes

Type	Description	QA level	Parameter	Units	Rating	Derating	Max. Permit.	Max Stress	Derated Stress %	Compliance
Resistor	R 27mR 1% 75ppm 1/8W 0805	AUTO	Voltage	V	50	0,8	40	0,027	0%	Yes
			Power Dissipation	mW	125	0,5	62,5	27	43%	Yes
			Tcase	°C	125	1	125	85	68%	Yes
Resistor	R 33k 1% 100ppm 1/8W 50V 0805	AUTO	Voltage	V	50	0,8	40	12	30%	Yes
			Power Dissipation	mW	125	0,5	62,5	4,36	7%	Yes
			Tcase	°C	125	1	125	85	68%	Yes
Resistor	R 39R 1% 100ppm 1/8W 0805	AUTO	Voltage	V	150	0,8	120	0,025	0%	Yes
			Power Dissipation	mW	125	0,5	62,5	17	27%	Yes
			Tcase	°C	150	0,835	125	85	68%	Yes
Resistor	R 3k3 1% 100ppm 1/8W 50V 0805	AUTO	Voltage	V	50	0,8	40	12	30%	Yes
			Power Dissipation	mW	125	0,5	62,5	43,63	70%	Yes
			Tcase	°C	125	1	125	85	68%	Yes
Resistor	R 3R65 1% 100ppm 1/8W 50V 0805	AUTO	Voltage	V	50	0,8	40	5,15	13%	Yes
			Power Dissipation	mW	125	0,5	62,5	4	6%	Yes
			Tcase	°C	125	1	125	85	68%	Yes
Resistor	R 4k7 1% 100ppm 1/8W 50V 0805	AUTO	Voltage	V	50	0,8	40	5	13%	Yes
			Power Dissipation	mW	125	0,5	62,5	5,31	8%	Yes
			Tcase	°C	125	1	125	85	68%	Yes
Resistor	R 56mR 1% 75ppm 1/8W 0805	AUTO	Voltage	V	50	0,8	40	0,028	0%	Yes
			Power Dissipation	mW	125	0,5	62,5	14	22%	Yes
			Tcase	°C	150	0,835	125	85	68%	Yes
Resistor	R 5k1 1% 100ppm 1/8W 50V 0805	AUTO	Voltage	V	50	0,8	40	5	13%	Yes
			Power Dissipation	mW	125	0,5	62,5	4,9	8%	Yes
			Tcase	°C	125	1	125	85	68%	Yes
Resistor	R 8mR 1% 75ppm 1W 2010	AUTO	Voltage	V	50	0,8	40	0,028	0%	Yes
			Power Dissipation	mW	1000	0,5	500	0,048	0%	Yes
			Tcase	°C	170	0,735	125	85	68%	Yes
Resistor	R 10mR 1% 60ppm 2W 2512	1 - ESCC B	Voltage	V	200	0,8	160	0,1	0%	Yes
			Power Dissipation	mW	2000	0,5	1000	810	81%	Yes
			Tcase	°C	170	0,735	125	85	68%	Yes
Resistor	R 10R 1% 50ppm 2W 500V MIL THT	2 - Q	Voltage	V	500	0,8	400	32	8%	Yes
			Power Dissipation	mW	2000	0,5	1000	0	0%	Yes
			Tcase	°C	250	0,5	175	85	49%	Yes
Resistor	R 1R 1% 100ppm 1/8W 0805	AUTO	Voltage	V	50	0,8	40	0,3	1%	Yes
			Power Dissipation	mW	125	0,5	62,5	44	70%	Yes
			Tcase	°C	150	0,835	125	85	68%	Yes
Resistor	R 100R 1% 100ppm 1/4W 100V MIL 1206	2 - Q	Voltage	V	100	0,8	80	0,1	0%	Yes
			Power Dissipation	mW	250	0,5	125	0	0%	Yes
			Tcase	°C	150	0,835	125	85	68%	Yes

Table 5-4 – Part stress analysis of the Diodes

Type	Description	QA level	Parameter	Units	Rating	Derating	Max. Permit.	Max Stress	Derated Stress %	Compliance
Diode	D SCH DUAL CA BAT54AW SOT32	AUTO	Forward Current (If)	mA	200	0.75	150	50	33%	YES
			Reverse Voltage (Vr)	V	30	0.75	22.5	12	53%	YES
			Dissipated Power (Pd)	mW	200	0.5	100	40	40%	YES
			Junction Temperature (Tj)	°C	150	0.73	110	85	77%	YES
Diode	D TVS ESD QUAD 30kV 5V3 400W 22A ESDA5V3SC6Y SOT23-6L	AUTO	Dissipated Power (Pd)	W	300	0.65	195	0	0%	YES
			Junction Temperature (Tj)	°C	150	0.73	110	85	77%	YES
Diode	D ZN 3.0V 350mW MMBZ4619-HE3-08 SOT233	AUTO	Current (Izm)	mA	85	0.65	55.25	16	29%	YES
			Junction Temperature (Tj)	°C	150	0.73	110	85	77%	YES
Diode	D SCH 70V 33mA 1N5711UR-1 DO213AA	2 - Q	Forward Current (If)	mA	33	0.75	24.75	1.6	6%	YES
			Reverse Voltage (Vr)	V	70	0.75	52.5	32	61%	YES
			Dissipated Power (Pd)	mW	15	0.5	7.5	1.6	21%	YES
			Junction Temperature (Tj)	°C	150	0.73	110	85	77%	YES
Diode	D TVS 30.8V 49.9V 30A 1N5646A DO13	2 - Q	Dissipated Power (Pd)	mW	1000	0.65	650	0	0%	YES
			Junction Temperature (Tj)	°C	150	0.73	110	85	77%	YES

With this analysis, some components have been found to be over the parameter value after derating and needed a re-selection, in order to keep the design and capability to be within the limits.

Chapter 6: Conclusions

The work presented in this dissertation concerns the analysis of a custom power supply and distribution unit for scientific exobiology facility in the International Space Station (ISS). As an application-specific, custom-engineered PSDU it will deliver exactly what is expected and did not involve redesigning the system to fit the range of what a COTS unit could supply. Since this unit will have the lives of the crew that work on the ISS and operational goals that depend upon its reliable performance, the benefits gained from this custom design far outweigh any financial or time-related constraints.

However, building electronic systems for high-reliability space applications requires diligent application of the best practices, use of the highest-reliability parts and materials, proven manufacturing processes and rigorous testing under environmental conditions that bracket the expected conditions in orbit.

Worst Case Analysis was how it was concluded that the circuitry will work as intended given that each constituent part will be subject to such variations over life. WCA, proved that, even if all parameters of all parts were to change simultaneously to their most unfavourable values, the circuit will still have a very high probability of meeting its performance requirements over the mission life.

At last, to prove the design robustness, the Parts Stress Analysis (PSA) to all components of the circuit determined the optimal operating range for each component using derating guidelines and allowed to verify that all selected components will work below their normal operating limit. This will reduce the deterioration rate of the component and minimize failures attributed to extreme operating conditions. Thus concluding, that on the one hand the average strength of the circuit has been increased as much as possible and that on the other hand the average stress has been reduced to its lowest.

6.1. Future Work

To assess the failure modes and identify the causes of potential failures while also analyzing their impacts on the system, a Failure Mode, Effects, and Criticality analysis (FMECA) must be performed. With this analysis it will be possible to infer if any of subsystems presents Single Point Failures (SPF) that could be catastrophic, causing loss of life, be life-threatening or permanently disabling someone. It will also show

that there will be no loss of an interfacing manned flight system, sever detrimental environmental effects, loss of launch site facilities or even complete loss of the system.

To complete the detailed design definition of the system at all levels, the printed circuit board (PCB) must be designed. Once the PCB is designed, all activities related to production, development testing and pre-qualification of the selected critical elements and components can begin. This phase includes the completion of the assembly, integration and test planning for the system and its components, a preliminary user manual and an update of the risk assessment. Once the first produced system is approved, the flight model qualification and production phases starts. The main tasks in this phase are the production, assembly and testing of the flight hardware, the interoperability tests between the space and ground segments and the preparation of the acceptance data package. Finally, launch and early orbital operations, as well as on-orbit verification and operations, are performed to achieve mission objectives and support the mission. In addition, a disposal plan must be prepared for when the mission ends.

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