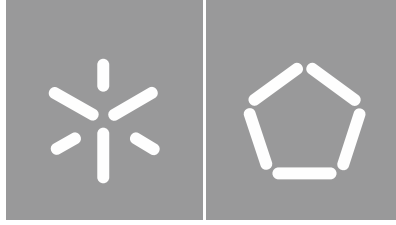


Universidade do Minho
Escola de Engenharia

Vitor Filipe Henriques da Silva

RF graphene oscillators
for biomedical applications



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RF graphene oscillators for biomedical applications

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Trabalho efetuado sob a orientação do(a)
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Professor Doutor João Pedro S. H. A. Alpuim

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Resumo

O grafeno, um material com estrutura atômica e com propriedades excepcionais, tem despertado interesse na comunidade acadêmica. Com uma elevada mobilidade de portadores, excelente condutividade térmica e características eletrônicas notáveis, o grafeno apresenta um enorme potencial para aplicações em eletrônica de radiofrequência (RF). Contudo, a integração deste material em dispositivos eletrônicos apresenta desafios, especialmente na adaptação dos processos convencionais de fabrico CMOS (*Complementary Metal-Oxide-Semiconductor*). Esta tese aborda esses desafios, avançando no desenvolvimento de métodos de desenho, fabrico e caracterização de transístores e osciladores de RF baseados em grafeno, com especial enfoque em aplicações biomédicas. Para melhorar o desempenho dos transístores de RF fabricados, foram implementadas várias estratégias, como a utilização de *gates* enterradas para reduzir a resistência da *gate*, a minimização da resistência de acesso através de um processo *Damascene* adaptado, o uso de substratos de silício de alta resistividade com camadas de SiO₂ para mitigar efeitos parasitas e a integração de camadas finas de óxidos com elevada constante dielétrica (alumina) depositados por deposição de camada atômica (ALD).

Duas metodologias de fabrico distintas foram desenvolvidas: um processo de *gate* traseira sem planarização da superfície e um processo de *gate* enterrada com planarização, utilizando *ion milling* antes da transferência do grafeno. Estas metodologias foram adaptadas às condições da sala limpa do Laboratório Ibérico Internacional de Nanotecnologia (INL), para aumentar a repetibilidade dos processos, uma vez que são baseados em processos padrão. Adicionalmente, os processos de síntese e transferência do grafeno foram estudados.

Nesta tese, fabricaram-se transístores com frequências de corte e frequências máximas de oscilação de 80 GHz e 14 GHz, respetivamente. Estes dispositivos foram modelados através de um modelo semi-empírico. Embora não tenha sido fabricado um oscilador de anel de RF baseado em grafeno totalmente funcional, as simulações realizadas com base no modelo permitiram estudar e otimizar os parâmetros necessários para o desenvolvimento de dispositivos funcionais no futuro, demonstrando a efetividade do processo de fabrico para a sua utilização em biossensores de grafeno. Assim, esta tese estabelece um processo de fabrico repetível e adaptável a outros dispositivos baseados em grafeno, lançando as bases para a integração deste material em sensores biomédicos e tecnologias de radiofrequência.

Palavras-chave: grafeno, osciladores em anel de grafeno, radiofrequência, transístores de radiofrequência de grafeno

Abstract

Graphene, a single-atom-thick carbon material arranged in a honeycomb lattice, has gained significant attention due to its exceptional electronic, thermal, and mechanical properties. With high carrier mobility, superior thermal conductivity, and remarkable electronic characteristics, graphene has immense potential for electronic and radiofrequency (RF) applications. However, integrating graphene into practical devices presents substantial challenges, particularly in adapting conventional Complementary Metal-Oxide-Semiconductor (CMOS) fabrication processes to accommodate its unique properties. This thesis addresses these challenges by advancing the design, fabrication, and characterization of graphene-based RF transistors and oscillators, with a focus on biomedical applications. Strategies to enhance the performance of the fabricated RF graphene transistors included implementing buried gates to reduce gate resistance, minimizing access resistance using an adapted damascene process, using high-resistivity silicon substrates with SiO₂ layers to mitigate parasitic effects, and integrating thin high-k oxide (alumina) layers grown via atomic layer deposition (ALD) for improved gate control.

Two distinct fabrication methodologies were developed: a bottom-gate process without surface planarization and a planarized buried bottom-gate process using ion milling prior graphene transfer. These methodologies were adapted to the cleanroom conditions of the Iberian International Nanotechnology Laboratory (INL) to enhance process repeatability, as they are based on standard processes. Additionally, the graphene synthesis and transfer processes were optimized, prioritizing continuous graphene films over large flakes to ensure scalability and uniform device performance.

In this work intrinsic cutoff frequencies of up to 80 GHz and maximum oscillation frequencies of 14 GHz using planar buried gate devices with a 5 nm oxide layer were achieved. These fabricated devices were modelled by a semi-empirical model. Although a fully operational graphene-based RF ring oscillator was not fabricated, simulations supported that further optimization of parameters could lead to designs that sustain oscillation in the future, demonstrating the effectiveness of the fabrication process for its application in graphene biosensors. In short, this thesis provides a repeatable fabrication process adaptable to other graphene-based devices, laying the basis for integrating graphene into advanced biomedical sensors and RF technologies.

Keywords: graphene, graphene ring oscillators, RF graphene transistors, radiofrequency

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LIST OF ABBREVIATIONS AND ACRONYMS

ALD	Atomic Layer Deposition
CMP	Chemical Mechanical Planarization
CMOS	Complementary Metal-Oxide-Semiconductor
CPD	Critical Point Dryer
DC	Direct Current
EBM	Electron Beam Evaporation
ECG	Electrocardiogram
EOT	Equivalent Oxide Thickness
E-Beam	Electron Beam
FIB	Focused Ion Beam
FOM	Figures of Merit
GFETs	Graphene Field Effect Transistors
HR	High Resistivity
ICP	Inductively Coupled Plasma
INL	International Iberian Nanotechnology Laboratory
IoT	Internet of Things
OM	Optical Microscopy
PECVD	Plasma Enhanced Chemical Vapor Deposition
PWMs	Pulse-Width Modulation
RF	Radiofrequency
RIE	Reactive Ion Etching
SEM	Scanning Electron Microscopy
VCOs	Voltage Controlled Oscillators
VNA	Vector Network Analyzer
RO	Ring Oscillator
DWL	Direct-Writing Lithography

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1 INTRODUCTION

Graphene is a 2D material with a one-atom-thick layer of carbon in a honeycomb lattice. Its discovery has caused an increase in the number of studies where its synthesis, physical properties, and electrical properties were analysed. The advances in those areas allowed for the exploitation of graphene's properties for its integration and improvement of electrical circuits [1]. Moreover, the development of large-scale synthesis methods such as Chemical Vapour Deposition (CVD) has allowed for an increase in the number of research findings and has made commercial applications possible. Graphene's exceptional electrical and mechanical properties make it particularly suitable for biomedical applications. It also exhibits excellent adsorption capabilities, enabling the development of biosensors that quantify adsorbed molecules by detecting changes in graphene's properties [2]. Given graphene's exceptional mechanical properties, it is possible to fabricate flexible sensors, as will be discussed later. Despite these advantages, integrating graphene-based devices with CMOS (Complementary Metal-Oxide-Semiconductor) technology remains challenging due to its distinctive material properties. Many conventional CMOS fabrication processes cannot be directly applied to graphene, complicating efforts to incorporate features such as RF communication or analyte quantification through frequency changes in devices.

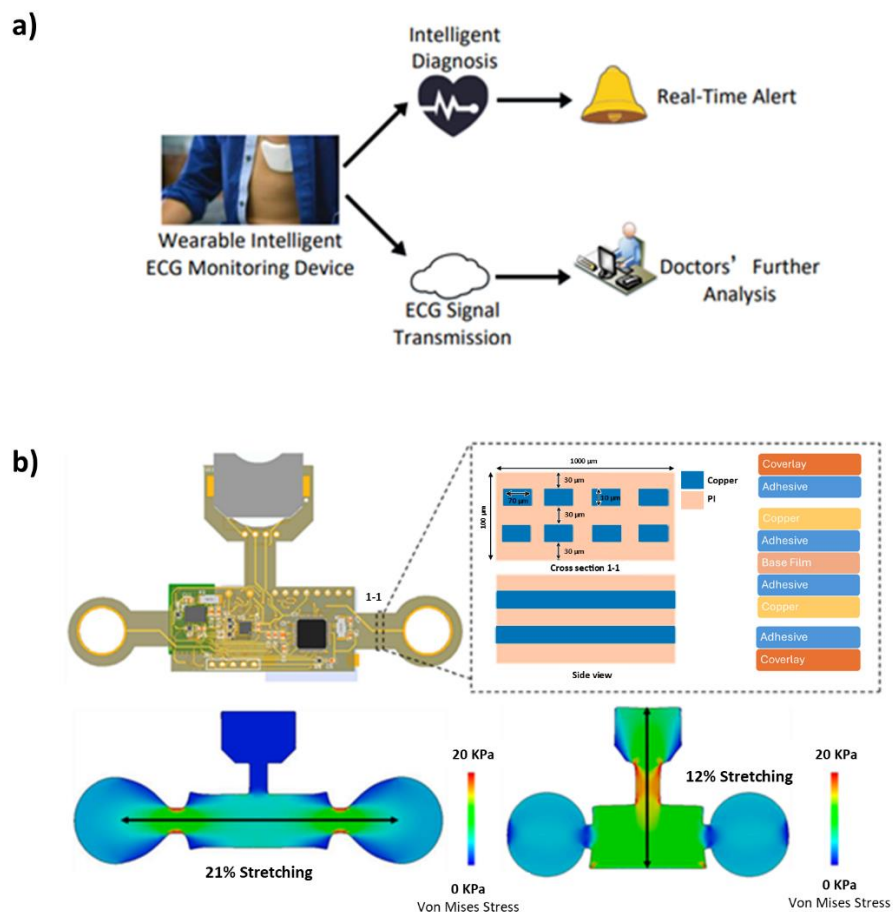
Given the previous considerations, this thesis focuses on developing a graphene-based oscillator for biomedical applications. This could range from a ring oscillator (RO), a resonant oscillator or a MEMS structure. The proposed design should be fully compatible with the International Iberian Nanotechnology Laboratory (INL) cleanroom, aligning with the standardized processes employed in most research laboratories worldwide.

1.1 Biomedical devices

The investigation and application of biomedical devices have indeed witnessed tremendous growth over the past years, particularly with the advent of various technologies aimed at enhancing patient care and monitoring. Wearable devices, flexible electronics, on-body systems, and miniature devices, along with remote charging, wireless power transfer systems, have emerged as pivotal innovations in this field. Wearable devices have gained significant traction due to their ability to monitor various physiological indicators continuously and non-invasively, allowing users to track their health without disrupting their

daily activities. For instance, Wang et al [3] developed a wearable device capable of simultaneously monitoring electrocardiogram (ECG) signals and counting physical activities in cardiovascular patients. This device has proven effectiveness in clinical practice, facilitating early detection of arrhythmias and enabling timely interventions to mitigate complications associated with severe cardiovascular diseases [3]. This device as well as the example of application can be seen in Figure 1 a). Similarly, Susana et al [4] introduced a non-invasive device that uses photoplethysmography sensors to monitor blood glucose levels, significantly improving the quality of life for diabetic patients by eliminating the need for frequent finger pricking. The continuous monitoring capabilities of these devices underscore their importance in modern healthcare, particularly for chronic disease management [4]. The evolution of flexible biomedical devices has further enhanced the comfort and sustainability of wearable technologies. Recent advancements in materials science have led to the development of flexible electronics using biocompatible polymers and conductive materials such as doped graphene. As reported in [5] the graphene could be used as a stretchable material to detect temperature, pressure, and metabolites in sweat, demonstrating its potential of this material for personalized health monitoring. In [6], the authors reported the development of a wireless and flexible biosensor patch designed for continuous, longitudinal monitoring of multiple physiological signals, including body temperature, blood pressure, and electrocardiography. The patch was engineered to be highly compatible with the skin, featuring optimized flexibility and mechanical stretchability to ensure durable and comfortable attachment, even on curved surfaces as can be seen in Figure 1b). The flexibility of these devices is crucial for ensuring accurate skin contact and comfort during use, which is essential for effective health monitoring. On-body devices have revolutionized continuous, non-invasive patient monitoring by integrating seamlessly with the human body. The trend towards miniaturization has enabled the development of smaller, lighter, and more comfortable devices that maintain high accuracy in monitoring functions. For instance, the pacemaker, an implantable medical device, has been miniaturized to less than the size of a coin, allowing for direct implantation into heart tissue [7], as can be seen in Figure 1 c). Hassan et al [8] further exemplified this trend with an implantable glucose sensor (LC tank resonator) that provides continuous monitoring for diabetic patients, transmitting data wirelessly [8]. This miniaturization not only enhances patient comfort but also increases adherence to treatment regimens. One of the significant challenges in the realm of implantable devices is the need for battery replacements, which can need invasive procedures. Innovations in wireless power transfer technologies have addressed this issue. Laughner et al [9] reported a wireless implantable pacemaker in mice which could pave the way for eliminating the need for surgical battery replacements and allowing for continuous monitoring from within the body [9]. Additionally, Heo et al [10] developed a wireless deep

brain stimulation device for Parkinson's disease rodents, powered through inductive coupling, which reduces the need for surgical revisions and enhances patient comfort [10]. The device could be seen in Figure 1 d). These advancements highlight the transformative potential of wireless technologies in improving the functionality and usability of biomedical devices. Given that, the recent advancements in biomedical devices, particularly in the areas of wearables, flexibility, miniaturization, and wireless power, signify a remarkable evolution in healthcare technology. These innovations are not only enhancing the accuracy and personalization of health monitoring solutions but are also paving the way for proactive healthcare management. Ongoing research into new materials, miniaturization techniques, and wireless power technologies promises to further revolutionize the field, ultimately leading to improved patient outcomes and a more integrated approach to health management.



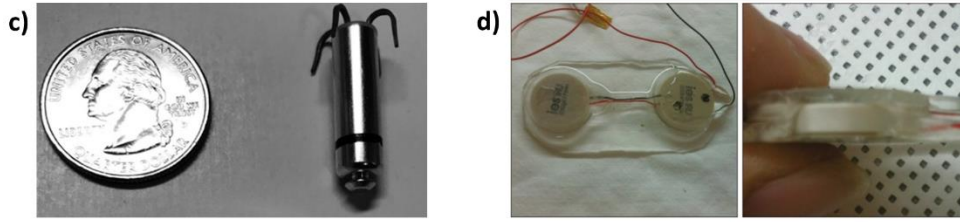


Figure 1 – Examples of biomedical devices a) Wearable intelligent ECG monitoring system. Adapted from [3]. b) Design and mechanical properties of flexible biosensor patch. Adapted from [6] c) pacemaker device. Adapted from [7] d) wireless deep brain stimulation device for Parkinson's disease rodents. Adapted from [10].

1.2 Oscillators and graphene technology

The integration of graphene into sensor technology has transformed research across various fields, including healthcare, environmental monitoring, and smart materials. Graphene has become a very attractive material due to its properties. It is a single sheet of sp^2 -bonded carbon, zero-gap semiconductor with a high conductivity. When compared to copper with the same thickness (though achieving such thinness with copper may not be feasible), it has got a lower resistance and can sustain a higher current density than any other known material [1]. For electronic applications, its key property is its high carrier mobility, with suspended graphene reaching mobilities up to $200000 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ [11], while silicon has got an electron mobility of $1400 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ [12]. This property makes the graphene a suitable material for radiofrequency (RF) applications [13]. The reported devices range from transistors with measured intrinsic cut-off frequencies (f_t) of up to 300 GHz, and with applications on low-loss interconnects and passives [14][15]. These unique electrical properties, along with mechanical strength, and flexibility, make it an ideal candidate for sensor applications [16], including pressure sensing, strain detection, and physiological signal monitoring. For instance, *Yang et al.* [17] demonstrated a wearable graphene strain sensor capable of precise pulse wave monitoring [17]. Similarly, *Xie et al.* [18] reported on the detection of physiological signals using graphene, emphasizing its potential in health monitoring systems [18]. However, while graphene-based sensors rely on the graphene as the sensing material, they often rely on CMOS chips for RF communication for data transmission as can be seen in the device reported in [19]. This need reveals a significant gap in current technology, emphasizing the importance of developing RF graphene devices, particularly RF graphene oscillators, for sensing or communication. Achieving a fully graphene-based sensor requires a unified and compatible fabrication process. Relying on CMOS integration with graphene, which is being done by the research community [20], can increase device complexity and costs, and it may even degrade performance since the standard RF components used in CMOS might not be optimized for graphene's unique characteristics. By using the resonant

properties of graphene, these oscillators could provide a compact and efficient means of generating RF signals tailored to the specific needs of graphene sensors. In [21] the resonant behaviour of graphene membranes was explored. The ability to tune the frequency response of graphene devices could enhance the performance of graphene sensors [22]. For instance, combining graphene sensors with oscillators could facilitate real-time monitoring of physiological signals, providing immediate feedback for health applications, exploring the benefits of using graphene as the interconnects [23] or being the oscillator the sensor itself. This integration could also enhance the capabilities of environmental sensors, allowing for more accurate and timely data collection in various settings [24]. In addition to improving performance, graphene oscillators could also contribute to miniaturization efforts in sensor technology. Graphene's compact size and exceptional electrical properties make it an ideal choice for miniaturized devices. This miniaturization could be particularly beneficial in wearable technology, where space and weight are critical factors. The necessity of developing graphene oscillators is further underscored by the growing demand for advanced sensor systems in various industries. As the Internet of Things (IoT) continues to expand, the need for efficient and reliable communication between sensors and data processing units becomes increasingly important. Given that, while graphene sensors have demonstrated remarkable capabilities for sensing, due to the facility to be functionalized and its mechanical flexibility, which enables new applications, the integration of RF communication systems presents challenges that can hinder their performance and usability. The development of dedicated graphene oscillators could address these challenges, streamlining communication processes and enhancing the overall functionality of graphene-based sensors. By leveraging the unique properties of graphene, researchers can create more efficient, compact, and sensitive sensing systems that meet the demands of modern applications.

1.3 Objectives

The development of new implantable solutions to support healthcare provision depends on the ability to integrate and miniaturize new implants, which should be cheaper, more effective, and more ubiquitous. Graphene-based sensors offer this possibility, but there are still some challenges to overcome in graphene RF systems. An unresolved challenge lies in implementing graphene oscillators integrated with graphene biosensors to facilitate RF communication or enable wireless analyte quantification. This is achieved by detecting changes in the device's frequency caused by the binding of analytes.

Given the previous, this PhD thesis aims to mitigate the issues associated with existing techniques and explore new strategies for achieving radio frequency oscillators in graphene. First, the strategy

involves selecting the solution with the highest potential to produce RF oscillators with the necessary characteristics for modulating and transmitting a signal wirelessly. This oscillator will then be fabricated and characterized. The fabrication process should be fully compatible with INL's cleanroom.

In summary, these work aims to:

- Select available solutions and techniques to fabricate the RF graphene oscillator.
- Adapt these techniques to the INL cleanroom (that are based on standard large scale fabrication processes) to establish a repeatable and reliable fabrication process for integrating graphene, aimed at incorporation into graphene biosensors.
- Design, implement, characterize, and model the RF components to fabricate the RF oscillator.

1.4 Contributions

The contributions of this thesis tackle the challenges of designing graphene-based RF oscillators. Since the ring oscillator was chosen to meet the specified requirements (graphene oscillator), several key contributions were made in this area:

- The establishment of a repeatable process for RF graphene devices fabrication, enabling semi-industrial production, paving the way for integration with graphene biosensors
- The design and fabrication of RF graphene transistors, inverters, and ring oscillators, as illustrated in Figure 2.

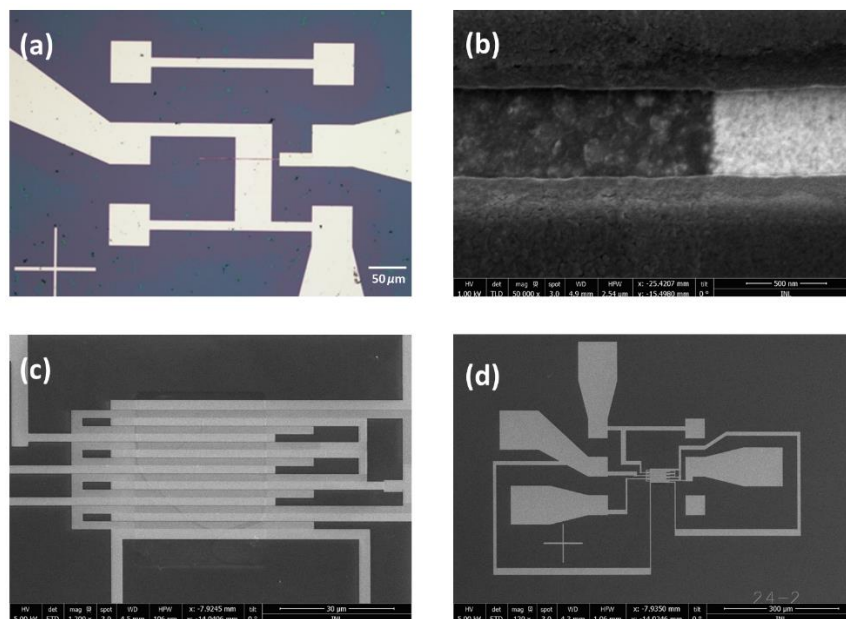


Figure 2 – Examples of devices fabricated under the scope of this thesis. a) Optical microscope of an RF graphene transistor. b) SEM image of the channel of the RF graphene transistor. c) and d) SEM image of a ring oscillator.

-The characterization of the RF graphene transistors (fabricated using large scale methods) achieving intrinsic f_T of 80 GHz and intrinsic f_{max} of 14 GHz.

-The development and implementation of a semi-empirical model, along with the modelling of the fabricated transistors.

-The application of the developed model to optimize the performance of the RF ring oscillator.

Through this work, various oral presentations were originated, as well as the following publications:

1-Diogo Baptista, Ivo Colmiais, Vitor Silva, Pedro Alpuim, P. M. Mendes, "2D Electronic circuits for sensing applications", "Graphene Field-Effect Transistors: Advanced Bioelectronic Devices for Sensing Applications, Omar Azzaroni, Wolfgang Knoll John Wiley & Sons, Limited, Dec 27, 2023" https://books.google.pt/books/about/Graphene_Field_Effect_Transistors.html?id=MchqzgEACAAJ&redir_esc=y

2-Fernandes J, Grzonka J, Araújo G, Schulman A, Silva Vitor, Rodrigues J, Santos J, Bondarchuk O, Ferreira P, Alpuim P, Capasso A. Bipolar Resistive Switching in 2D MoSe₂ Grown by Atmospheric Pressure Chemical Vapor Deposition. ACS Appl Mater Interfaces. 2024 Jan 10;16(1):1767-1778. doi: 10.1021/acsami.3c14215. Epub 2023 Dec 19. PMID: 38113456.

3-Colmiais, Ivo; Silva, Vitor; Borme, Jérôme; Alpuim, Pedro; Mendes, P.M. "Extraction of Graphene's RF Impedance through Thru-Reflect-Line Calibration". Micromachines 14 1 (2023): 215. <http://dx.doi.org/10.3390/mi14010215> .

4- Colmiais, Ivo; Silva, Vitor; Borme, Jérôme; Alpuim, Pedro; Mendes, Paulo M.. "Towards RF graphene devices: A review". FlatChem 35 (2022): 100409. <http://dx.doi.org/10.1016/j.flatc.2022.100409> .

5-Jmai, B.; Silva, Vitor; Mendes, P.M. 2D Electronics Based on Graphene Field Effect Transistors: Tutorial for Modelling and Simulation. *Micromachines* **2021**, *12*, 979. <https://doi.org/10.3390/mi12080979>

6- Silva, Vitor. "Oxygen assisted monocrystalline graphene growth by chemical vapor deposition". Paper presented in NanoPT2020, 2020.

7-V. Silva, I. Colmiais, L. Baptista, J. Borme, P. M. Mendes, P. Alpuim, "Towards graphene based RF devices", JORNADAS CF-UM-UP 2019, Centro de Física das Universidades do Minho e do Porto, Portugal, December 13th 2019.

8- Silva, Vitor; Mendes, P.M.; Alpuim P; Borme, Jérôme. "Graphene Radio-Frequency Transistors with Self-Aligned Channel and Core-Shell Nanowire Gate". Paper in 5th Edition of the European Graphene Forum - EGF 2019, Lisbon, 2019.

1.5 Thesis outline

The first chapter introduces graphene, highlighting its unique characteristics, significance, and applications in electronics. It then establishes the context for the importance of graphene oscillators, particularly their potential in biomedical applications.

The second chapter reviews the oscillators available in the literature, discussing their performance and designs, with a particular emphasis on ring oscillators. Additionally, it provides a literature review on the current state of graphene transistors.

Chapter three outlines the design approaches to meet the required specifications of RF graphene transistors for ring oscillators. The fabrication processes for the devices developed in this thesis are detailed, presenting two approaches: a bottom-gate graphene device fabrication process without surface planarization, and another with a buried gate using ion milling to planarize the surface. Additionally, the chapter discusses the growth of the graphene used in this work and the challenges encountered during its fabrication.

Chapter four focuses on the development of the oscillator. It presents the equations used to model the fabricated devices, along with the RF and DC measurements of these devices, which are analysed and discussed. The transistor models are extracted based on these measurements. Additionally, the chapter covers the oscillator design process, and the optimization of inverters intended for use in the ring oscillator.

Finally, Chapter five presents the conclusions of this work, summarizing the key findings and their implications. It also highlights potential directions for future research and development in this field.

2 GRAPHENE OSCILLATORS

In the previous section, it was demonstrated that the development of graphene oscillators to be integrated into biomedical devices could impact the graphene sensors, with a fully compatible process, enabling new applications for them. Given that, in the following section, the current state of graphene oscillators will be explored with the focus on the ring oscillators due to its reduced size, when compared with other kind of oscillators. Given that, this type was selected as the approach to implement in this thesis.

2.1 Ring oscillators

A ring oscillator is a circuit that is comprised of an odd number of cascaded logic inverters in loop. This loop makes the ring oscillator unstable, inducing oscillation at high frequencies [25]. As described earlier, the absence of a bandgap, which makes it impossible to turn off the graphene transistor is a disadvantage in low-power digital applications. However, it does not hinder the use of this material for RF applications.

For a ring oscillator to operate, it is mandatory that the voltage gain ($A_v = g_m / g_d$, where g_m is the transconductance and g_d is the output conductance) is higher than the unit to match the inputs and outputs of the inverters. It is important to note that the oscillation of the stages of the ring oscillators is strongly dependent not only on the cutoff frequency (f_c) and maximum oscillation frequency (f_{max}) of the transistor (which would be addressed later) but on many other factors such as the loading caused by the following stage, mismatch between different stages, interconnects, and gate resistances. The used FOM (Figure of Merit) for the graphene ring oscillators is the oscillation frequency (f_o), since the $f_o < f_r$, ring oscillators are the standard test benches for evaluating the ultimate technology performance limits. The general schematic of a ring oscillator can be seen in Figure 3 a).

In [25], the first-ever graphene ring oscillators were presented. The graphene ROs were fabricated through a multi-transistor approach, using high carrier mobility graphene (CVD grown monolayer), and achieved f_r of 1.28 GHz. The complementary operation of the graphene inverters was obtained between the Dirac points of the two GFETs (graphene field effect transistors), after a positive voltage was applied [26]. A back-gate voltage was used to shift the Dirac point to guarantee the maximum voltage swing of the inverters. Still in the same work, 3 types of ring oscillators were fabricated: large ($L = 3 \mu\text{m}$ and $W = 20 \mu\text{m}$), medium ($L = 2 \mu\text{m}$ and $W = 10 \mu\text{m}$) and small ($L = 1 \mu\text{m}$ and $W = 10 \mu\text{m}$). Furthermore, three-

stage ring oscillators were fabricated. The biggest voltage swing achieved in those inverters was 0.57 V. After the three inverters stage, one buffer was added to provide gain to the circuit and to isolate the ring oscillator from the external connected loads. It should be noted that this buffer stage degrades the performance of the ring oscillator since it has a significant input capacitance, compared to those of the ring oscillators stage. The achieved oscillation frequency of the fabricated ring oscillators was $284 \text{ MHz} < f_o < 350 \text{ MHz}$ for the large, $504 \text{ MHz} < f_o < 750 \text{ MHz}$ for the medium ones, and $1 \text{ GHz} < f_o < 1.28 \text{ GHz}$ for the small ones. It is important to note that the parasitic capacitances play an important role in the small L/W relationship inverters. The delay caused by an $L = 1 \text{ }\mu\text{m}$ transistor is about 100 ps which is like that caused by Si CMOS inverters at the same gate length, which is a good indicator for the graphene ring oscillators. The fabricated devices and the output signals of the buffered graphene ROs are shown in Figure 3 and Figure 4, respectively.

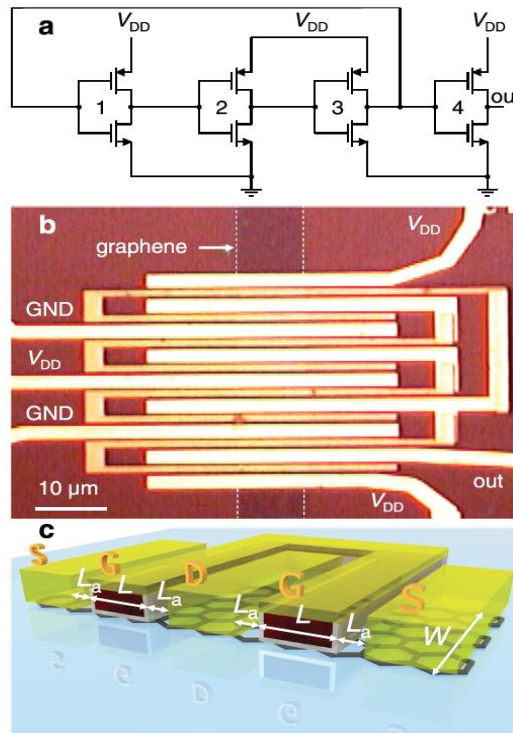


Figure 3 – Integrated monolayer graphene ring oscillator. a) Circuit diagram of the ring oscillator. b) Optical microscope of a ring oscillator fabricated in [25]. c) Cross section schematic of a graphene inverter composed of two FETs.

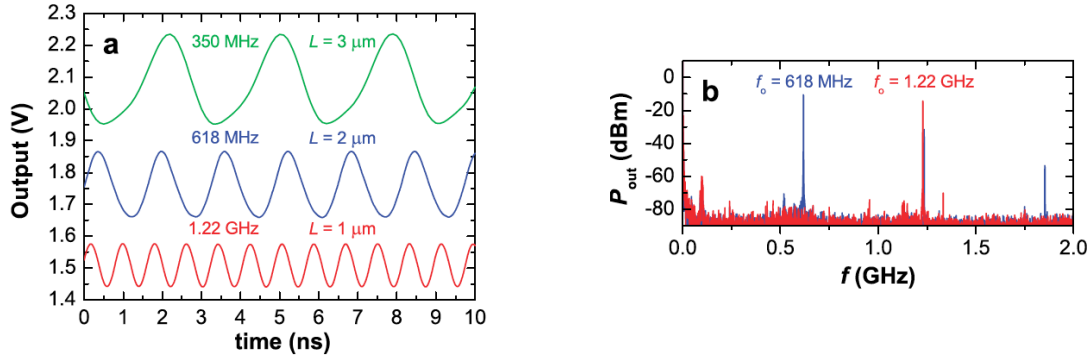


Figure 4 – a) Output signals of buffered graphene ROs reported in [25], at $V_{\text{DD}} = 3.5\text{V}$ b) Power spectrum of the medium and small ROs.

In [27], another similar ring oscillator was presented. In that work, nine different ring oscillators were made, with nine different gate lengths, from $0.5 \mu\text{m}$ to $3.3 \mu\text{m}$ while varying the channel width, access length, and source and drain contact thickness at the same time. The shortest achieved gate delay was 31 ps, at a gate length of $0.9 \mu\text{m}$. This value is smaller than the CMOS transistors with the same gate length. This delay allowed the authors to fabricate the fastest graphene ring oscillator reported to date, running at 4.3 GHz. It was possible to obtain this value since a high voltage gain ($A_v \gg 5$) was achieved. For that work, graphene monolayers were grown by CVD on copper foil. A 4 nm thick film of aluminium was evaporated on top of graphene to be oxidized, to form the gate dielectric. The ring oscillators, which require low or zero back-gate voltage, were operated at room temperature while the ones that require large back gate voltages ($V_{\text{BG}} > 50 \text{ V}$) were operated on air under an N_2 flow (to stabilize the position of the Dirac point at 0).

In that work, the ROs made with inverters with $L < 0.8 \mu\text{m}$ do not oscillate. The authors found that the gain of the stages decreased from 5 to approximately 2. This occurred due to the contact and access resistance, which do not scale with the gate length. At short gate lengths, these resistances become comparable to the channel resistance and therefore suppress the voltage gain. The fabricated devices can be seen in Figure 5.

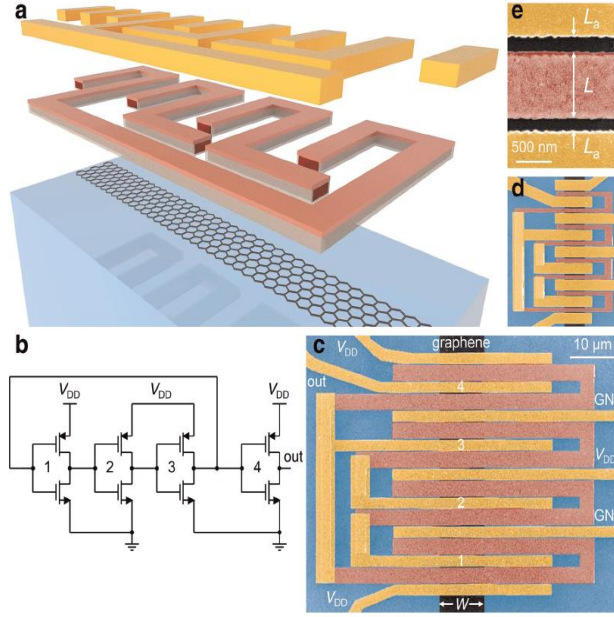


Figure 5 - Fabricated ring oscillators (ROs) in [27]. a) 3D view of a buffered three-stage graphene RO. b) Circuit diagram of the three-stage ring oscillator. c) and d) SEM image of the fabricated RO. e) SEM image of an GFET in a RO [27].

Another work that presents a graphene ring oscillator is reported in [28]. In that publication, the authors not only made a fully graphene ring oscillator but also tried to incorporate some CMOS circuits to prove the compatibility of the two technologies. They proposed a novel class of graphene-Si CMOS circuits that exploit the ambipolarity of graphene, to simplify the circuit and provide additional functionality to them. The authors implemented a ring oscillator fabricated only with graphene, a Si CMOS D latch, and a timing RC circuit. The objective of the D latch is to provide switching and large voltage swing to control the GFET, while the RC circuit is used to set the oscillation frequency. The maximum obtained oscillation frequency was 4.2 MHz. The authors claimed that the ambipolarity of the graphene allows for the accomplishment of pulse-width modulators (PWMs) and voltage-controlled oscillators (VCOs) from the same circuits, i.e., without any circuit modification. The top gated GFETs were made with CVD grown graphene transferred to a SiO_2/Si substrate on which h-BN was previously exfoliated. The h-BN was used since the authors believe that the GFETs fabricated on top of this substrate are more stable (with the same electrical properties over time), than the ones fabricated directly on top of the SiO_2 substrates. A 4 nm thick gate dielectric made of Al_2O_3 was obtained after oxidizing an evaporated Al film directly on top of graphene. To perform the study reported earlier, this device was connected to the silicon circuits that are assembled on a breadboard or in printed circuit boards. These circuits will not be addressed in this report, since only the layout of the ring oscillator and its performance are important for this work. The implemented graphene RO can be seen in Figure 6.

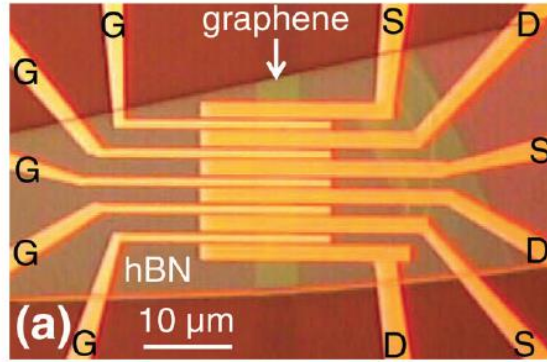


Figure 6 – Graphene oscillator fabricated on top of an h-BN flake, with five GFETs reported in [28].

In [29] a graphene ring oscillator based on high performance inverters were reported. The oscillation frequency of such devices was in the range of dozens of MHz, demonstrating an effective method for fabricating RF graphene transistors. However, this approach may not be suitable for certain applications due to the low oscillation frequency. The optical micrograph of the ring oscillator can be seen in Figure 7.

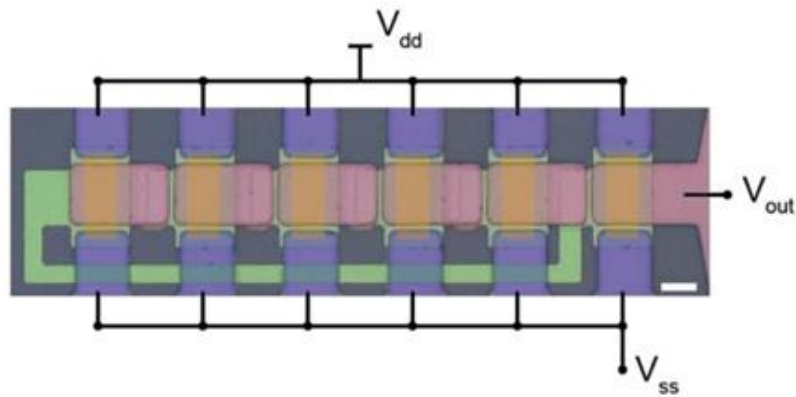


Figure 7 – Optical micrograph of a ring oscillator with false color annotations highlighting the various circuit elements. The scale bar represents 10 μm. Source and drain contacts are shown in blue, the local back gate.

2.2 Resonant oscillators and MEMs oscillators

Ring oscillators are not the only kind of oscillators where graphene could be important. Graphene is also important in some MEMS (Microelectromechanical Systems) structures or LC tanks. In [30], a tantalum disulfide-boron nitride-graphene device was developed. In that oscillator, the boron nitride was used to protect the device against oxidization, maintaining the phase of the generated wave. A GFET was fabricated to control the oscillation frequency of the oscillator, which in this case is a voltage-controlled

oscillator (VCO). The oscillation frequency of the device could be adjusted by changing the gate voltage of the device. The illustration and the SEM image of the fabricated device can be seen in Figure 8.

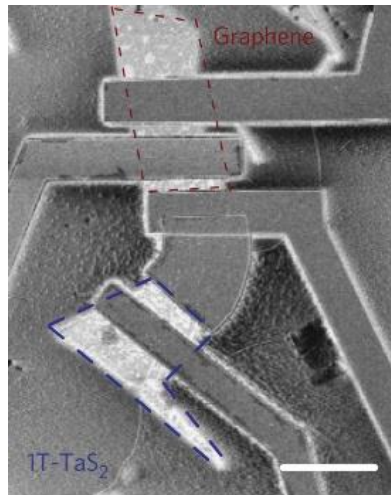


Figure 8 – SEM image of the VCO fabricated with graphene and 1T-TaS₂, highlighted in the figure, and reported in [31].

In [32] another GFET based oscillator was presented. This device is based on a resonator nanoplate of aluminium nitride. A graphene membrane was placed on top of this structure obtaining an oscillation frequency of 245 MHz. The working principle of this device is similar to the reported before. The illustration and the SEM image of the fabricated device are shown in Figure 9.

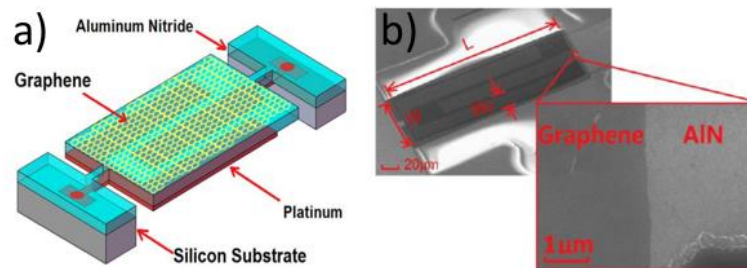


Figure 9 – Aluminium nitride nanoplate resonator with graphene: a) schematic illustration of the structure of the proposed device, and b) SEM image of the device reported in [32].

It is important to note that RF transistors can also be used in LC tanks to compensate for losses during oscillations. In this context, academia has been focusing on this material, as demonstrated in [33], where the authors proposed the first algorithm for analysing such circuits. This development could pave the way for the integration of this technology into LC tanks and sensors. In Figure 10 it is possible to observe the schematic of the proposed GFET based LC-VCO.

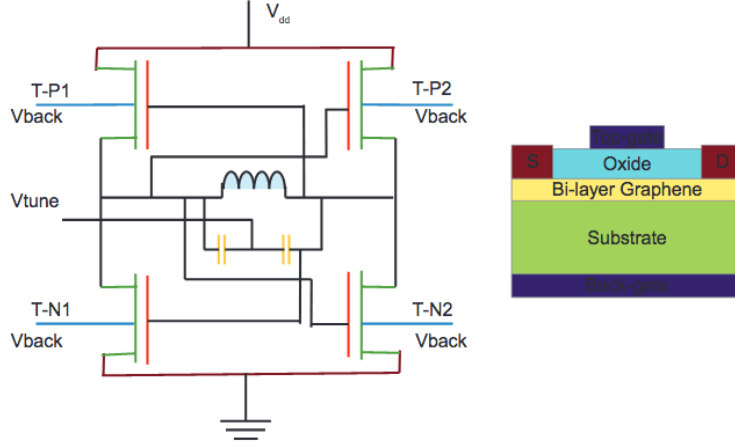


Figure 10 – Schematic of the proposed GFET based LC-VCO on the left, and cross-section of the GFETs on the right [33].

2.3 Other types of oscillators

Transistor-based oscillators are not the only type of oscillators that can be fabricated. Graphene MEMS-oscillators have been also reported.

Similarly to transistors, to evaluate the performance of MEMS oscillators, it is necessary to establish the FOMs. The most used FOM for MEMS oscillators structures are the quality factor (Q) and the resonance frequency (f_r) [34]. The quality factor is the ratio between the stored energy in one device and the dissipated energy per resonance cycle, and is given by Q :

$$Q = \frac{f_r}{f_u - f_o} \quad (1)$$

where f_r is the resonant frequency, f_u is the upper oscillation frequency and f_o is the lower oscillation frequency, being $f_u - f_o$, also known as Δf .

The resonant frequency of an oscillating device generally refers to a particular frequency where the stored kinetic energy and the potential energy are in resonance. Graphene is a suitable material for resonator structures due to its high young modulus and its atomic thickness. These properties enable graphene to achieve resonant natural frequencies of hundreds of MHz and to tolerate high strains without damage. The graphene membrane could be actuated thermally, mechanically or electrically to achieve high oscillation frequencies. In the next few pages, several MEMS devices will be presented. In [35], the authors used graphene foils obtained by mechanical exfoliation and placed them directly on top of trenches previously opened on SiO_2 with gold contacts. A general illustration of the fabricated device can be seen Figure 11.

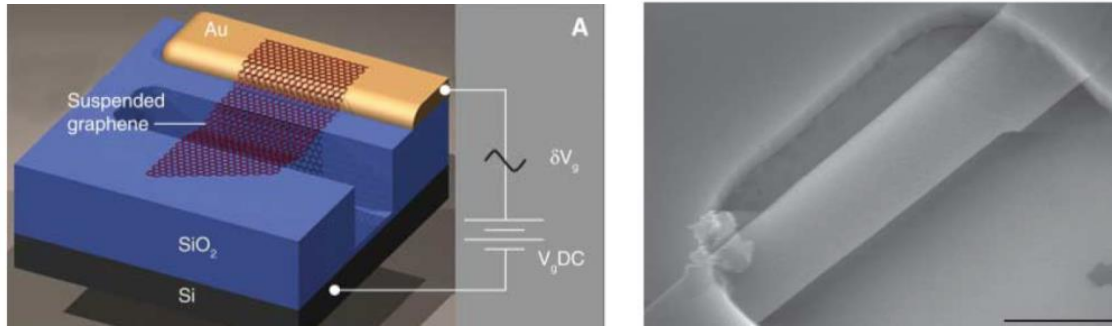


Figure 11 – On the left is represented the schematic of the oscillator, and on the right the SEM image of the device, as reported in [35].

These membranes were actuated in 2 forms: electrically and optically. The oscillation frequency of the oscillators varied from 1 MHz to 170 MHz, and the Q changed from 20 to 850. A SEM image of this device is shown Figure 11 on the right.

In [36] an on-chip heater for tuning of graphene nanodrums is presented. This heater adjusts the nanodrums properties through the Joules effect. Using a ring structure submitted to thermal expansion, the authors demonstrated that the applied nanodrums voltage control tunes the oscillation frequency. The oscillation frequency of the device is 11.5 MHz. The SEM image of the device and the general operation schematic of the device can be seen in Figure 12.

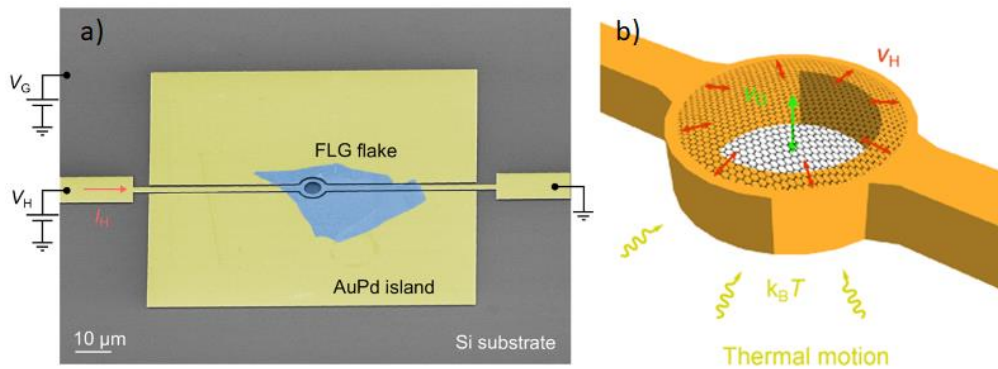


Figure 12 – SEM image of the reported oscillator nanodrums on the left, and schematic diagram of the device on the right [36].

Other non-conventional options to obtain oscillators could consist in using spin-torque nano-oscillators. This kind of oscillators are typically more complex, but the great advantage of these structures is the absence of current flowing through the device's active area. In [37], the authors proposed a method to make spin-orbit torque nano-oscillator based on a single permalloy layer with the thickness in the 15-20 nm range, grown on an alumina substrate and capped with silicon dioxide. With this method, the nano-

oscillators could achieve frequencies of several GHz. The fabricated device is presented below, in Figure 13.

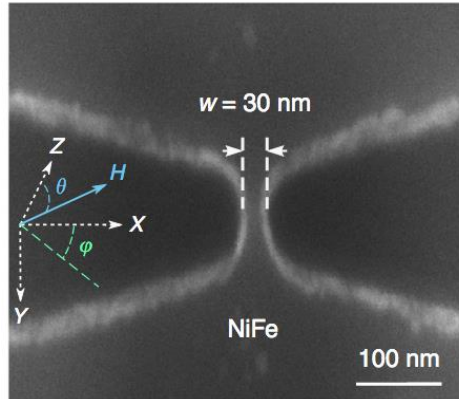


Figure 13 – SEM image of a permalloy nano-constriction, width of 30 nm [37].

In [38], a 3-terminal spin torque nano-oscillator is presented (STNO), which is based on a magnetic tunnel junction excited by a spin injection mechanism. The combination of the two mechanisms outperforms the use of only one to excite the free layer into dynamic regimes. As a result, high output powers are achieved. The fabricated device is shown in Figure 14.

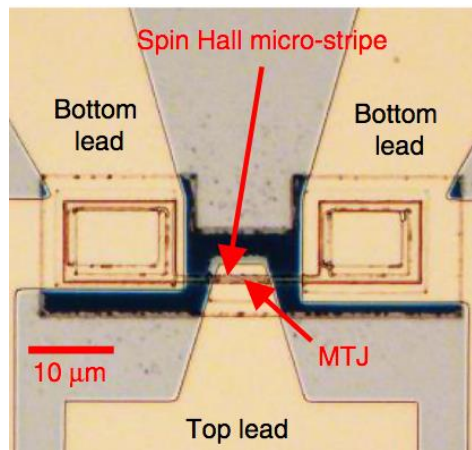


Figure 14 – Optical microscope of the spin-torque nano-oscillator device, showing the MTJ and the spin Hall micro-stripe fabricated in [38].

In [39], a device that combines local injection of a pure spin current with enhanced spin-wave radiation losses is presented. The authors demonstrated coherent auto-oscillations excited by a pure spin current in magnetic nanodevices. Their findings paved the way for the implementation of magnetic nano-oscillators based on conducting or insulating materials, without the use of current flowing through the active area of the device. In Figure 15 it is possible to see the device under test in [39].

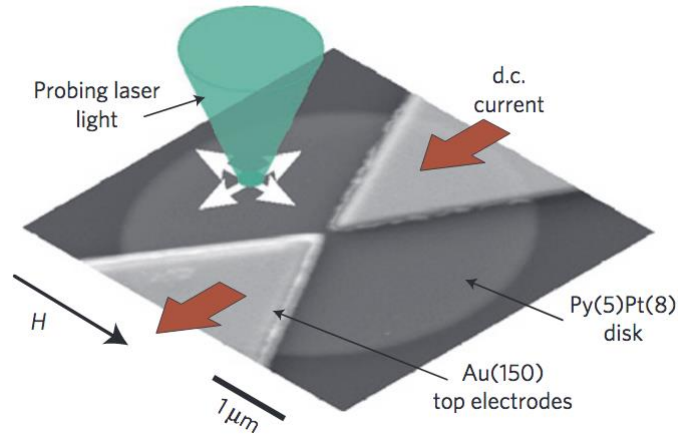


Figure 15 – SEM image of the device showing its structure and composition, and the measurement scheme, applying a DC current between both contacts, and probing it with a laser light [39].

A skyrmion-based spin-torque nano-oscillator is presented in [40]. The system involves a circular nanopillar with an ultrathin film free magnetic layer with strong Dzyaloshinskii-Moriya interaction and a polarizer layer with a vortex-like spin configuration. The authors showed the appearance of a skyrmion gyration which leads to oscillations of the material. The general schema of the proposed device can be seen in Figure 16.

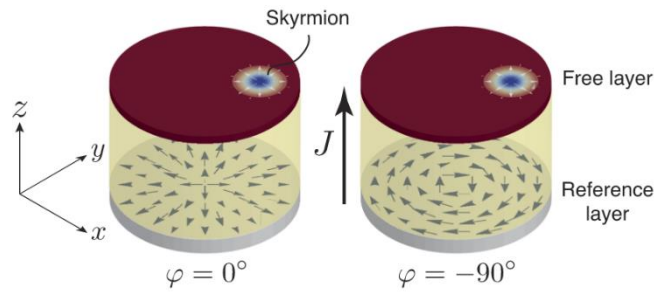


Figure 16 – Skyrmion-based spin-torque nano-oscillator, designed with a nanopillar, with the skyrmion in the free layer, and two different possibilities for the distribution of the magnetic field in the reference layer [40].

2.4 RF Graphene transistors

As stated below; to fabricate graphene ring oscillators, it is necessary to fabricate graphene transistors with RF capabilities, since they are the building block of these circuits. In recent years, there has been significant progress in the speed and integration of integrated circuits, primarily due to efforts in downscaling silicon transistors. However, silicon transistors are now approaching their technological limits. To guarantee that electronics technologies are evolving and to ensure that the improvement of the current devices is possible, further research on new materials to replace silicon needs to be undertaken. For this purpose, researchers are putting a big effort into the study of graphene due to its amazing electrical properties such as high saturation velocity and high carrier mobility, which are important for RF electronics. There are several RF graphene active devices reported in the existing literature. Due to graphene's ambipolar conduction, it is possible to develop non-linear electronics which can be switched from n-type to p-type by adjusting the Fermi's level through tuning the gate bias. The high carrier mobility and high current saturation velocity of graphene can enable the use of graphene in RF circuits. The difficulty to turn off these devices is a problem for logic applications due to increased power consumption [41], however, in RF applications it does not have a big effect [25]. RF graphene transistors have oscillation frequencies and cutoff frequencies in the tens of GHz range (concepts that will be further addressed later in this document), with some of the reported devices achieving intrinsic cutoff frequencies higher than 300 GHz [15]. Connecting these transistors or polarizing them in particular states enable the design of several RF circuits. One simple example of these can be the ambipolar mixer reported in [42]. More complex RF circuits can be fabricated with graphene, such as ring oscillators. These devices can work above 4 GHz [27] and can be used in biosensors or RF communications. In the field of RF communications, a graphene radiofrequency receiver was developed in [43]. Despite the low availability of graphene to provide power at high frequencies (because of its low saturation current [44]), some RF graphene amplifiers were reported in [45] and [46]. Although graphene isn't a well-established technology, it is a good candidate to develop RF devices due to its properties. Graphene has a higher electron mobility than silicon, and although CMOS has a higher f_T and f_{max} , it is achieved at twice the current consumption [47]. Nevertheless, GFETs only have a narrow I_{DS} operation window, their performance is limited by its lower g_m and parasitics, and to exceed the GFETs performance, it is predicted that a mobility higher than $3000 \text{ cm}^2\text{V}^{-1}\text{s}^{-1}$ is required [47].

The performance of RF graphene FETs is commonly evaluated by the cut-off frequency (f_T) and the maximum oscillation frequency (f_{max}). The cut-off frequency (f_T), the widest figure of merit for RF graphene

transistors, is defined as the frequency at which the magnitude of the small-signal current gain of the transistors is reduced to unity. In general, the cut-off frequency can be defined as described in equation 2 [48]:

$$f_T = \frac{g_m}{2\pi[(C_{gs} + C_{gd})(1 + (R_d + R_s)g_{ds}) + C_{gd}g_m(R_d + R_s) + C_{pg}]} \quad (2)$$

where g_m is the transconductance, C_{gs} is the gate to source capacitance, C_{gd} is the gate to drain capacitance, C_{pg} is the gate parasitic capacitance, R_s and R_d are the source and drain resistance, and g_{ds} is the output conductance (conductance between drain and source). The transconductance, g_m , is the slope of the curve I_{DS} vs V_{GS} with V_{DS} constant, as shown in section 4.1.4.

The f_{max} which refers to the frequency when the maximum available power gain becomes unitary. This refers to the ability of the transistor in providing gain, important for example in amplifiers and ring oscillators. Achieving a high f_{max} is challenging because GFETs are strongly affected by short-channel effects. This is primarily due to the gate capacitance approaching the same order of magnitude as the graphene quantum capacitance, which reduces the ability to modulate the graphene channel effectively. Additionally, the high contact resistance in graphene devices further impairs performance, leading to a loss of control over the channel. Typically, this value is one magnitude lower than the f_T GFETs [49]. The f_{max} can be obtained by:

$$f_{max} = \frac{f_T}{2\sqrt{g_{ds}(R_g + R_s) + 2\pi f_T R_g C_{gd}}} \quad (3)$$

where R_g corresponds to gate resistance, and the remaining variables are the same as in equation 2.

By analysing equation 2, to increase the f_T it is necessary to increase g_m or decrease g_{ds} and all the parasitic capacitances, by decreasing the gate oxide thickness, for example. Since the g_m is proportional to the carrier mobility and all g_m , C_{gs} , and C_{gd} are inversely proportional to the channel length, to achieve a big cut-off frequency, f_T , it is essential to have a high carrier mobility and a small channel length of the device. However, this is not so simple, since the GFETs are highly affected by the short channel effect due to the quantum capacitance of the material [50].

According to equation 3 (and the equation of the f_T formula shown in 2), to achieve a high f_{max} , it is necessary to decrease the gate capacitance ($C_{gs}+C_{gd}$), the contact resistance (included in R_s and R_d), and the parasitic capacitances (C_{pg}) of the GFETs [51].

To measure correct FOMs, a correct de-embedding needs to be performed. There are several methods to perform de-embedding. The Multiline Thru-Reflect-Line (TRL) is often regarded as the most accurate algorithm as it does not require the fabrication of high precision resistors. However, its feasibility in low GHz frequencies is limited due to the impractical long reference lines required [52]. Another widely used de-embedding algorithm is the open-short algorithm. Even though this algorithm works very well at low frequencies, it requires the lengths of the pads and signal-to-ground interconnects to be smaller than $l/20$ of the wavelength. For this reason, it should be used after both SOLT (Short-Open-Load-Thru) calibration and TRL de-embedding. Thru-only algorithms hold the same limitations as the open short [52]. Despite these limitations, the open short de-embedding procedure is the most used algorithm to extract the intrinsic parameters of the graphene devices. The general structures for this kind of de-embedding are shown in Figure 17 [53]. The detailed algorithm for this kind of de-embedding is presented in [54] and will be addressed in section 4.1.3.

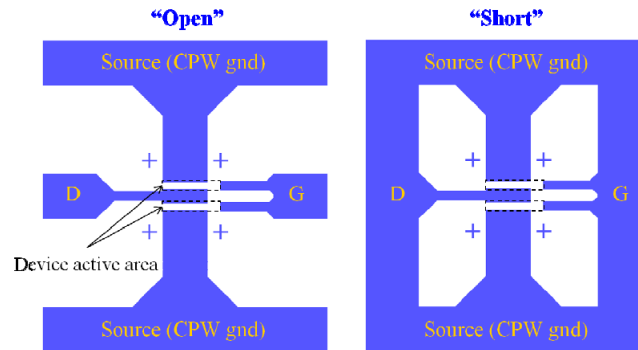


Figure 17 – Schematic of open and short structures used for the de-embedding of the devices presented in [53].

2.4.1 Graphene influence on transistor performance

As previously noted, while graphene exhibits excellent properties, it also presents certain electrical characteristics that must be considered during the development of graphene transistors, as they significantly impact electrical performance, namely, current saturation and quantum capacitance.

2.4.1.1 Electrical current saturation

The current saturation is one of the main drawbacks of the GFETs, reducing the applications of these transistors, since the current saturation is very important in analogue applications, for example in analogue amplifiers which operate at the saturation region of the transistor. When a transistor is in saturation, it should operate as an ideal current source, i.e., the output current is constant for a large range of voltages. Without current saturation, the GFET is only a voltage-controlled resistor with limited use for any electronic applications. Graphene channel has no “pinch-off” effect in the same way as a semiconductor channel does. The researchers claim that the current saturation exists in graphene, however, it is dependent of the charge trapping effects and dielectric materials [55]. The graphene experiences a quasi-saturation state, i.e., not a full saturation. In a real transistor the non-presence of a current saturation could be attributed to:

1. poor quality of graphene, i.e, bad sample;
2. non-optimal device structure;
3. high contact resistance;
4. too thick gate oxide, poor gate control of the channel;
5. non-optimal bias, i.e, no separate back-gate and top-gate;
6. trapped charges at substrate and oxide interface.

2.4.1.2 Quantum capacitance

A big capacitance is important since it provides a wider range of control of the electrostatically carriers. High-k dielectrics are important to prevent the tunnelling effect in transistors. As the channel length of the transistor shrinks the gate capacitance becomes comparable with the quantum capacitance. The quantum capacitance is a measure of the energy required to move the carriers from the source to the channel. Although the gate capacitance is constant, the effective capacitance that is responsible for modulation of the channel conductance varies due to the quantum capacitance. The short channel

transistors are dominated by the quantum capacitance instead of the electrostatic oxide capacitance, which compromises the function of the device. This quantum capacitance is a capacitance that appears in series in all graphene devices with the electrostatic gate capacitance. This capacitance is approximately linear on graphene varying with the channel voltage and with its minimum value at the Dirac point. The quantum capacitance of the graphene channel needs to be considered when the gate dielectric thickness is reduced. The total capacitance (C_t) of a device is given by:

$$C_t = \frac{C_{ox}C_q}{C_{ox} + C_q} \quad (4)$$

where C_{ox} is the gate electrostatic capacitance and C_q is the quantum capacitance.

2.4.2 Typical transistor devices

Despite the issues regarding the current saturation and quantum capacitance in graphene transistors, several studies have reported the use of graphene transistors for RF applications. Some works present simple layouts to demonstrate the feasibility of using graphene for transistor fabrication, while others report more complex designs aimed at enhancing the RF performance of graphene transistors. Starting from the simpler designs, in [56] a top-gated field-effect device is reported. A back gate was also fabricated to help in the improvement of the device's performance. Note that this is not an RF graphene device, but it is interesting to analyse this device since it is the standard design of a graphene field-effect device, and such interesting aspects are addressed. This graphene device was fabricated on top of an oxidized silicon wafer (300 nm) with mechanical exfoliated graphene, having the device been fabricated on a pre-identified single-layer graphene flake. All the metal materials used for the contacts were evaporated directly on top of the graphene, while evaporated silicon oxide was used for the gate dielectric. The fabricated device ($L = 0.492 \mu\text{m}$ and $W = 0.265 \mu\text{m}$) and its performance are shown in Figure 18.

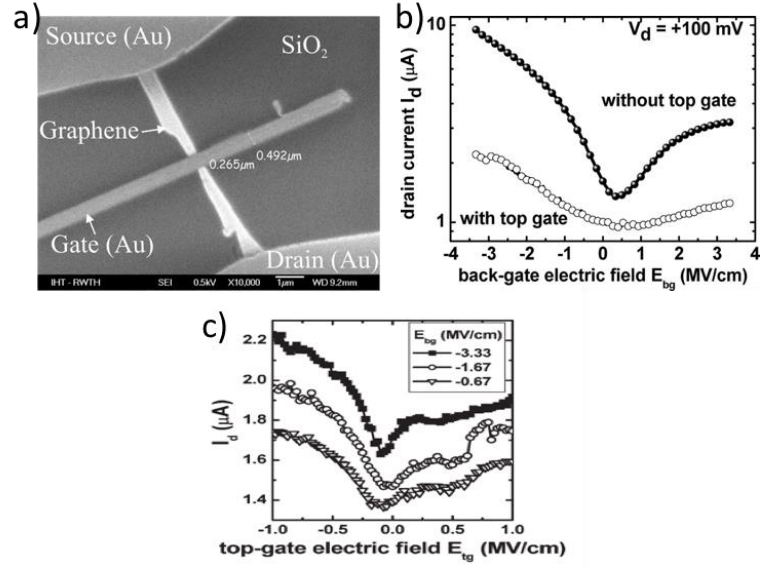


Figure 18 – Graphene FET: a) SEM image of the GFET reported in [56]. b) Transfer characteristics of the back gate Graphene FET with and without top gate. c) Transfer curves of the top gate Graphene FET for different back-gate fields (E_{bg}).

In [56], the degradation of the charge carrier mobility after the gate deposition was clearly observed. According to calculations, the carrier mobility of the graphene was $4790 \text{ cm}^2 \text{V}^{-1} \text{s}^{-1}$ and $4780 \text{ cm}^2 \text{V}^{-1} \text{s}^{-1}$ for the holes and electrons, respectively. After the gate deposition, these values decreased to $710 \text{ cm}^2 \text{V}^{-1} \text{s}^{-1}$ and $530 \text{ cm}^2 \text{V}^{-1} \text{s}^{-1}$, respectively. Obviously, and following the previous description, the drain current was also degraded after the gate deposition.

In [57], a back-gated and top gated devices were reported. Transistors with lengths down to 90 nm were fabricated. The general structure of the developed devices is shown Figure 19.

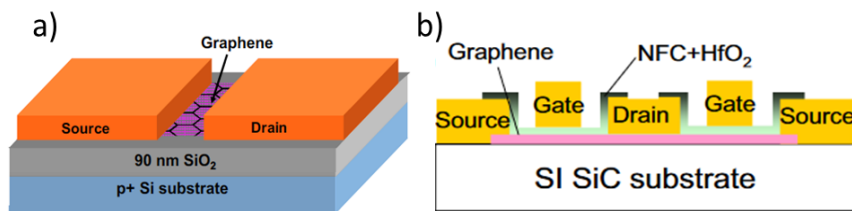


Figure 19 – a) Schematic view of the back-gated graphene FET and b) schematic view of the top-gated graphene FET reported in [57].

The e-beam evaporation was used to evaporate the contacts while the gate dielectric in top gated devices was NFC/HfO_2 . The highest achieved intrinsic cut-off frequency was 170 GHz on top gated devices with a drain voltage of 2.2 V, however, the authors claimed that this value could be increased if a self-aligned structure was used due to the decrease of the series resistance.

In [58], a top gated graphene field-effect transistor is presented by the authors. Note that this transistor was not designed for RF purposes, but an interesting novelty is featured. While using a gate length of 310 nm, the Dirac point was adjusted by simply changing the top gate material by Ti to Pd. This GFET device also has a high transconductance of 0.69 mS/mV. High mobility graphene was used ($5400 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$), which was obtained by mechanical cleavage of graphite. The dielectric used was yttrium dioxide obtained by thermal oxidation on the hot plate of previously evaporated yttrium film. The general schema of the reported transistor can be viewed in Figure 20.

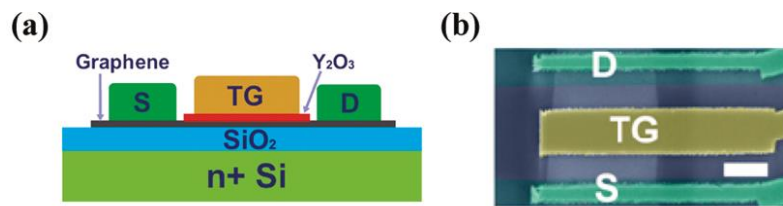


Figure 20 – a) Cross section schematic of the GFET reported in [58]. b) SEM image of the fabricated device with the channel length of $2.6 \mu\text{m}$ and the gate length of $1 \mu\text{m}$.

2.5 Discussion

In this section the oscillators fabricated using graphene transistors available in the literature were reported as well as the other types of oscillators. Despite the reported devices, with good performance, the fabrication processes lack of the integration with biosensors, and integration with other graphene devices. The fabrication of such devices is challenging, evidenced by the number of reported devices in the literature. The fabrication of graphene devices lacks the incompatibility of some CMOS processes with graphene.

The state of the art of RF graphene transistors was also presented in this chapter. RF graphene transistors are part of an emerging area that has had a tremendous growth in the last years due to the potential use of graphene on RF applications. However, there is still a lot of work to do in this research field. The quantum capacitance of graphene becomes significant as the gate length decreases, since it is of the same order of magnitude as the geometric capacitance. This results in performance degradation due to the reduced modulation of channel charge carriers. Therefore, a trade-off between channel length and the relationship between quantum capacitance and geometric capacitance must be considered. The low electrical current saturation in graphene remains as a challenge in the fabrication of graphene transistors. Currently, the main problem of RF graphene transistors is not the cutoff frequency (the extrinsic cutoff frequency remains a problem), but the maximum oscillation frequency due to the low

current saturation of the graphene devices, caused by its low gain. Several attempts are being made to increase the f_{max} of the transistors, which will be addressed later in this document.

In Table 1 the characteristics of more important reported transistors are presented. The I_d current was evaluated in a general scale since sometimes it is hard to precisely indicate the highest drain current of the device. Both the complexity of the process and the complexity in the integration with CMOS were evaluated qualitatively (low, medium and high). To note that this evaluation might be considered highly subjective, since the articles sometimes did not refer to anything about this topic. To note that not all the devices were shown in this chapter, however, will be addressed later in this document. These were added to add more information and variability in the analysis.

Table 1- Comparison between the performances of the reported transistors.

Ref	$f_{max,in}$ (GHz)	$f_{T,int}$ (GHz)	$f_{max,ex}$ (GHz)	$f_{T,ext}$ (GHz)	I_d range	g_m (mS/ μ m)	Device structure	Graphene technology	Process complexity	CMOS integration complexity
[57]	-	170	-	-	mA	0.025	Back and top gate	Grown on SiC	Low	Low
[59]	6.8	15.8	5.6	10.1	μ A	0.1	Top gate	CVD graphene on sapphire	High	Medium
[51]	50	34.5	21.3	42	μ A	0.46	Back gate	CVD graphene on metal foil	Medium	Medium
[53]	-	-	23	10	μ A	0.5	Top gate	CVD graphene on metal foil	High	Medium
[60]	105	96	-	-	mA	0.71	Top gate	Grown on SiC	High	High
[61]	-	100	-	35	mA	-	Back gate	CVD graphene	Low	Low
[62]	35	280	-	-	mA	2	Top gate	Grown on SiC	Low	Low
[63]	-	-	26	17	μ A	-	Back and top gate	CVD graphene	High	High
[64]	20	11.4	-	-	mA	0.29	Back gate	CVD graphene	High	High
[65]	200	255	106	70	mA	1.18	Top gate	CVD graphene	High	High

[66]	-	22	-	5	hundreds of mA	0.25	Top gate	Exfoliated graphene	Low	High
[67]	-	75	-	55	mA	0.36	Top gate	CVD graphene	High	High
[49]	29	427	-	-	mA	1.33	Top gate	CVD graphene	High	High

In Table 1 it is possible to observe the most relevant GFETs and their performances. The silicon MOSFETs were reviewed in [68], and the reported devices can be used to compare the MOSFET's performance with GFET's. In [62], the GFET with the highest transconductance is reported, 2 mS/ μm in contrast with the highest reported values for n-channel MOSFET of 1.84 mS/ μm , or 1.6 mS/ μm for p-channel MOSFET [69]. However, a higher transconductance was achieved in 3.45 mS/ μm in III-V FETs [70]. When analysing the f_T , the maximum value of 427 GHz was achieved. When compared with the MOSFET devices, this value is near the state of the art, with the highest reported value of 485 GHz [69]. Regarding f_{max} , the highest value was achieved in [65], 200 GHz. When compared with the reported devices in [68] the 450 GHz for an n-channel MOSFET was achieved. This highlights that, despite graphene's potential, further development is required to improve this figure of merit in graphene technology.

3 DESIGN AND FABRICATION

As discussed in the previous chapters, the design and fabrication of graphene transistors is challenging and requires careful consideration of both the design and fabrication processes. Since transistors serve as the fundamental units of ring oscillators, the oscillator type selected in this thesis, given its suitability for integration with biosensors and other biomedical devices, its fabrication is detailed in this chapter, with a primary focus on the fabrication of RF graphene transistors. Due to the limitations of the INL cleanroom, a trade-off between performance and fabrication capabilities must be considered. This chapter provides a comprehensive overview of the design approaches employed to meet the specifications required for fabricating the building blocks of the ring oscillators, specifically the transistors, while considering the available fabrication processes. Two fabrication processes are proposed and fabricated. It also outlines the strategies used to address the challenges encountered during the fabrication steps. The chapter begins with an exploration of how various design techniques are applied to optimize key parameters to achieve high-performance devices. Additionally, the fabrication of CVD-grown graphene is discussed, along with the challenges and optimization strategies involved in the material's production, since the fabricated graphene were used in the fabrication of the RF graphene devices presented in this thesis.

3.1 Materials and fabrication methods

As seen previously, only a few works with graphene oscillators were reported. This is due to the single atomic thickness of graphene which presents significant challenges, since many electronic fabrication processes traditionally used in silicon technology cannot be directly applied to graphene. These conventional processes often damage the graphene lattice, leading to performance degradation. The most critical and challenging step in the fabrication of RF graphene devices is the integration of a high-k dielectric on the graphene surface. Standard fabrication techniques typically damage the graphene lattice, altering its intrinsic properties or, in some cases, destroying it. Furthermore, the fabrication of graphene in a large scale is also challenging. The incorporation of a high-k dielectric is crucial to prevent excessive current leakage due to direct electron tunnelling. High-k dielectric materials enable an increase in the physical thickness of the graphene transistor's gate dielectrics while preserving the performance characteristics typical of thin SiO₂ layers. To address this challenge, several research groups are exploring innovative solutions, such as the physical gate transfer using core-shell nanowires [71] or the application

of thermal tape [72] to transfer pre-patterned structures. Additionally, self-aligned processes are being developed to minimize access resistance and parasitic capacitances, both of which are detrimental to RF performance.

The devices fabricated for this thesis were designed to be compatible with the INL cleanroom, as all fabrication steps were performed within these facilities, where parameter tunability is constrained by the requirements of other processes running in parallel in this cleanroom. INL's cleanroom (that are based on standard large scale fabrication processes), classified as ISO 5 class and spanning an area of 1,200 m², is equipped with cutting-edge tools for micro- and nanofabrication mainly optimized for 200 mm wafers, supporting applications across fields such as electronics, medical devices, microfluidics, energy, and sensor technologies. Despite the extensive capabilities, adjustments were necessary for graphene processing, as certain cleanroom processes are not fully optimized for graphene applications. For graphene growth, the facility includes an Easytube 3000 CVD system, while material deposition options include several specialized systems. The Kenosistec KS1000 PVD system is equipped with both RF and DC (Direct Current) capabilities, featuring a UHV multi-target setup with 11 magnetrons. This includes 3 RF magnetrons for depositing non-conductive materials and the remaining DC magnetrons for metal deposition, enabling the sputtering of thin films. The SPTS MPX CVD Module is designated for PECVD silicon oxide and silicon nitride depositions. Additionally, thin films such as Al₂O₃ (alumina) or AlSiCu can be deposited with the Timaris FTM system from Singulus. This machine has the availability to perform RF and DC sputtering (oxide and metals) with a good uniformity (70%) and conformality. The dielectric and amorphous silicon films are deposited using an SPTS PECVD machine, which can produce films in the nanometer to micron thickness range. For dielectric deposition, atomic layer deposition (ALD) is available, although only Al₂O₃ can be deposited. The system is the ALD Beneq TSF 200, which regarding its modular architecture is ideal for R&D activities, supporting thermal ALD, remote plasma ALD and direct plasma ALD. Lithography processes at INL include mask aligners and a direct-writing lithography (DWL) system from Heidelberg, with available laser beams at $\lambda = 405$ nm and $\lambda = 375$ nm, which provides significant flexibility for iterative R&D processes by allowing CAD layout exposures. For high-precision nanometer-scale work, an electron beam system of Vistec is available, the EBPG 5200 with an operation voltage of 100 kV and 50 kV; however, due to its cost and complexity, it is used sparingly. Supporting lithography, INL offers a priming oven and automatic coaters by Suss MicroTec. A critical point dryer is also accessible within the facility.

While INL is compatible for a range of CMOS processes, some limitations for graphene remain, particularly the lack of a gold evaporator, which is commonly needed for creating contacts in graphene

devices. Nonetheless, the facility's equipment supports many aspects of graphene-based RF device fabrication. In the following sections, key considerations in the development of RF graphene devices will be examined in detail with focus in graphene transistors since they are the building block of the ring oscillators which was the selected kind of oscillator to this thesis due to their small size and since the incorporation of graphene transistors with RF capabilities in graphene biosensors could be valuable to implement other kind of RF circuitry (RF mixers, frequency doublers or rectifiers).

3.1.1 Substrate for graphene transistors fabrication

The correct choice of the substrate for the graphene transistors fabrication impacts the performance and/or fabrication steps, as well as integration potential. The substrate may be imposed by the fabrication facilities, by the integration methodology required, or by the graphene fabrication and processing steps.

Graphene transistors can be fabricated on several substrates, with the most common being Si/SiO₂ [73], SiC [74], glass and quartz [75]. Graphene transistors are also reported in flexible substrates such as polyethylene naphthalate (PEN) [76] or polyethylene terephthalate (PET) [77]. These are very useful in nonplanar applications (wearables for example), with their low insertion loss being a good characteristic for THz applications [78]. The most used substrate is Si/SiO₂, due to their compatibility with the standard fabrication processes and the easy optical identification of the graphene on SiO₂. This property makes these the most suitable substrates for the fabrication of high-quality CVD-grown graphene devices after graphene transfer. The presence of a thick layer of SiO₂ on top of the Si substrate makes this substrate also very useful in RF applications, decreasing the parasitic substrate capacitances. SiC substrates are often used for the epitaxial growth of graphene for electronics applications, with the advantages of the use of the conventional top-down lithography techniques well established in nanotechnology [76]. In contrast to CVD-grown graphene, graphene grown on SiC substrates does not require a transfer. However, SiC-grown graphene remains cost-ineffective. Insulator substrates such as glass or quartz are very useful in graphene FET fabrication. These substrates bring advantages for RF applications due to their ability to reduce the parasitic substrate capacitance, reducing the RF losses associated with the substrates [79].

3.1.2 Oxide deposition on graphene

To fabricate RF devices, it is necessary to grow an oxide on top of the graphene, to do a gate oxide of a GFET or the center contact of a coil, for example. The first approach to grow a high-k dielectric on top of the graphene is the ALD, however, the lack of reaction sites on graphene turns this method more

complex than usual, being the deposition of continuous thin oxides hard. The intentional lattice damage, that improves the oxide layers adhesion, is not desirable [80]. In the case of the GFETs (and other transistors), a big C_{ox} is desirable, and consequently a thinner oxide, since it increases the transconductance and consequently the frequency performance of the device. However, thin oxides have high leak current and poor long-time reliability [81]. The appropriate choice of the gate oxide is very advantageous to the GFET performance, as reported in [82], where, despite the high-k of TiO_2 , the HfO_2 showed to be a better choice to increase the GFET performance. The deposition of a metal seed layer prior to the ALD showed to be effective in the ALD process, however, the deposition of the seed layer might cause graphene doping during the ALD process. The use of a metal as a seed layer affects the oxide k dielectric constant and the morphology of the oxide [83]. Other approach could be the growth of an induced layer of amorphous carbon by electron beam scanning as a seed layer for oxide deposition by ALD. In [84] a thin HfO_2 thin layer with 1.3 nm of EOT (equivalent oxide thickness) was grown, achieving a gate capacitance of $2.63 \mu F/cm^2$. The functionalization of graphene prior to the ALD deposition could be done by an ozone pre-treatment which allows a conformal deposition of the oxide with low mobility degradation and minimal graphene doping [85]. In this work, a tri-methylaluminium (TMA) and O_3 at $25^\circ C$ ALD was performed on a commercial ALD reactor to pre-treat the graphene prior to the Al_2O_3 deposition. Other surface treatments could be performed such as exposure to NO_2 [86]. Spin coated polymers prior to ALD were reported also, such as in [87], where a PVA polymer was adsorbed to graphene surface as seed layer for ALD due to its high dielectric constant (~ 6) leading to a gate capacitance reduction. Molecular buffer layers could be also chosen prior to the ALD deposition, such as the noncovalent functionalization of graphene by carboxylate-terminated perylene molecules in [88]. Boron Nitride could also act as a buffer layer for plasma enhanced atomic layer deposition (PE-ALD). With this technique, thin dielectrics of 4 nm could be grown without functionalization or need of a seed layer [89]. The use of hexagonal Boron Nitride (h-BN) as gate dielectric on top of graphene is also reported in [66] and [90]. This approach preserves the graphene mobility with a relatively high dielectric constant ($k \sim 4$), however, the wafer-scale device fabrication is not possible. New emergent fabrication processes are appearing based on top-down techniques, removing the need of the deposition/growth of an oxide on top of the graphene [49], [91], [92]. In section 3.2.5, this topic will be further explored, providing literature examples of graphene transistors where various fabrication approaches have been employed to develop RF graphene transistors.

3.2 Design techniques to improve performance of graphene devices

Despite the challenges associated with the fabrication methods discussed in subsection 3.1, particularly in selecting the appropriate substrate for graphene deposition and the optimal approach for growing the gate oxide to fabricate RF graphene transistors and, consequently, ring oscillators, there are several techniques that can be employed to enhance the performance of these devices. While these techniques inherently involve fabrication processes, their primary focus is on optimizing and improving the performance of the transistors. These techniques will be explored in the following subsections.

3.2.1 *Graphene contacts and contact resistance*

To achieve high performance in RF devices, mainly in RF transistors, it is necessary to achieve good contact between graphene and the metal. Numerous studies have explored methods to reduce contact resistance in graphene. This issue stems from the injection of charge carriers at the interface between a three-dimensional material (metal electrode) and the two-dimensional graphene layer. In short-channel GFETs, contact resistance can significantly impact performance, as it dominates the total resistance, rendering the modulated resistance of the channel negligible. To minimize the contact resistance (R_c), the selection of the metal contact must be carefully selected to achieve lower contact resistance. For example, the Pd provides a lower R_c when compared with Au [93]. To reduce the contact resistance several approaches have been studied such as the work function engineering of graphene work function under metal electrodes [94], the annealing of the contacts prior the graphene transfer (to remove the polymer residues that are stucked to the surface of the metal electrode) [95], cleaning the graphene surface prior the metal contacts deposition with UV/ozone plasma [96], edge contact of graphene with metal by the fabrication of antidots [97] or patterning graphene by introducing graphene cuts in the contact area [98], creating defects on graphene by thermal annealing in hydrogen of Ni contacts [99], adding a MoO₃ interlayer on contact between graphene and the metal electrode [100] or a clean transfer of graphene using gold as support layer [101]. Sandwiched contact structures have been reported also [102].

Regarding to the chosen metal and work function engineering, several studies are being carried out to understand how the contact resistance influences the device's performance and how this effect can be mitigated. The total resistance between two contacts is the sum of the semiconductor resistance, the contact resistance, and the metal resistance. Sometimes the metal resistance is neglected due to its low value when compared with the other two. So, by subtracting the graphene resistance from the total

resistance it is possible to obtain the contact resistance between the metal and the graphene. The contact resistance for each contact is half of the total contact resistance (Equation 5).

$$R_c = \frac{R_{total} - R_{graphene}}{2} \quad (5)$$

Where R_c is the contact resistance between graphene and metal, assumed to be the same for both contacts (source and drain), R_{total} is the total resistance measured between source and drain and $R_{graphene}$ is graphene channel resistance.

In [103] is possible to observe the influence of the chosen method for contact deposition in the contact resistance. For RF applications low contact resistances are preferable. In Figure 21 it is possible to see the measurement results of different methods of contact deposition.

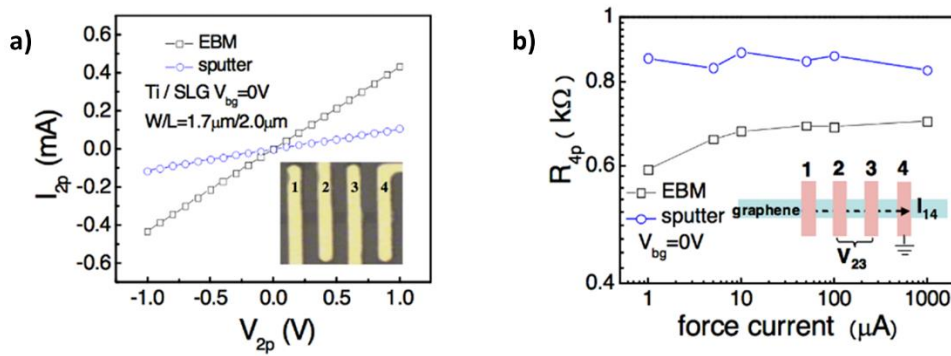


Figure 21 – a) The $I_{2p} - V_{2p}$ plots of Ti/SLG devices for EBM (electron beam evaporation) and sputter processes, respectively. The optical image of measured device is shown in inset of a); (b) The graphene resistance R_{4p} (R_{4p}) between two probes as a function of force current. The schematic for four-probe measurement is shown in inset of b. Adapted from [104].

After the measurements, the authors reported a contact resistance of 0.78 kΩ and 4.1kΩ for EBM (electron-beam evaporation) and sputter deposition, respectively. It is important to note that in GFETs where the contacts were deposited by E-Beam evaporator, the ρ_c (contact resistivity) is insensitive to the layer thickness, however, in the devices where the contacts were sputtered, the ρ_c exhibits layer dependence and increases with the decreasing of the layer thickness. It is important to note that, in multilayer graphene, this effect is not observed. In such cases, the ρ_c is compared with that of EBM devices. This is because, in multilayer graphene, the metal atoms primarily interact with the surface layers, creating vacancies where the metal penetrates, contacting the underlying layers. This interaction differs from single-layer graphene, where the contact resistance effect is more pronounced. Another resistance that sometimes is not considered when the GFET models are developed is the resistance between the

graphene and the substrate (typically SiO₂ or HfO₂). There are several techniques to reduce this resistance, but in some cases it should be considered such as in applications that require low leakage currents.

The Graphene-metal contact resistance, R_c , has proven to be the main responsible for degrading the transistor's performance. The contact resistance plays an important role on the transistor's performance, mainly when the gate length decreases, since this does not scale down with the gate length, playing an important role in the cut-off frequency, extrinsic transconductance, the maximum frequency of oscillation, the $I_{DS}-V_{GS}$ linearity and the limit of the on-current. Several contact resistances of the literature reported devices could be observed in the next table [104].

Table 2- Contact resistivity (Adapted from [104])

Metal/Graphene	$\rho_c \ \Omega \ \mu m$	Reference
Ni	500	[105]
Ti	>1000	[106]
Ti/Pt/Au stack	100	[107]
Cr/Pd/Au stack (1D edge contact)	100	[108]
Cu (Cuts patterned)	125	[109]
Pd (Cuts patterned)	457	[109]
Pd	185-900	[110]

Typically, graphene transistors have top and back gate, the back gate is used to dope the graphene reducing the contact resistance. The global back gate is used to dope the graphene under the contacts which significantly decreases the overall series parasitic resistance.

3.2.2 Access resistance in RF graphene transistors

Despite the importance of the contact resistance between the graphene and the metal, another resistance plays a big role in the RF GFET fabrication, the access resistance (R_a). This resistance is caused by the ungated graphene region, affecting the RF performance of the device. In [111] the impact of the R_c and R_a in GFET on quartz substrates was investigated separately. To reduce this resistance several works using self-aligned structures were reported. In [60] a self-aligned structure based on T-shape gate structure was implemented achieving an f_{max} of 105 GHz, in [15] a high-speed transistor with a self-aligned nanowire gate was reported with a f_t of 300 GHz with an extrinsic cutoff frequency bigger than 50 GHz in a quartz substrate [67]. In [112], a process for self-aligned gate graphene FETs was reported. In [113]

the access resistance was reduced by the chemical doping using polyethyleneimine with a 2.5 x increase in electrical performance, such as the transconductance.

3.2.3 Designs to improve the $f_{\max}$ of the devices

One of the main drawbacks of the GFET transistors is their low $f_{\max}$. As previously described, it is one of the most important FOM of the transistors since it indicates the transistor's power amplification ability. This low value is caused by the lack of a bandgap of graphene. Lowering the gate resistance (burying the gates, for example) could be a solution to improve the $f_{\max}$ [51]. In [59], a high-quality grown graphene was used to improve the quality of the device. The graphene was grown on a sapphire substrate that enables a clean transfer due to the absence of a metal to be etched, which could leave some impurities on graphene. In the abovementioned work, the authors fabricated a mushroom-shaped core-shell AlO_x/Al top-gate with 200 nm (Figure 22). A self-aligned process was employed to decrease the access resistance. The 10.1 GHz and 5.6 GHz were the extrinsic values of f_{T} and $f_{\max}$ of the device, respectively.

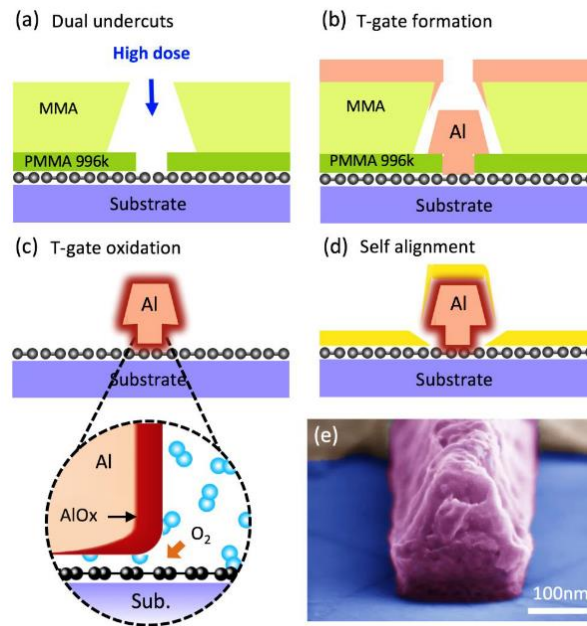


Figure 22 - Schematic illustration of the fabrication processes for the top gate and self-aligned process reported in [59]. a) Formation of the undercut using an e-beam exposure in an MMA/PMMA two-layer resist. b) Deposition of aluminium to fabricate the T-gate. c) Formation of the natural aluminium oxide layer by oxidizing the aluminium d) Metallization of self-aligned source/drain contacts. e) SEM image of the final device.

In [51], a $f_{\max}$ of 50 GHz was achieved with a buried-gate transistor (length 200 nm). Devices with 100 nm gate length were also fabricated, but the results were not satisfactory since the parasitic effects

have an important role in shorter channel transistors. The general fabrication process flow is shown in Figure 23.

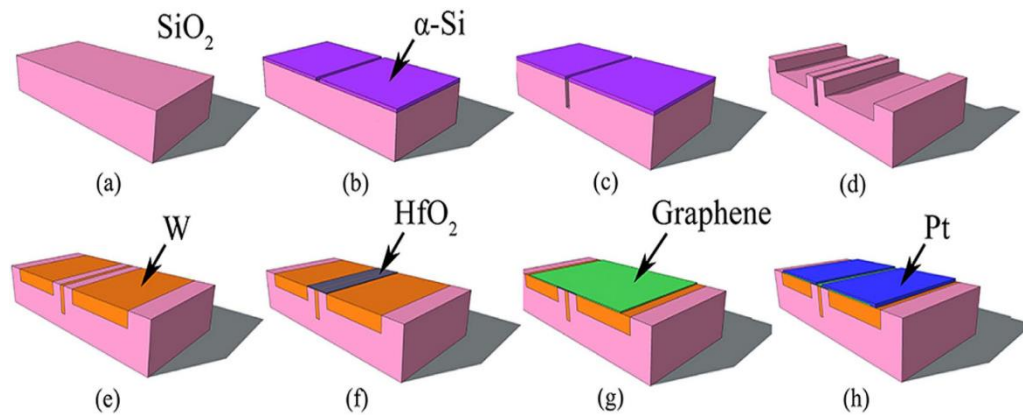


Figure 23 – Process flow of the devices reported in [51]. a) High-resistivity silicon substrate with SiO_2 on top. b) Hard mask sacrificial layer for the definition of the gate. c) Etching of the gate. d) Source/drain bottom contacts definition and etching. e) Tungsten (W) deposition and planarization (CMP). f) Deposition of HfO_2 gate dielectric. g) Graphene transfer. h) Lift-off of the source/drain top contacts.

These devices were fabricated in high resistivity silicon substrates following the Damascene process. The gates were patterned by e-beam lithography, followed by RIE (Reactive Ion Etching) to open the trenches. The metal was deposited by PECVD (plasma-enhanced chemical vapor deposition) and CMP (chemical mechanical polishing) was used to planarize the surface. After that, HfO_2 was deposited by ALD and the excess of HfO_2 was removed by ICP (inductive coupling plasma). The graphene used in this device was obtained by CVD growth on Pt foils. In Figure 24, it is possible to see the fabricated devices.

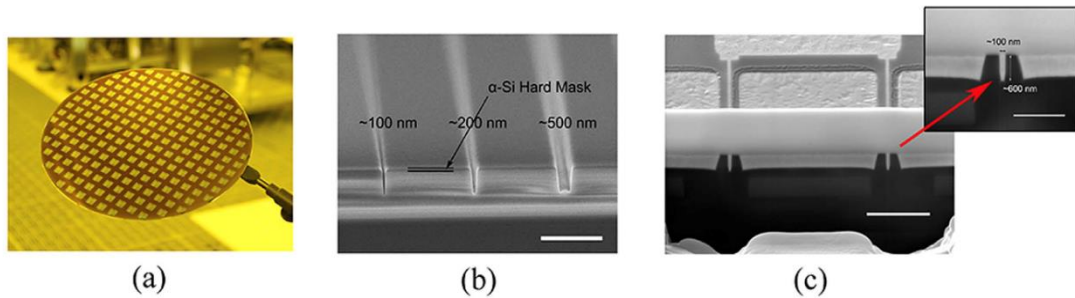


Figure 24 – a) Photograph of the fabricated devices on a 200 mm Si wafer. b) Buried gate trenches. c) SEM image of the cross-section of a 100-nm-gate-length GFET [114].

Another work that was developed with a view to increasing the f_{max}/f_T ratio was accomplished in [53]. In this work, a T-shaped gate was fabricated. This structure is similar to the one reported in [59], where a self-aligned process was used to minimize the access resistance. This technique allows small gate dioxide thicknesses of 2.3 nm, gate lengths down to 100 nm, and transconductance of 0.5 mS/mm. The best performance was obtained for a device with a gate length of 110 nm, with a f_T of 23 GHz, and a maximum oscillation frequency of 10 GHz (f_{max}). The graphene used for this device was grown by using

the standard CVD process on copper foils. A 3D photoresist process was employed to pattern the T-gate. In addition, an aluminium film was evaporated to form the Al_2O_3 gate dielectric after oxidation on air. Subsequently, a thin layer of palladium was used to do the self-alignment of the source and drain electrodes, and finally, devices with multi-finger (double gate) were tested as well. The general process flow of the reported transistor can be observed in Figure 25. In Figure 26 it is possible to see the fabricated devices.

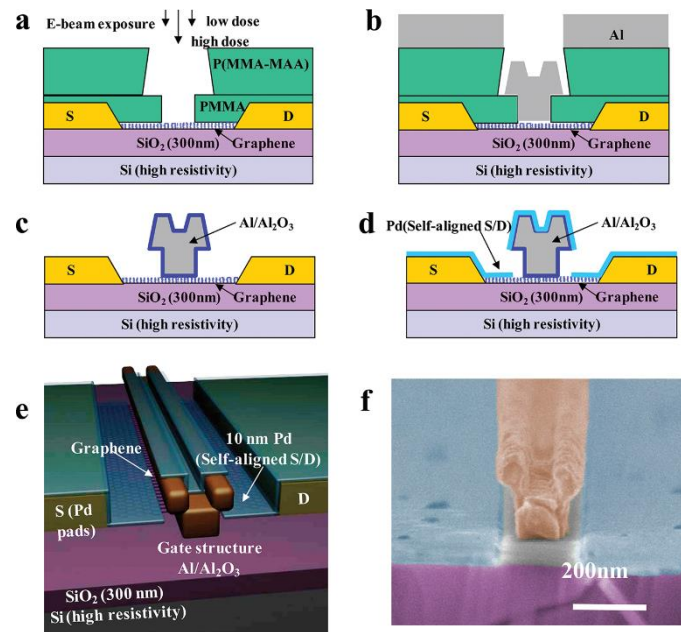


Figure 25 – Fabrication flow and schematic diagram of self-aligned GFET reported in [53]. a) Bilayer PMMA resist exposed in e-beam. b) T-shaped gate formed by the deposition of Al. c) Oxidation of the Al gate in air to form an Al_2O_3 layer after the PMMA resist removal. (d) Self-aligned source and drain contacts fabrication by the deposition of Pd. e) Diagram of the final GFET. f) Cross-section of the final device,

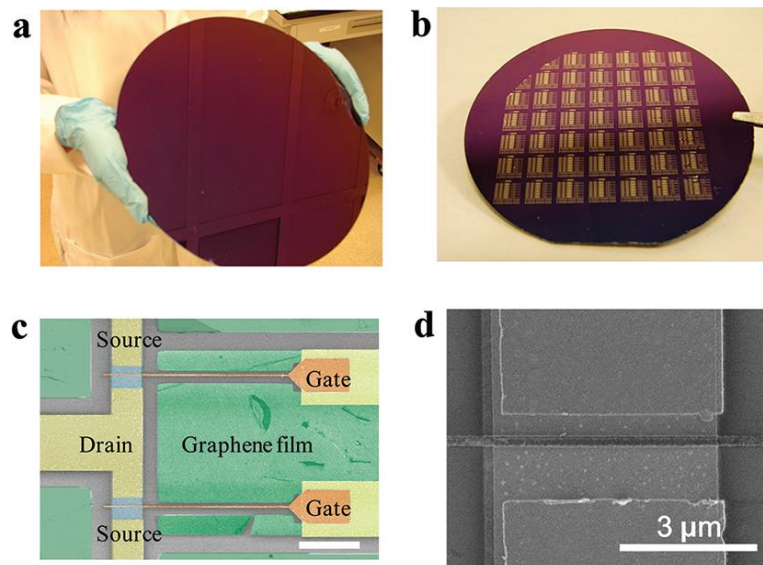


Figure 26 – a) Silicon wafer with transferred graphene on top. b) Photograph of fabricated graphene devices. c) Artificial color SEM image of a self-aligned graphene transistor with multi-gate configuration. d) SEM image of the transistor channel [53].

The authors of [60] describe an ultra-clean self-aligned process to achieve high $f_{\max}$ in double gated GFETs. In the aforementioned article, the authors used gold to transfer graphene instead of the more commonly used PMMA. The rest of the process is very similar to the previously reported one. The same article reports on an $f_{\max}$ of 105 GHz in a 100 nm gate length transistor, and the achieved f_r was 96 GHz. The general overview of the process is shown in Figure 27.

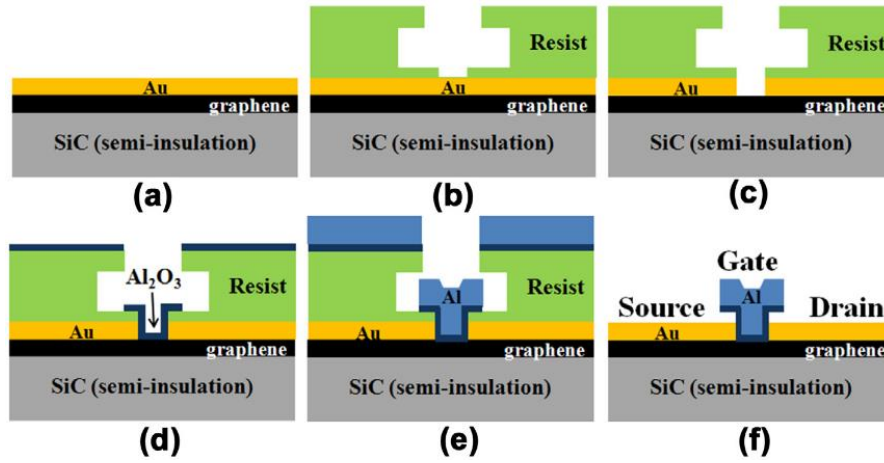


Figure 27 – Fabrication flow of a self-aligned graphene FET, reported in [60]. In a) is shown the deposition of gold on top of graphene, b) shows the patterning of the resist for a T-shaped gate, c) shows the etching of the gold under the gate, d) shows the deposition of 2 nm of Al, which is self-oxidized to Al_2O_3 , forming the gate oxide, e) shows the deposition of Al to form the gate contact, and f) shows the cross section of the final device.

3.2.4 Multiple gate transistors

In this area of multiple-gated devices, several devices were made by the researchers as an attempt to increase the yield of the GFETs, since double gated transistors allow for better control of the channel. A dual gate GFET is proposed in [61]. The Al_2O_3 , which was naturally oxidized on exposure to air from an aluminium film, was used as the gate oxide of this device. Pure gold was used on drain/source electrodes to decrease the access resistance of the device, and the graphene was grown by the standard CVD process on copper foil. The best device performance achieved was obtained in 180 nm channel length and 12 μm of channel width devices. The achieved extrinsic and intrinsic f_r was 100 GHz and 35 GHz, respectively. Figure 28 shows the fabricated device.

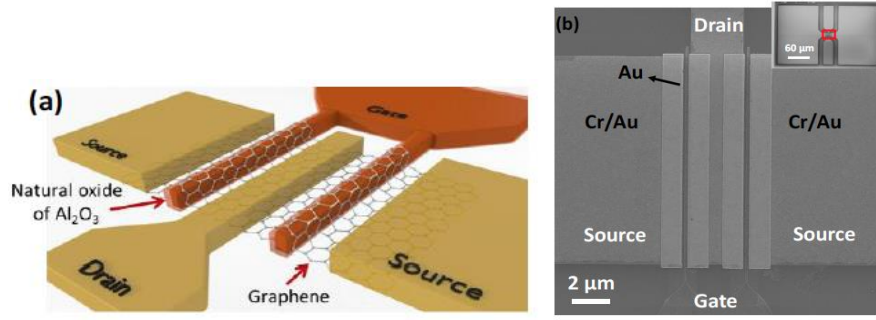


Figure 28 – Multiple-gated GFET with natural oxide of aluminum [61]. a) 3-D schematic of the fabricated device. b) SEM image of the multi-gated transistor.

Another work with multiple gate was reported in [62] and the fabricated device is described in Figure 29. In the mentioned work, the authors aimed to improve the performance of the GFET by optimizing the gate dielectrics and by doping the graphene channel. The graphene was grown on top of a SiC substrate. The gate dielectric oxide was 15 nm of Si_3N_4 deposited by PECVD, and HfO_2 deposited by Atomic Layer Deposition (ALD). Gate lengths as small as 40 nm and 1 μm width were fabricated. The authors selected this small width to minimize the domain boundaries and non-uniformity within the channel. An output transconductance of 2 mS/mm and an output current of 5mA/mm were achieved. An extrinsic f_T of 280 GHz was achieved for this graphene transistor. The authors claimed that an f_{max}/f_T ratio larger than 1 was achieved in most of the fabricated devices.

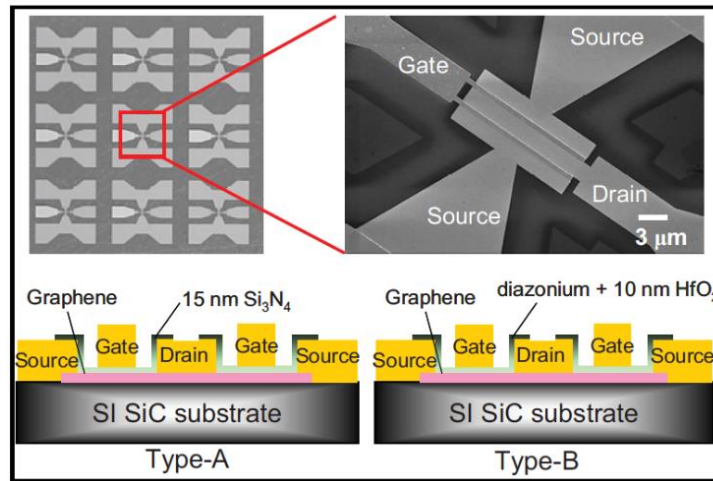


Figure 29 – SEM image of the fabricated multiple-gate transistor on top, and cross section of the device on the bottom, reported in [62].

In [115], a high mobility dual GFET with Al_2O_3 gate dielectric was fabricated. As previously mentioned, high-k dielectrics are important to achieve high GFET transconductances. The authors of the abovementioned work used Al_2O_3 as the gate dielectric, deposited directly on the graphene's surface by ALD, after the evaporation of a 1-2 nm thick layer of aluminium due to the hydrophobic surface of

graphene. This method provides a low interaction with the surface of graphene, which preserves its high mobility. The graphene flakes used in this work were exfoliated from bulk natural graphite by mechanical cleavage. To prove that this was a non-aggressive method for the graphene's surface, a dual gated GFET of 2.4 μm and 6.6 μm was fabricated. The high mobility of the graphene was preserved ($8000 \text{ cm}^2 \text{V}^{-1} \text{s}^{-1}$). The general scheme of the reported device can be observed in Figure 30.

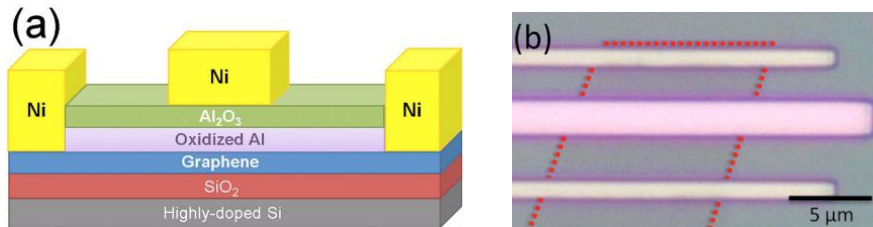


Figure 30 – a) Cross section of dual-gate GFET structure. b) Optical microscope image of the fabricated GFET [115].

Another dual-gate transistor was reported in [63]. This transistor was based on the same assumptions as the previous ones, but a buried gate and a top gate were fabricated. This strategy was adopted as an attempt to increase the f_{max} of the transistor. According to the authors, an improvement in the current saturation and gate resistance in GFETS will improve the f_{max} , and the buried gates reduce the fringing capacitance between gate and source/drain electrodes [116]. The fabrication process was similar to the one reported in [51], but the gate dioxide was replaced by 15 nm of Al_2O_3 deposited by ALD to form a 300 nm gate device. CVD grown graphene was used for these devices. An f_{max} and an f_{T} of 26 GHz and 17 GHz were achieved respectively, which corresponds to an $f_{\text{max}}/f_{\text{T}}$ ratio of 1.5. The process flow of the reported device is shown in Figure 31.

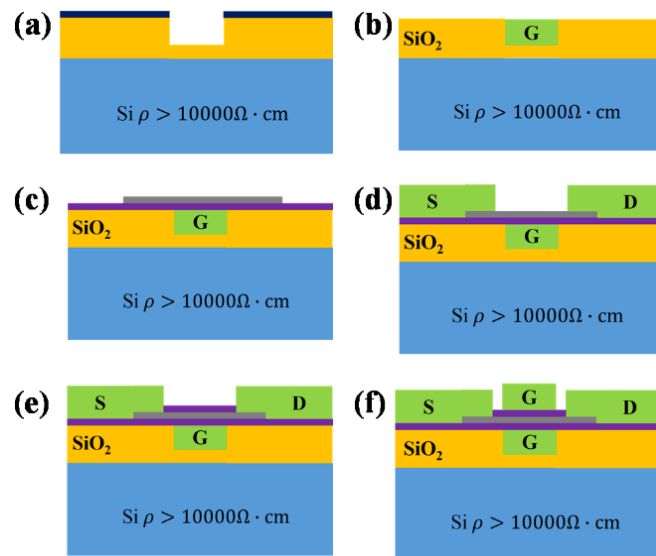


Figure 31 – Schematic diagram of the fabrication process reported in [63]. a) Etching of the buried gate. b) Ti/Au deposition. c) ALD deposition of Al_2O_3 and graphene transfer. d) Source and drain contacts definition. e) Growth of the top-gate dielectric by ALD. f) Top-gate fabrication [63].

Further information regarding the advantages of the use of buried gates can be found in [117]. Another approach that has attempted to increase the $f_{\max}$ was the one reported in [64]. In the latter, a multi-finger T-shaped gate transistor was reported to decrease the gate resistivity and the parasitic capacitance, to achieve a bigger $f_{\max}$. A thick SiO_2 layer was grown on top of a high resistivity silicon substrate, and deep trenches which define the bottom part of the T-gate were defined by RIE. A standard lithographic process was used to fabricate the T-gate. The used gate oxide was 10 nm of Al_2O_3 deposited by ALD. After that, the graphene was transferred and patterned. The general flow of the fabricated device can be seen in Figure 32.

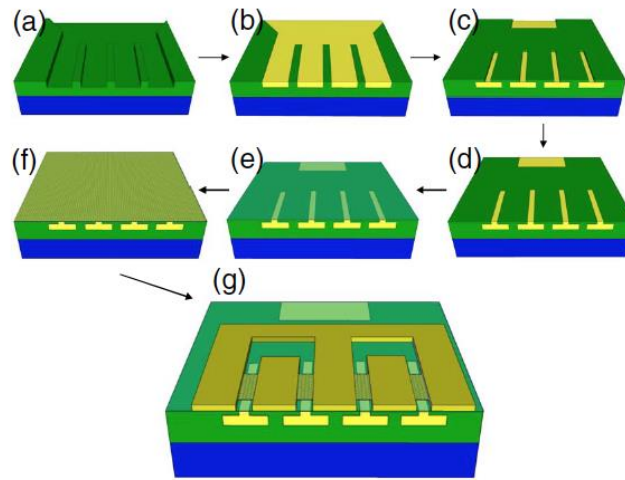


Figure 32 – Schematic of the fabrication process reported in [64]: a) RIE of bottom part of the T-gate. b) Filling the trenches with Cu and planarization with CMP. c) and d) Similar process of a) and b) to form the top gate. e) Growth of 10 nm of Al_2O_3 by ALD to form the gate oxide. f) Monolayer graphene transfer. g) Deposition of the metal contacts and graphene patterning.

In the aforementioned work, the $f_{\max}$ was 25% to 43% bigger than the f_r , highlighting their ability to deliver power across a broader range of frequencies. Furthermore, a wafer-scale process for graphene GFETs was reported. The fabricated device is shown in Figure 33.

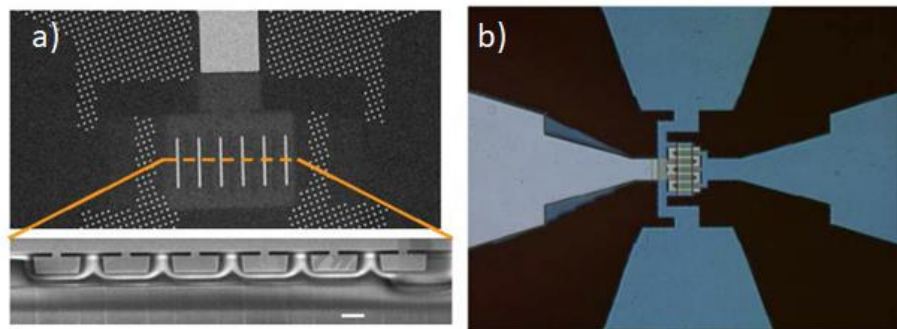


Figure 33 – Images of the graphene transistors reported in [64]: a) SEM image of the cross-section of the embedded T-gate. b) Optical micrograph of the device.

The results in [65] reported that a 200 GHz maximum oscillation frequency in CVD grown graphene GFETs was achieved. This improvement was achieved due to a novel transfer technique, preventing graphene from organic contamination. A self-aligned process was used to decrease the access resistance. The multi-gate fabricated devices with 60 nm gate lengths exhibit a high $f_{\max}$ of 106 GHz and 200 GHz, before and after the de-embedding, respectively. An obtained transconductance of 11.8 mS was achieved. In that work, an Au film as a sacrificial layer was used to avoid the presence of the organic compounds on top of the graphene's surface. The method also enables an ohmic contact between graphene and the Au film. The lithography steps were done directly on top of the Au film, and not on top of graphene. The Au film was etched by a $KI+I_2$ solution and a T-shaped gate was patterned. A thin film of Al was deposited to be oxidized on air to form the Al_2O_3 gate oxide, whose thickness was increased by an ALD process. Both the description of the process and the fabricated device are shown in Figure 34 and Figure 35, respectively. A similar process was reported in [60].

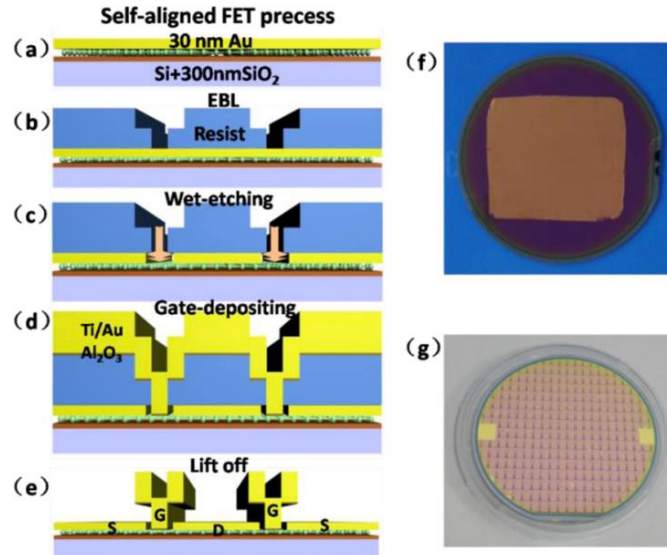


Figure 34 – Schematic of the fabrication flow of the fabricated devices: a) 30 nm Au/graphene on Si substrate. b) trilayer photoresist for T-gates patterned by E-beam lithography. c) Gold film under the T-gates etched away. d) Ti/Au deposited on top as the gate metal after the deposition of the gate dielectric by ALD (Al_2O_3). e) Lift-off to fabricate the final devices. f) Photograph of the transferred graphene with Au. g) photo image of the patterned silicon wafer with the patterned GFETs [65].

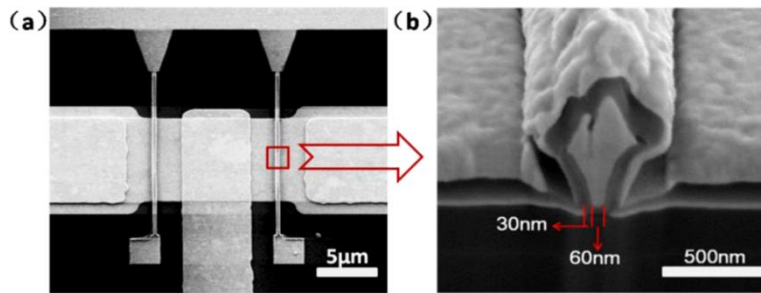


Figure 35 – Images of the GFETs reported in [65]: a) SEM image of a dual-gate GFET. b) FIB (Focused Ion Beam) image of the cross-section of the GFET.

3.2.5 Other solutions for transistor gate dielectrics

In the previously mentioned publications, it is possible to note a great effort made by the researchers to place high-k dielectrics directly on top of graphene. ALD is the most used technique and the least aggressive for the graphene lattice. However, another way to place a dielectric on top of graphene could be by transferring h-BN film. In [90], a h-BN film was used as the gate dielectric and support substrate. Despite the low dielectric constant of the h-BN film (~ 3.4), the authors showed that this technique was able to preserve the high mobility of graphene, improving the current characteristics of the device. The h-BN film was obtained by direct exfoliation of h-BN single crystals and the thickness of the gate dielectric was approximately 8.5 nm. The advantage of using this material is its flatness, which is 3 times less rough than the silicon oxide, commonly used on GFET transistors. Back-gated devices with $3.4 \mu\text{m}$ of width and $2.8 \mu\text{m}$ of gate length were fabricated. Finally, currents of more than 1 mA/mm were achieved. The fabricated device can be observed in Figure 36.

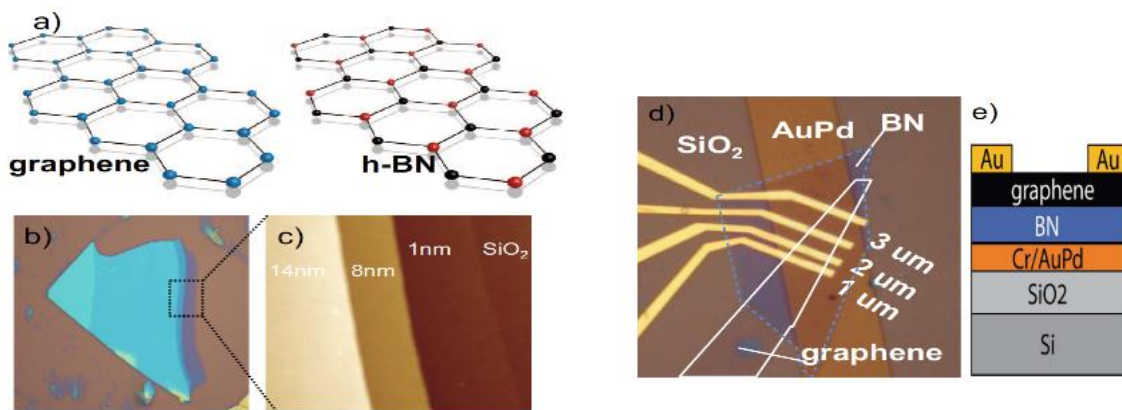


Figure 36 – Back-gated GFET with h-BN gate dielectric: a) Schematic of the atomic structure of the graphene and h-BN. b) optical image of an exfoliated h-BN flake. c) AFM image of h-BN with different layer thickness. d) optical image of GFET. e) Cross-section schematic of the back-gate device structure [90]

In [66], h-BN was also used as the gate dielectric. In that work, two layers of h-BN were used, one to act as the passivation layer of the silicon, and another one to act as the gate dielectric. This technique allows for the preservation of the graphene quality and consequently of the graphene carrier mobility. The achieved f_T after de-embedding was 22 GHz on devices with 450 nm of gate length and $3 \mu\text{m}$ of gate width. A high current density of 1.2 A/mm was achieved. The fabricated device is shown in Figure 37.

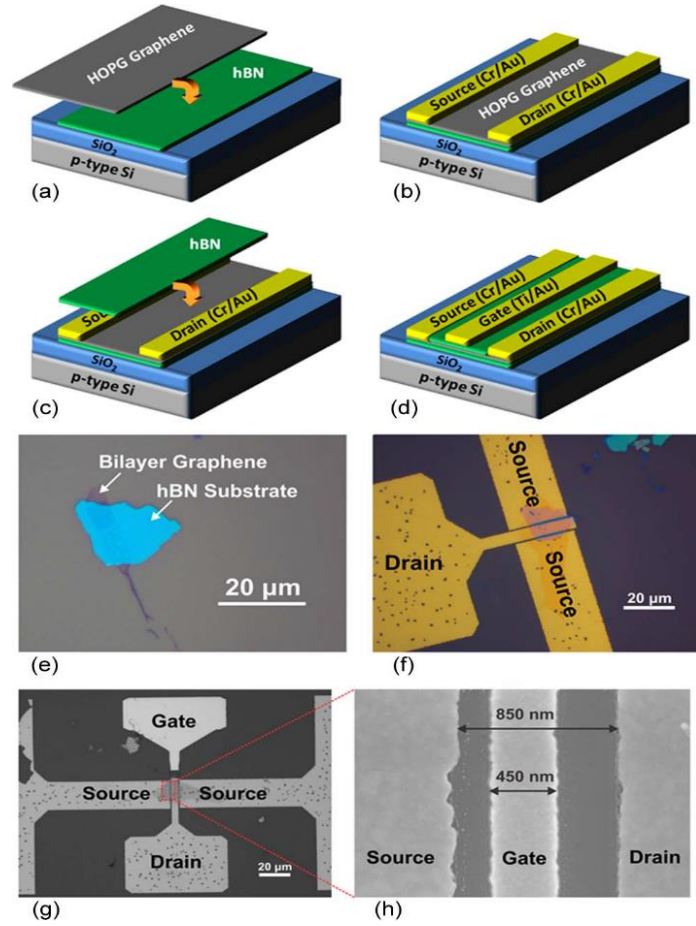


Figure 37 – a) to d) Fabrication steps of the BN/graphene/BN FETs. e) Optical image of a bilayer graphene flake exfoliated and transferred on top of the h-BN substrate. f) Optical image of the final device. g) Optical micrograph of the final device. h) SEM image of the final device [66].

In works [15] and [67], the authors proposed the use of a core-shell nanowire as the gate of the GFET. In [67], the used substrate was glass to avoid the power loss through the substrate, thus minimizing the gate parasitic capacitance. The process consists of the precise alignment of the source-gate-drain electrodes, minimizing the access resistance. The physical assembly of a nanowire on top of the graphene material prevents the damage of the graphene lattice to preserve its properties. The nanowire was assembled by dielectrophoresis on top of CVD grown graphene. The shell (Al_2O_3) of the nanowire was deposited by ALD and the core of the nanowire was constituted by Co_2Si . The general flow of the fabrication process and the fabricated device are shown in Figure 38 and Figure 39, respectively.

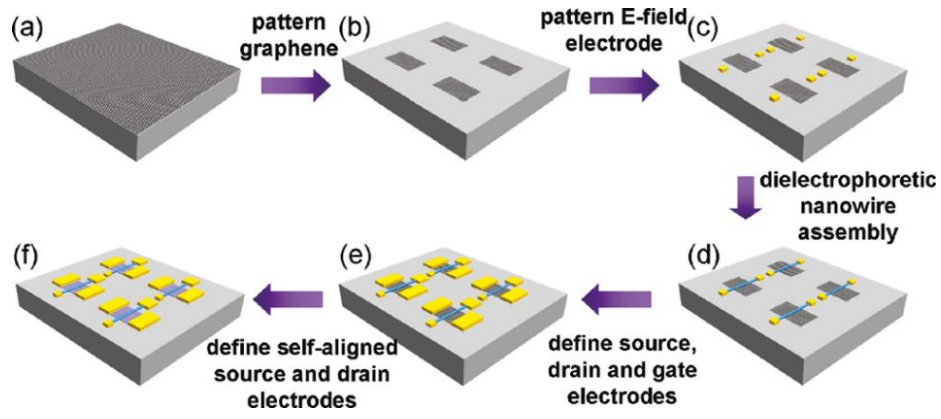


Figure 38 – Schematic illustration of the fabrication steps of the top-gated graphene transistor [67].

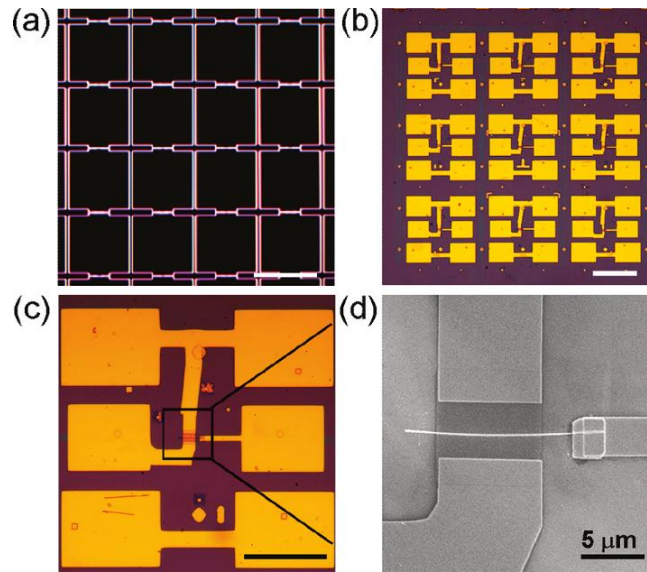


Figure 39 – Self-aligned graphene transistors reported in [67]. a) Optical image of the assembled nanowire array. b) Optical image of GFETs and c) Zoom in of b) in one GFET. d) SEM image of GFETs showing the channel and the gate nanowire.

The previously reported transistors were able to achieve high extrinsic cut-off frequency, higher than 50 GHz, with a 170 nm gate length (diameter of the nanowire). Despite the good results achieved, this is a hard process to develop and replicate since positioning the nanowires is challenging. Further work undertaken to preserve the graphene lattice characteristics using a physical gate transfer is reported in [49]. In that publication, the access resistance is reduced due to the self-aligned technique that was employed. The authors report that a high intrinsic f_r and f_{max} of 427 GHz and 29 GHz were achieved. Furthermore, it is also reported that a pre-patterned structure was transferred with the help of a thermal release tape directly on the top of the glass and Si/SiO₂ substrates, and CVD grown graphene was previously transferred to the top of this. The gate stack was constituted by Al₂O₃/Ti/Au. In addition, the gate stacks were easily peeled off by thermal release tape due to the low adhesion between SiO₂ and Au.

Finally, the source-drain electrodes were patterned after the gate stack transfer. The general process can be seen in Figure 40.

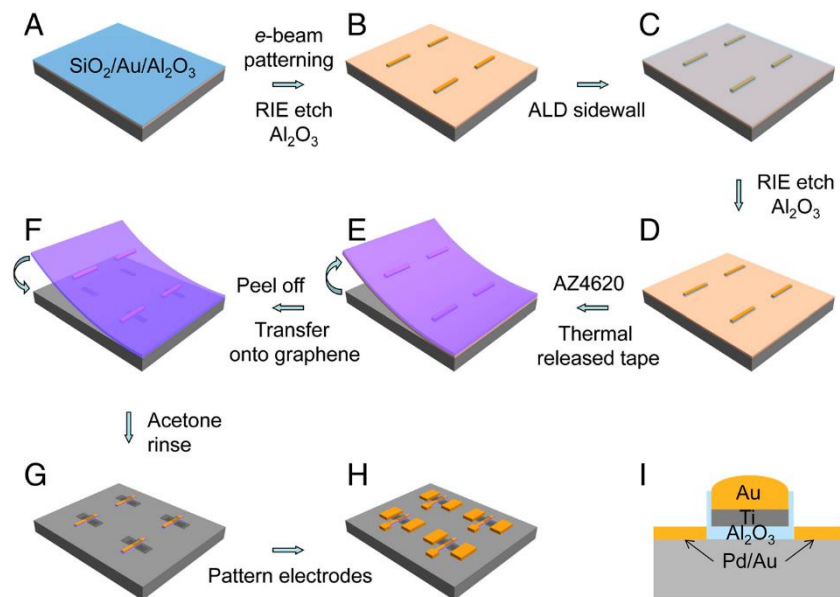


Figure 40 – Illustration of the fabrication of self-aligned graphene transistors with transferred gate stacks reported in [49].

The final aspect of the fabricated devices is shown in Figure 41.

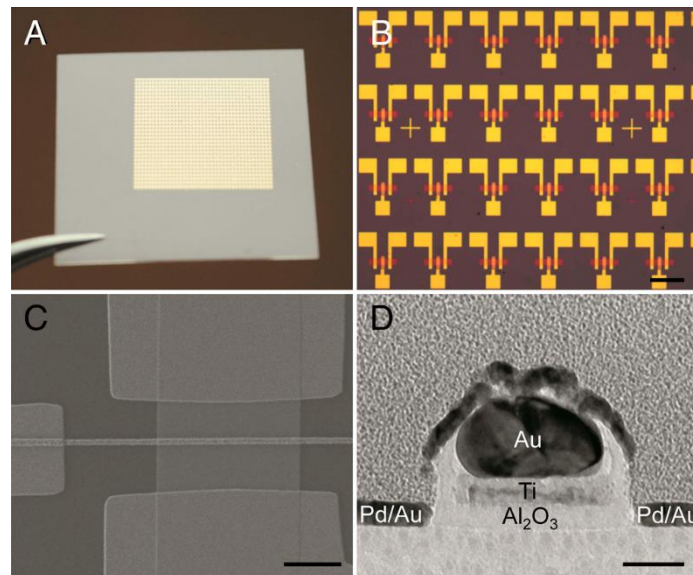


Figure 41 – The self-aligned GFETs: a) Photo image of the final devices on a glass substrate. b) Optical image of the GFETs. c) SEM image of the channel of the GFET. d) TEM image of the cross section of the final device [49].

As previously discussed, several critical factors must be considered for the fabrication of RF graphene transistors, the fundamental component of ring oscillators. These include the reduction of gate resistance, achieved by employing buried gates, and the use of high-quality graphene. Minimizing access resistance is also essential to enhance the performance of RF graphene transistors, as mentioned earlier. The use of a high-resistivity silicon (HR-Si) substrate, with a SiO_2 layer on top, is crucial to mitigate parasitic substrate effects, especially when compared to doped silicon with SiO_2 .

For improved RF performance, the integration of thin gate oxides with high-k dielectrics is essential. Such materials enable better electrostatic control of the gate, which is critical for achieving a voltage gain greater than 1. Atomic layer deposition (ALD) is the preferred technique for oxide deposition due to its minimal impact on the graphene surface. Alternatively, the transfer of pre-patterned physical gates (metal/oxide stacks) or oxide films such as h-BN has been explored, although these approaches pose additional challenges for scalability.

While reducing the channel length is beneficial for faster transistor switching, it requires a trade-off due to short-channel effects inherent in graphene transistors. These effects can compromise gate control over the channel. The implementation of multi-gate transistor architectures mitigates this issue by improving channel control. As highlighted earlier, chemical vapor deposition (CVD) graphene is the most employed material due to its scalability and tunability, ensuring consistent device performance.

Based on these considerations, the following strategies were selected to maximize the performance of the fabricated transistors:

1. Implementation of buried gates to reduce gate resistance.
2. Minimization of access resistance by depositing source/drain electrodes at the end of the process (via a damascene process) to align gate, source, and drain electrodes.
3. Use of a high-resistivity silicon substrate with a SiO_2 layer to minimize parasitic effects between the device and substrate.
4. Incorporation of a thin oxide layer grown via ALD using a high-k dielectric (e.g., alumina) to enhance gate control over the channel.
5. Adoption of CVD graphene to enable large-scale process scalability and optimize graphene quality for device performance.

It is important to note that these approaches were selected not only based on their technical advantages but also to ensure full compatibility with the fabrication processes available at the International Iberian Nanotechnology Laboratory (INL), one of the key objectives of this thesis. Consequently, alternative

methods such as physical gate transfer or h-BN as a gate oxide were excluded due to their scalability limitations. Despite the fabrication of multi-gate transistors, they do not exhibit better performance compared to single-gate devices and, therefore, will not be discussed further in this thesis.

3.3 Fabrication of RF graphene devices

The main goal of this work is to fabricate RF graphene ring oscillators for biomedical applications. As previously discussed, the fundamental building block of a graphene ring oscillator is a graphene inverter, which is composed of several graphene transistors (as it will be addressed in section 4). Therefore, the processes required to fabricate graphene transistors capable of operating under RF conditions have been thoroughly researched. To achieve scalability in graphene technology, CVD graphene is being used. The transfer of graphene from the growth substrate to the final substrate poses significant scalability challenges and introduces defects that can adversely impact the performance of graphene devices. For the fabrication of RF graphene devices, the use of a high-k gate dielectric is required to maximize the RF performance. This is due to the increased oxide capacitance, which leads to a higher total capacitance and consequently a higher cutoff frequency (f_T). Nevertheless, depositing or growing such materials on top of graphene is challenging due to graphene's 2D nature, its hydrophobicity, and the lack of reactive sites, particularly when using atomic layer deposition (ALD). This often results in the island-type growth of Al_2O_3 on the graphene surface. To avoid this issue, researchers have been transferring physical gates, but this approach is difficult to scale.

Buried gate topologies have been reported in the literature as a viable method for fabricating graphene devices due to their relatively straightforward fabrication process. However, the use of global back gates is not perfect because they polarize the entire graphene layer, which modulates the graphene under both the source and drain electrodes, leading to variations in resistance during device operation. When a thick oxide is used, a relatively flat surface is obtained for the graphene transfer, minimizing issues during the transfer process. However, challenges arise when a gate contact needs to be patterned on a thin oxide layer, which is preferred for RF applications as it reduces parasitic resistances compared to top-gate configurations. The use of a thin oxide can lead to significant surface topography, complicating the graphene transfer process. Although directly transferring graphene onto a rough surface might result in small cracks, it simplifies the fabrication process.

Given this, two approaches will be presented in this thesis. First, a bottom-gate graphene device fabrication process without surface planarization, along with a detailed discussion of the associated

challenges. To achieve a crack-free graphene transfer, a critical point drying process was developed and employed to dry the samples, preserving the graphene lattice characteristics. In the other approach, a surface planarization technique using ion milling prior to graphene transfer was applied, resulting in the successful fabrication of a buried gate RF graphene FET, demonstrating the effectiveness of the planarization process.

The diagram of the two fabrication processes reported in this thesis can be seen in Figure 42.

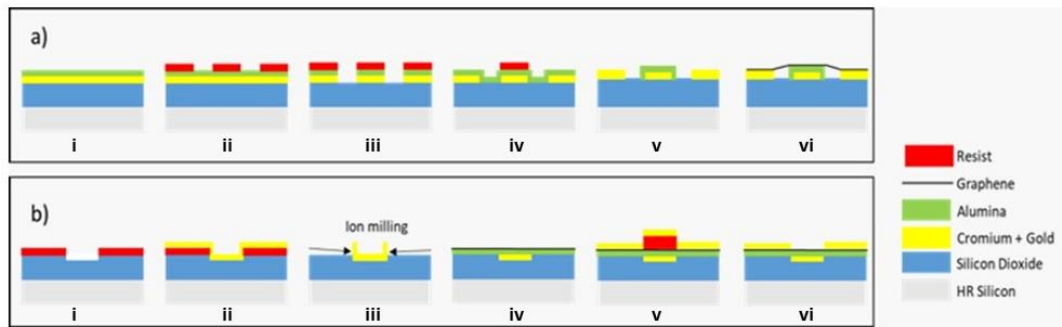


Figure 42 – Diagram of the two main processes reported in this thesis with and without planarization, a) and b) respectively. In a) i) HR silicon wafer with chromium + gold and alumina on top; ii) e-beam lithography to define source, drain and gate contacts by ion milling; iii) device after ion milling; iv) e-beam lithography to define the gate oxide after the growth of fresh alumina by ALD (after the resist removal by O_2 plasma, and alumina by wet etch); v) result after the patterning of the gate oxide by ion milling; vi) final device with graphene. b) i) device after e-beam lithography and ICP RIE; ii) after the chromium gold deposition; iii) after the lift-off, showing the ears to be removed by ion milling, to planarize the device; iv) after the graphene transfer; v) after the e-beam lithography and copper + gold deposition to define the source/drain electrodes by lift-off; vi) final device.

3.3.1 Bottom-gate graphene device fabrication process without surface planarization

The fabrication of the first structure (bottom-gate without planarization) began with a p-doped silicon wafer, on which 500 nm of SiO_2 was grown via PECVD. This choice of substrate was driven by cost considerations, as the p-doped wafers were used as a “dummy” option during the process validation phase. Since the process was successfully validated, high-resistivity (HR) silicon wafers were used for the final structures. Subsequently, 3 nm of chromium and 97 nm of gold were deposited by sputtering. To define the contacts using ion milling, 10 nm of alumina was sputtered on top of the gold to facilitate the removal of the photoresist. After alumina deposition, the sample was prepared for electron beam (e-beam) lithography. The wafer was coated with AR-N 7520.18 1+1, and e-beam lithography was performed to pattern the source, drain, and gate contacts. The contacts were then patterned using ion milling at an angle of 130 degrees, followed by 165 degrees to remove redeposited metal “ears.” The photoresist was stripped using an oxygen plasma, and an aluminum etchant (Fujifilm AES) was employed to remove the alumina, resulting in a clean surface devoid of resist residues. These steps are shown in Figure 43.

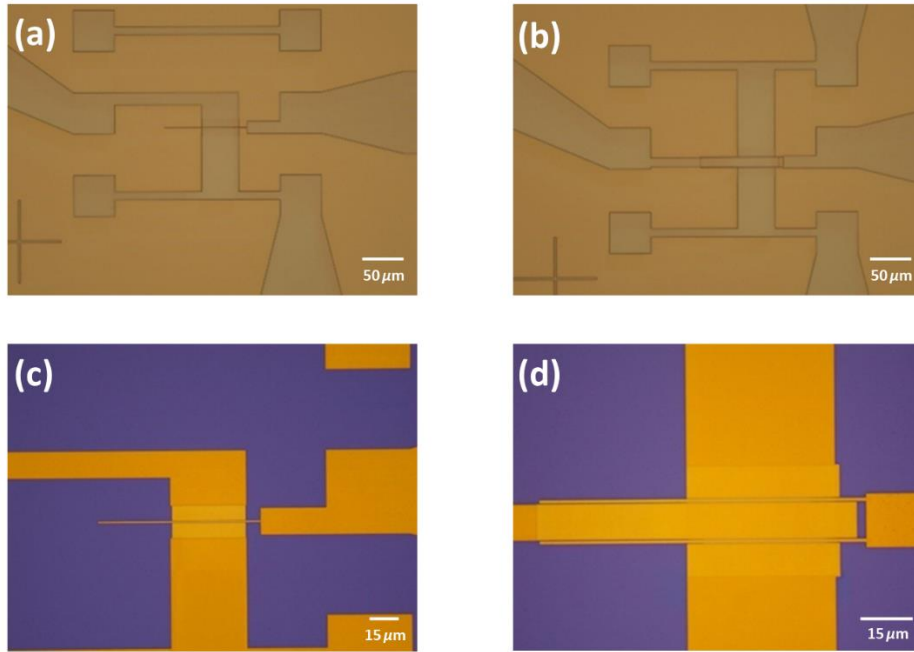


Figure 43 – First steps of the fabrication process with a) and b) showing an optical image of the lithography and c) and d) showing the optical micrograph after the ion milling and the resist removal by an O_2 plasma.

Next, 10 nm of Al_2O_3 was deposited by ALD to serve as the gate dielectric. The dielectric was patterned using ion milling after an e-beam lithography with AR-N 7520.18 1+1. The photoresist was then removed using an oxygen plasma, as illustrated in the Figure 44 and Figure 45.

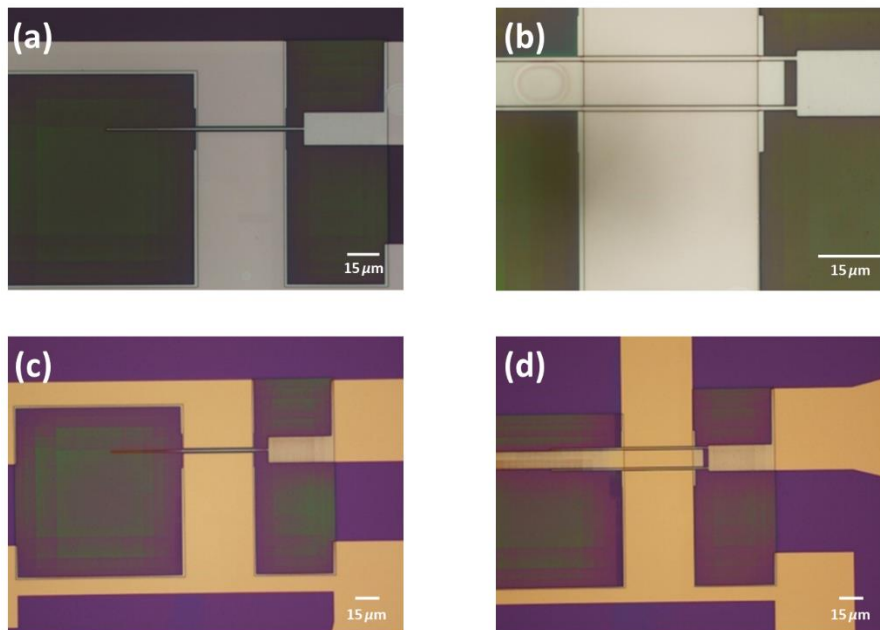


Figure 44 – a) and b) show an optical image of the lithography performed to pattern the gate dielectric (alumina) and c) and d) shows the optical image after the ion milling. To note, since the gate is very thin, some e-beam resist was left to act as anchor of the e-beam resist responsible for the patterning of the gate dielectric.

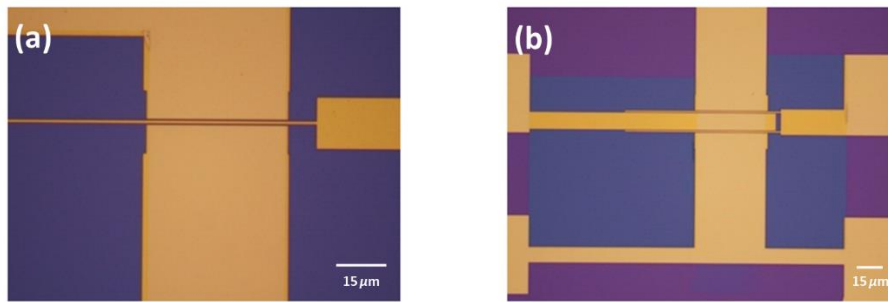


Figure 45 – a) and b) Optical photograph of the device after the resist removal with the oxygen plasma.

CVD graphene grown on copper foil was transferred onto the top of the structures using a PMMA-assisted wet transfer method (as detailed in the next chapter). Shortly, prior to the transfer, an O_2 plasma treatment was applied to the back side of the copper foil (which contains the graphene protected with the PMMA) to remove the graphene from that side. The copper foil was then etched in an iron chloride solution. Subsequently, the graphene-PMMA stack was transferred to an HCl solution to remove iron chloride contaminants and then to water before the final transfer to the substrate. Prior to the transfer to the final substrate the substrate surface was dehydrated and primed using a vapor prime oven to promote the adhesion of the graphene to the final substrate. After the transfer, the graphene was dried at room temperature. The PMMA was then removed using acetone. Finally, the graphene was patterned using an O_2 plasma beam following lithography with AZ1505. The resist was removed using acetone. In Figure 46 it is possible to observe the graphene laying in the graphene channel.

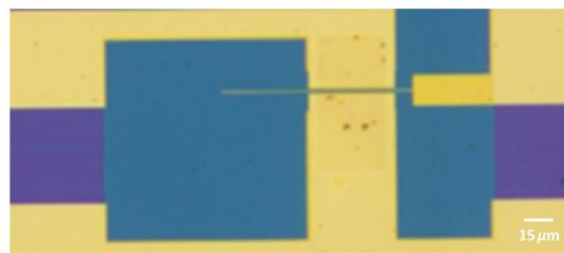


Figure 46 – Optical image of the graphene laying in the channel of the device.

To evaluate the feasibility of using graphene flakes in GFET fabrication, devices were constructed using this kind of graphene. The growth of such flakes will be addressed later in this document. However, the substandard quality of the flakes, likely resulting from inadequate handling during post-fabrication, led to unsatisfactory device performance. The Figure 47 presents the performance of these fabricated devices. Additionally, as this process was implemented on p-doped silicon wafers, the devices did not exhibit RF performance.

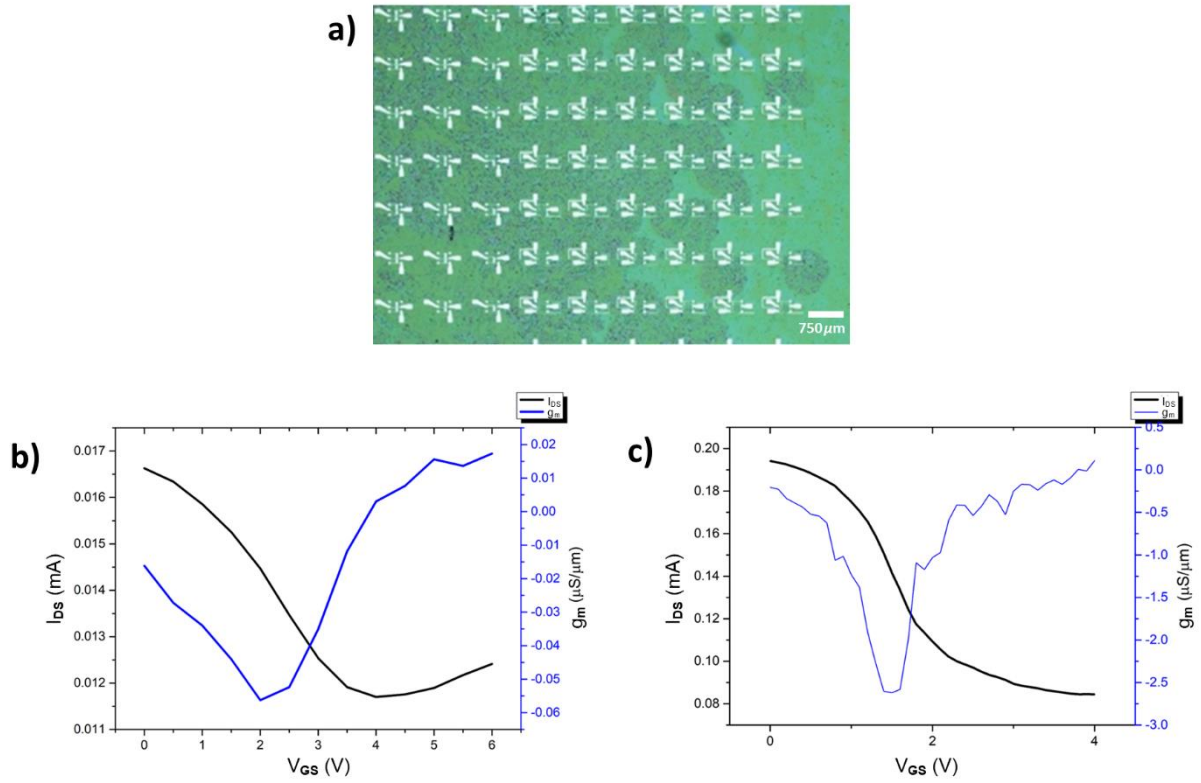


Figure 47 – Microscope image of the patterned substrate with the graphene flakes (a) and V_{gs} vs I_{DS} and g_m characteristic curves of devices presented in that substrate with $W = 35.6 \mu\text{m}$ and $L = 1.19 \mu\text{m}$ (b) and (c).

Since the graphene flakes did not yield satisfactory results and a large area of continuous graphene is essential for achieving high yield in device fabrication, continuous graphene films were used in a new sample replicating the same fabrication process. The p-doped silicon wafer was replaced by a high-resistivity silicon wafer to minimize parasitic capacitances from the substrate. Due to the small gaps between the source and drain contacts, the drying process is critically important. Two approaches were tested with the continuous graphene film after patterning (using O_2 plasma, as it was discovered that graphene only breaks after patterning, i.e., after the removal of the photoresist, not after the removal of the PMMA used for transfer).

In the first approach, the sample was dried on air. In the second approach, critical point drying was used. In the first approach, due to the surface tension of acetone (during the drying process), resulted in damage to the graphene at some sites, making it unsuitable for RF device fabrication (see Figure 48 c) and d)). For thicknesses above approximately 500 nm, the graphene tends to conform to the surface of the contacts rather than remaining suspended (see Figure 48 b)), which mitigates the impact of the drying process. This observation supports the use of coplanar structures in sensor fabrication, where graphene on the sidewalls enhances sensor sensitivity [118]. The performance of the fabricated devices is shown in the next section.

In contrast, the second approach, using critical point drying, allowed the graphene to remain suspended due to the uniform drying process (see Figure 48 e) and Figure 48 f)).

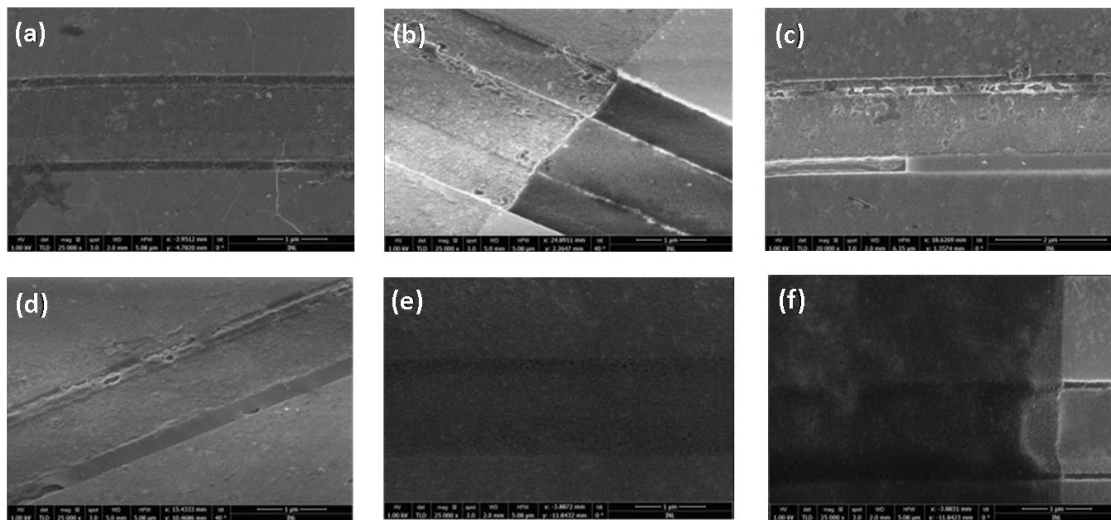


Figure 48 – SEM images of graphene after the transfer. a) after the transfer without the patterning, b) after the patterning with graphene following the topography of the contacts, c) and d) suspended graphene patterned and dried on air evidencing the cracks and e) and f) after the patterning and dried with critical point dryer.

To address this issue, and to simplify the process, a planar bottom-gate topology was developed.

3.3.2 Planar buried bottom-gate topology

The gate contact was buried within the SiO₂, and its surface was planarized using ion milling. Initially, 500 nm of SiO₂ was grown on a high-resistivity silicon wafer via PECVD. The gate contact was defined using e-beam lithography, involving the sequential spin coating of ARP 617.03 and ARP 6200.09 resists. These resists were selected to simplify the lift-off process for the gate metal. An ICP RIE was performed to open the SiO₂ trenches without compromising the resists for the lift-off process. Without removing the resist mixture, 3 nm of chromium and 67 nm of gold were sputtered onto the sample. The metal was subsequently lifted off using a solution of NEP with ultrasonic agitation. Due to the lift-off process, lift-off ears were observed, as shown in Figure 49 a). These lift-off ears were removed by ion milling at a 174-degree beam angle, resulting in a flat surface suitable for graphene transfer (see Figure 49 b) and c)). To note that in c) it is possible to see only small ears around 4 nm, which could be assumed as a flat surface for graphene.

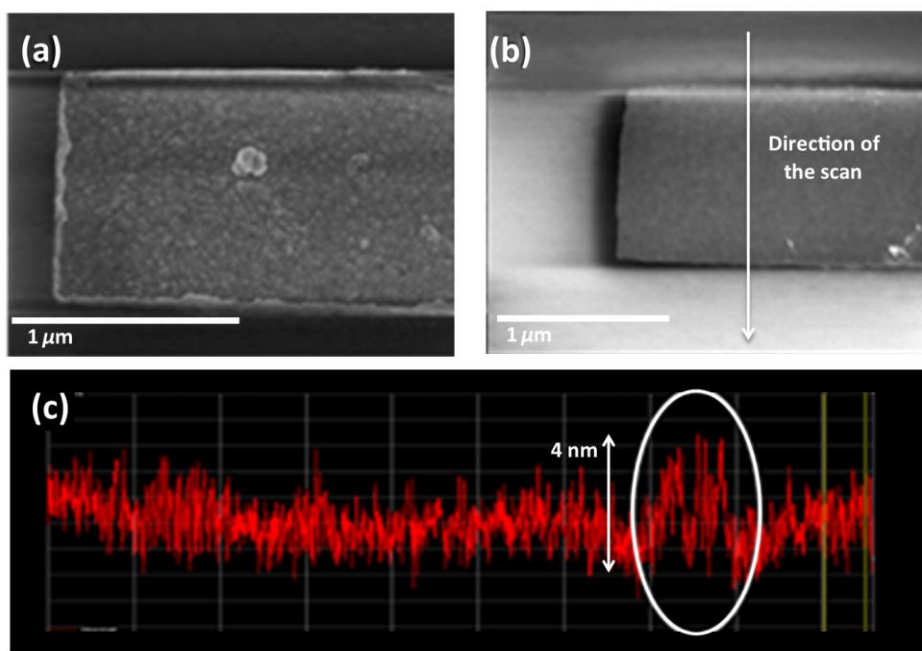


Figure 49 – SEM images of the gate structures showing the metal ears a) and after the planarization b). c) Profilometer measurement of the gate after the planarization.

After planarization, 10 nm of alumina was deposited using atomic layer deposition (ALD) at 200°C. Standard optical lithography was then employed to selectively remove the alumina via wet etching to expose areas for probe contact. Graphene was subsequently transferred onto the surface and patterned into various shapes to optimize the contact resistance between the metal and the graphene (Figure 50 a) and b)).

The selected patterns for the graphene were: no pattern, horizontal and vertical rectangles (with width of 1 μm and length of 28 μm separated by 2 μm center to center for vertical rectangles and with width of 2 μm and length of 35 μm separated by 4 μm center to center for horizontal rectangles), circles (with diameter of 2 μm separated by 4 μm center to center), and crosses (with a width of 2 μm separated by 5 μm center to center). The source/drain electrodes were defined using e-beam lithography with a PMMA bilayer (ARP 617 + ARP 679). Following this, 5 nm of copper and 50 nm of gold were sputtered and then lifted off using acetone. Copper was chosen as the adhesion layer because sputtered chromium, when used with gold, exhibited higher contact resistance compared to copper. It is important to note that after the graphene transfer in both fabrication processes, the quality of the graphene was assessed via Raman spectroscopy. Figure 50 c) and d) show the final device and the planarized surface with graphene.

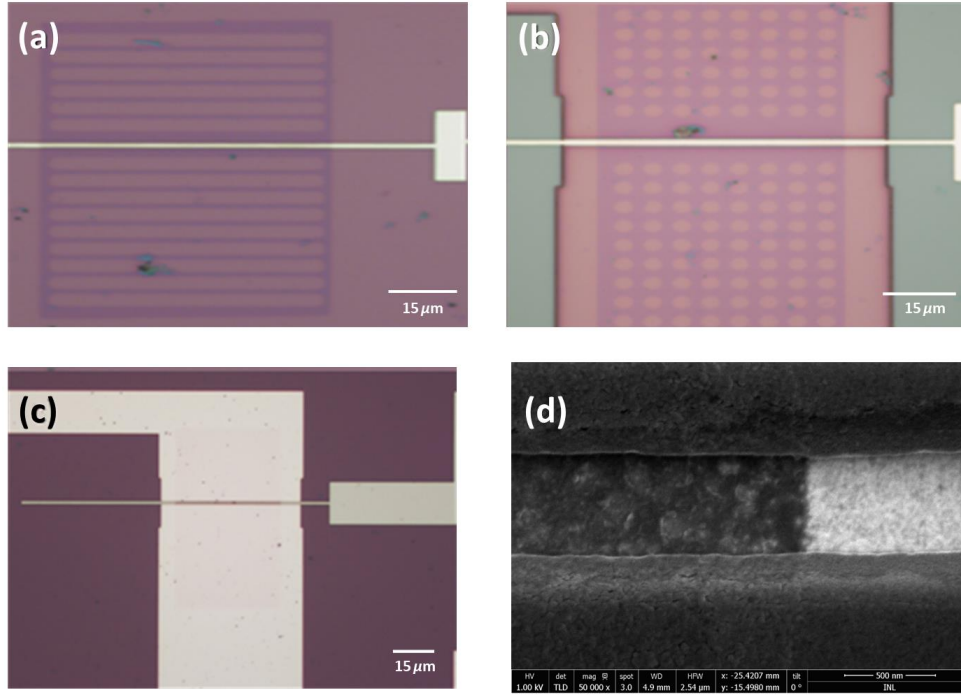


Figure 50 – a) and b) optical image of different graphene patterns used in graphene to reduce the contact resistance, c) optical image of the final device and d) SEM image of the final device showing graphene without cracks.

3.3.3 Planar buried bottom-gate topology improved

To optimize the RF performance of the GFETs (according to the observed in chapter 4), the buried gate process was replicated with a modified gate oxide thickness, decreasing it to 5 nm. While decreasing the gate oxide thickness typically results in a higher gate capacitance, which can decrease the cut-off frequency (f_T), it simultaneously improves the electrostatic control over the channel. This improved control enhances the transconductance (g_m), which can lead to an overall increase in f_T . Given that the goal of this thesis was the fabrication of a graphene ring oscillator, a variety of different structures were fabricated to explore the potential of this technology. These structures ranged from individual inverters to more complex oscillator circuits, incorporating graphene capacitors designed to modulate the oscillation frequency. The various fabricated structures and the corresponding schematics are illustrated in the following figure.

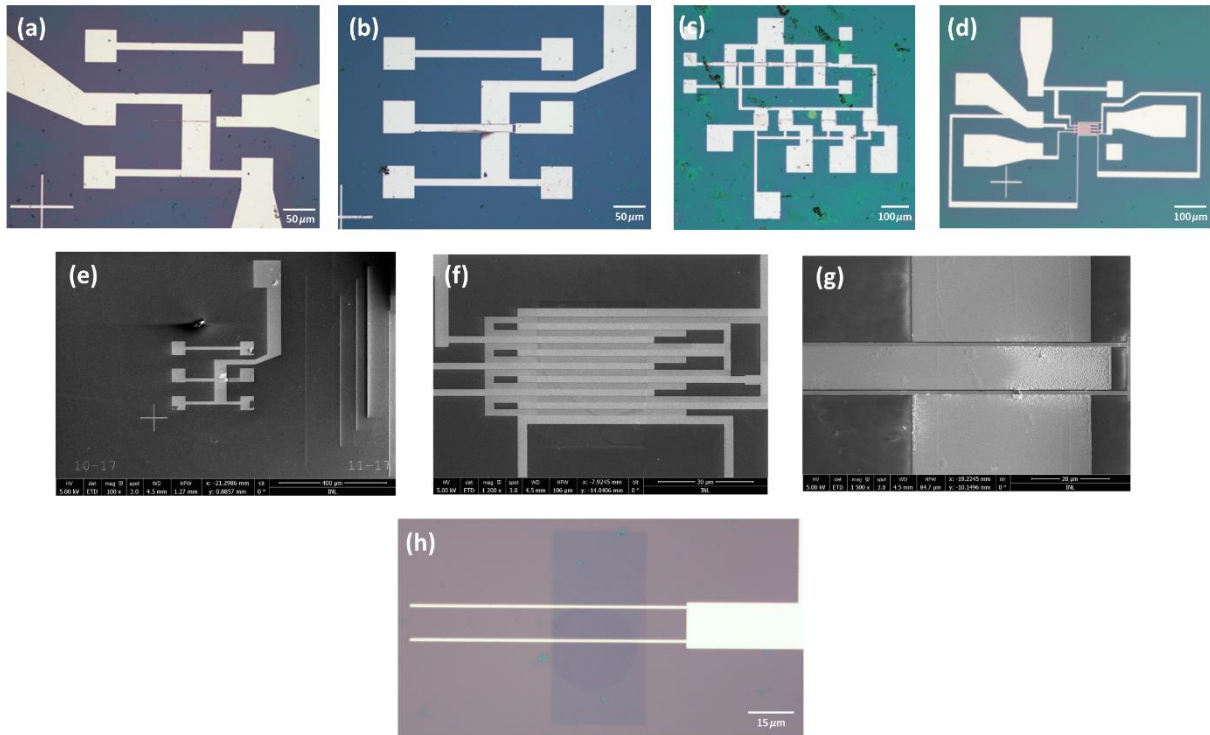


Figure 51 – Different types of the fabrication structures, a) single gate transistor, b) inverter, c) ring oscillator with variable graphene capacitors through back gate and compact ring oscillator, e) SEM image of an inverter after the electrical measurement showing the contact pads scratched or damaged, f) SEM image of the compact ring oscillator, g) SEM image of the channel of the inverter and h) microscope image of the clean graphene laying in a gate of a device prior the deposition of the remaining contacts (in this case an inverter).

The structure in Figure 51 c) was designed to provide access to each signal within the RF oscillator. Due to the significant length of the interconnections, it is expected that any oscillation, if present, would occur at lower frequencies, attributed to the additional capacitance introduced by the signal lines. The structure in Figure 51 d) involved the fabrication of a standard RF graphene ring oscillator, following the design detailed in [119]. In Figure 51 c) graphene structures with capacitor behaviour that feature back-gate capabilities were added. This enables tuning of the graphene capacitance via the back gate, based on a parallel study that will be published shortly. By modulating the back-gate voltage, it was expected that the oscillation frequency could be altered through corresponding changes in the graphene capacitance. This approach presents a promising avenue for the development of biosensors, where analyte detection is facilitated by frequency shifts. Furthermore, this concept enables the integration of graphene capacitors or the engineering of interconnects that can be functionalized with specific target analyte receptors, thus expanding the potential applications in sensor technologies. In the following chapter, the performance of the various fabricated structures will be evaluated, accompanied by a detailed discussion of the results.

In this process, as in the previous fabrication steps, monocrystalline graphene was used to achieve a high yield in the fabrication devices. The graphene was carefully transferred onto the substrates to maintain its crystalline integrity. To ensure the quality and continuity of the graphene layer, Raman spectroscopy was employed. The graphene spectra can be observed Figure 52.

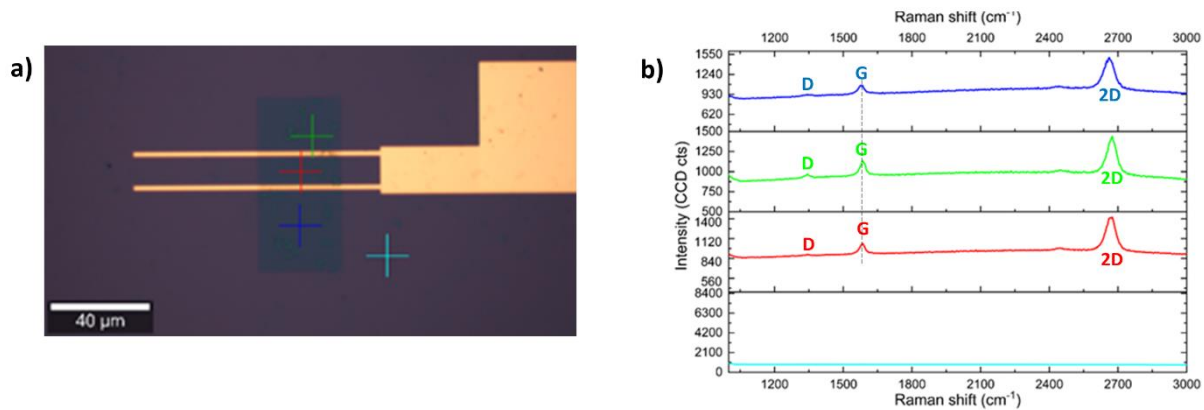


Figure 52 – Raman spectra of the monocrystalline graphene used in the fabricated devices, a) Raman spectra sites and b) Raman spectra at 532 nm intensity laser. It is possible to evaluate the correct patterning since out of the graphene channel there is no graphene signature.

As observed in the Raman spectra, a blue shift occurs, specifically with the G peak shifting to a higher wavenumber. This shift indicates the presence of p-type doping [120]. The p-doping may originate from the fabrication process (PMMA contaminants or photoresist [121]) or from contaminants in the ambient environment that interact with the graphene surface [122]. Furthermore, the Raman spectra confirm that the graphene is predominantly monolayer, although defects are present, as evidenced by the appearance of the D peak. The successful patterning of the graphene is demonstrated by the absence of graphene outside the designated channel region, as seen both in the corresponding images and Raman spectra.

3.4 Graphene technology

The core of all the devices fabricated in this work is the graphene. Given that, in this section the fabrication aspects as well as the selected method and faced constraints will be addressed. Despite the availability of various methods for synthesizing graphene, the fabrication of RF graphene devices predominantly relies on techniques such as chemical vapor deposition (CVD) on metal foils or silicon carbide (SiC) substrates, and mechanical exfoliation via the Scotch tape method. CVD on metal foils is particularly advantageous for producing large-area graphene, with layer thickness controlled by the choice of metal: copper is typically employed for monolayer graphene, while nickel is preferred for multilayer growth. However, a critical limitation of this approach is the required transfer of graphene from the metal

foil to the target substrate. This transfer process, often polymer-assisted, frequently introduces defects and contaminants, leaving residual polymer deposits that can significantly degrade graphene's charge carrier mobility.

CVD growth on SiC substrates offers the advantage of producing planar, two-dimensional graphene directly compatible with top-down lithographic techniques. However, the high cost of SiC substrates is a significant barrier to their widespread adoption for large-area production. Mechanical exfoliation, which involves peeling graphene layers from bulk graphite, can yield high-quality graphene with excellent electronic properties. Nevertheless, the small and irregularly shaped flakes produced by this method limit its scalability for industrial applications.

Considering that processes compatible with large-scale mass production are preferred in the industry, CVD-grown graphene should be favoured over other methods. In this thesis, CVD graphene was used, being the continuous graphene films preferred over graphene flakes. Continuous films are scalable, but they typically contain a higher density of defects compared to graphene flakes. In contrast, graphene flakes offer superior quality but are constrained by their limited size, which poses challenges for scaling up the fabrication process. Notably, the shared use of the CVD furnace for the synthesis of both graphene and carbon nanotubes (CNTs) created significant challenges in achieving high-quality graphene. The co-use of the furnace for CNT production introduced contamination and process variability, complicating the development of pristine graphene films within this shared system.

3.4.1 CVD growth of large-area single-crystal graphene

Large-area single-crystal graphene was synthesized on copper foil using catalyst-assisted growth within a low-pressure chemical vapor deposition (CVD) system (CVD First Nano, EasyTube 3000). The selection of copper foil was strategic due to its low carbon solubility, which facilitates the formation of a homogeneous monolayer graphene film. However, the system's configuration restricts the maximum sample size to 10 cm x 10 cm. To achieve continuous graphene films, a 25 μm thick copper foil (Alfa Aesar, purity 99.99%) underwent a pre-treatment process in an ultrasonic bath containing a solution of 10 ml 0.5 M of FeCl_3 , 10 ml of 37% HCl, and 280 ml of DI H_2O for approximately one minute. This step was crucial for reducing the microscopic roughness of the copper surface. Following this, the foil was subjected to oxidation on air in a hot plate at 250 $^{\circ}\text{C}$ for 30 minutes before being placed in a graphite box, which served to enhance the growth process by shielding the sample from contaminants potentially introduced by reactions with the quartz reactor walls. The combination of copper foil and graphite box was placed into the EasyTube 3000 furnace for processing. The copper foil was then annealed at 1040 $^{\circ}\text{C}$

under a pressure of 4.5 Torr during 30 minutes within the quartz tube furnace. For the graphene growth process, a gas mixture of 300 sccm Ar, 100 sccm H₂, and 1.5 sccm CH₄ was introduced into the quartz chamber, maintaining the 4.5 Torr pressure for 60 minutes. After growth, the samples were cooled using 500 sccm Ar until the furnace reached ambient temperature. As documented in the literature, rapid cooling is essential to minimize defects within the graphene lattice, thereby preserving its high crystalline quality [123]. The general process of the graphene continuous film fabrication could be seen in the Figure 53.

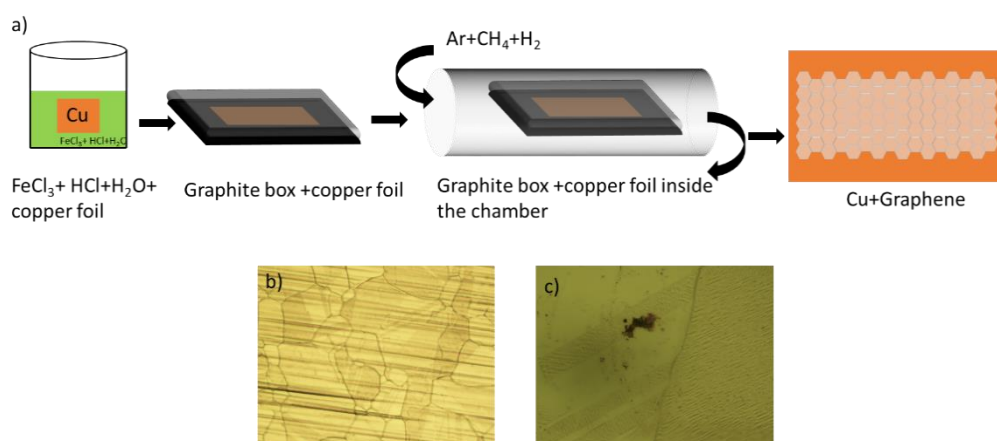


Figure 53 – a) General fabrication process of the single layer graphene continuous film. b) graphene on copper and c) carbon chunk on top of the graphene arising from contaminations in the graphene furnace.

3.4.2 Graphene flakes

Despite the overall quality of continuous CVD-grown graphene films, a significant drawback is the presence of grain boundaries, which occur when graphene flakes coalesce during growth. These grain boundaries introduce defects in the film due to the presence of dangling bonds that can anchor contaminants, acting as scattering centres and thereby degrading critical properties of graphene, such as its carrier mobility—an essential parameter in electronic applications. Increasing the grain size in large-area continuous graphene films reduces the number of grain boundaries per unit area, which in turn enhances the mobility of graphene, leading to improved performance in graphene-based devices.

To mitigate the detrimental effects of grain boundaries, the growth of isolated CVD graphene flakes is essential, since it facilitates the selection of the best regions visually. Achieving high-quality graphene flakes requires precise control over the flow rates of the gases involved in the growth process. This thesis presents a comprehensive study on the CVD growth of graphene flakes, with a particular focus on the influence of key gas flow parameters, including hydrogen (H₂), methane (CH₄), and argon (Ar).

Hydrogen plays a crucial role in graphene growth, functioning as a co-catalyst that aids in the activation of the metal surface, thereby promoting the growth of graphene. Additionally, H_2 significantly influences the shape of the graphene grains by etching weak carbon-carbon bonds, thus controlling the morphology of the graphene flakes [124]. The flow of methane is equally critical, as it serves as the carbon source, directly impacting the growth rate and quality of the graphene layer.

To optimize the growth process, a confinement graphite box containing an oxygen source (sapphire wafer) was employed to manage the native oxide layer prior to annealing. This approach was aimed at controlling nucleation on the copper surface. The copper foil was deliberately oxidized on a hot plate within a cleanroom environment to incorporate additional oxygen into the process, which helped decrease the nucleation sites on the copper foil. The presence of oxidized copper suppresses carbon nucleation, reducing the likelihood of nucleation and increasing the spacing between nucleation sites. This allows for greater lateral growth of graphene flakes and permits the use of a higher methane flow rate during growth, without saturating the copper foil with unwanted graphene satellites.

Substrate preparation

The roughness of the copper foil significantly influences the quality of the transferred graphene. To prevent the collapse of graphene following transfer, it is essential to minimize the roughness of the copper surface, as any irregularities on the copper foil will be transferred to the PMMA and subsequently to the final substrate. To achieve a smooth copper surface, chemical polishing was performed using an ultrasonic bath. The polishing solution consisted of 10 ml of 0.5 M $FeCl_3$, 10 ml of 37% HCl, and 280 ml of deionized (DI) water. After polishing, the samples were rinsed thoroughly with DI water and then dried using a nitrogen (N_2) gun. After the polishing process, the copper foils were oxidized in a hot plate set at 250°C for 30 minutes within an ISO 5 class cleanroom environment. This oxidation step is crucial for preparing the copper surface for subsequent graphene transfer.

Catalyst oxidation state control

To maintain the oxidation state of the copper foil during the graphene growth process, a sapphire disk (3-inch Al_2O_3 wafer) was positioned over the substrate using two graphite spacers as shown in Figure 54. This setup was then placed inside a graphite box. The graphite box serves multiple critical functions: it traps gases released from both the sapphire disk and the oxidized copper foil during growth, thereby increasing the local oxygen concentration. Additionally, the graphite box protects the sample from contamination by SiO_2 particles that may be released from the walls of the quartz tube.

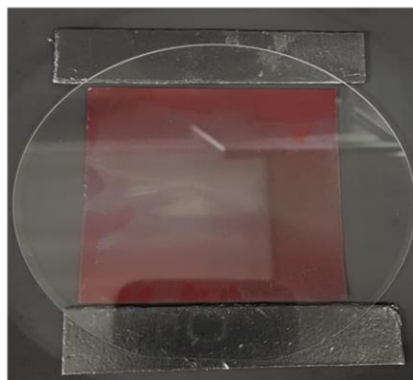


Figure 54 – Picture of the sapphire mounted over the treated copper foil.

Graphene flakes growth

The graphene flakes were grown using the same CVD system (EasyTube 3000 from First Nano) as employed for continuous graphene films, with the setup previously described: copper substrates with a graphene cap enclosed in a graphite box. The growth procedure involved the following steps:

1. Heating: The reactor and the sample are heated to 1040 °C with an Ar flow (which lasts around 30 minutes).
2. Annealing: The sample was annealed in an argon (Ar) atmosphere to prepare the surface for graphene deposition for 30 minutes.
3. Graphene Deposition: Graphene growth was achieved by introducing 1.5 sccm of methane (CH_4) and 350 sccm of hydrogen (H_2) into the reactor for 90 minutes at a pressure of 4.5 Torr.

Both the annealing and growth processes were conducted at the same pressure. After the growth process, the graphene flakes were characterized using optical microscopy. This was performed immediately after cooling the sample to room temperature. The presence of graphene was confirmed by observing areas of the oxidized copper where graphene was absent. The oxidized copper was clearly visible in regions without graphene. The workflow of graphene flakes growth can be seen in Figure 55.

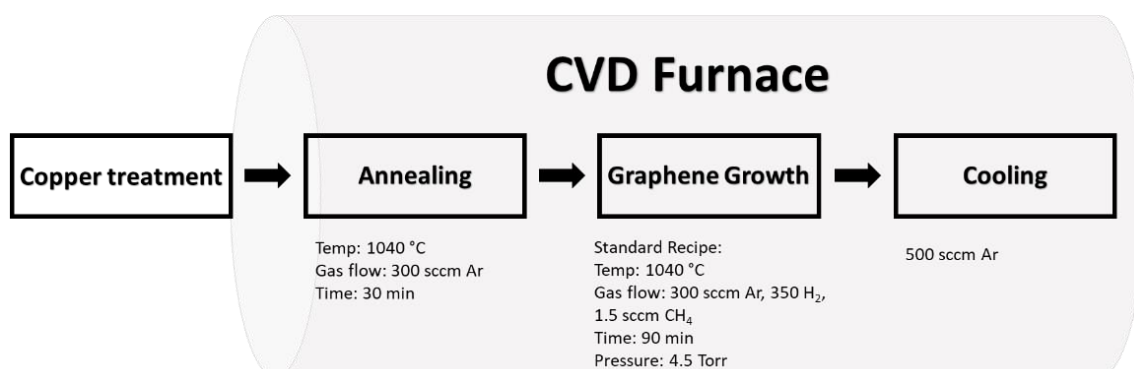


Figure 55 – General scheme of the graphene flake growth.

3.4.2.1 Control of graphene flake morphology through gas flow ratios

Tuning the flow rates of H_2 , CH_4 and Ar gases during the CVD process allows for precise control over the nucleation density, size, and shape of the graphene flakes.

Effect of the H_2 in the flake's growth

In the chemical vapor deposition (CVD) process, H_2 serves both as a surface activator and an etchant. By adjusting the flow rate of H_2 , it is possible to influence the shape of the graphene crystals. Specifically, the ratio of H_2 to CH_4 plays a critical role in determining the morphology of the graphene flakes. A low H_2/CH_4 ratio tends to produce dendritic shapes, whereas a high H_2/CH_4 ratio results in hexagonal and circular shapes, with excess H_2 facilitating the formation of these latter geometries. Hexagonal graphene flakes are particularly desirable because they help to minimize grain boundaries when forming continuous graphene films. Studies have shown that continuous films composed of randomly oriented, irregularly shaped, micrometer-sized flakes tend to have a high density of grain boundaries, which can adversely affect the film's properties. In contrast, hexagonal flakes with zigzag edges are beneficial for the oriented growth of continuous graphene films, reducing the number of grain boundaries and thereby enhancing the film's properties [125].

In a study conducted to investigate these effects, the flow rates of argon and methane were kept constant at 300 sccm and 1.5 sccm, respectively, while the H_2 flow rate was varied from 50 sccm to 300 sccm at a pressure of 4.5 Torr, with a growth duration of 90 minutes. The results, as depicted in the Figure 56, align with existing literature: increasing the H_2 flow leads to a more rounded flake morphology due to the etching of the flake edges by hydrogen.

Challenges were encountered in identifying an optimal graphene recipe for RF device fabrication due to contamination issues from carbon nanotube growth, as the same reactor was used for both processes. This contamination affected the cleanliness of the reactor and complicated the development of a suitable graphene synthesis protocol.

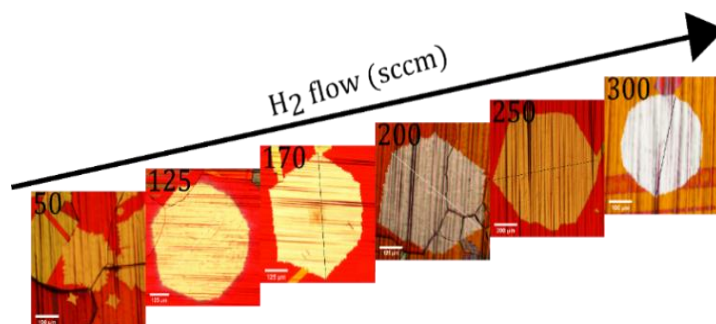


Figure 56 – Evolution of graphene flakes with the increasing of Hydrogen (H_2) flow.

Effect of the CH_4 in the flake's growth

Methane plays a crucial role in the growth of graphene as the carbon source in this molecule is essential for graphene formation. To conduct this, an H_2 flow rate of 350 sccm and 300 sccm of Ar at 4.5 Torr were used, with varying CH_4 flow rates to study their effects (from 1.5 sccm to 2.95 sccm). Consequently, the methane flow rate was found to directly influence the size of the graphene flakes. However, simply increasing the CH_4 flow is not always advantageous. Elevated CH_4 levels can lead to an increased number of nucleation sites, resulting in a higher density of coalesced graphene flakes. This coalescence often leads to multilayer graphene forming at the centers of flakes and an increase in grain boundaries.

While increasing the CH_4 flow enhances the availability of reactive carbon species, which promotes the growth of larger graphene flakes, it also introduces complications. Specifically, excessive methane can lead to a higher nucleation density, which may cause more flakes to merge. This merging can create multilayer regions and increase the overall number of grain boundaries within the graphene film. The evolution of the graphene flakes with the increase of CH_4 can be seen in Figure 57.

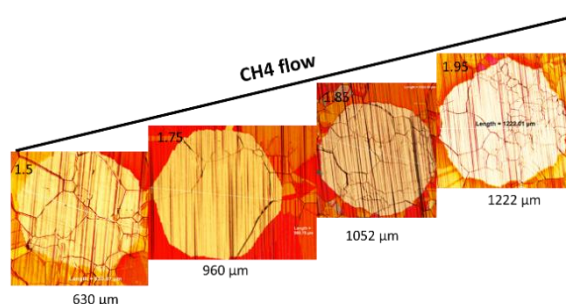


Figure 57 – Evolution of graphene flakes with the increasing of methane (CH_4) flow.

The use of the same reactor for both graphene and carbon nanotube synthesis posed significant challenges in optimizing graphene recipes for RF device fabrication.

3.4.2.2 Samples characterization

Following the growth process, the graphene flakes were characterized using optical microscopy (OM), scanning electron microscopy (SEM), and Raman spectroscopy. Initially, the samples were protected from oxidation by the graphene layer. To reveal the underlying copper in areas without graphene, the samples were oxidized in air by placing them on a hot plate at 180°C for approximately 5 minutes. This oxidation treatment highlighted the regions where graphene flakes were absent, facilitating the identification of graphene coverage as shown in Figure 58.

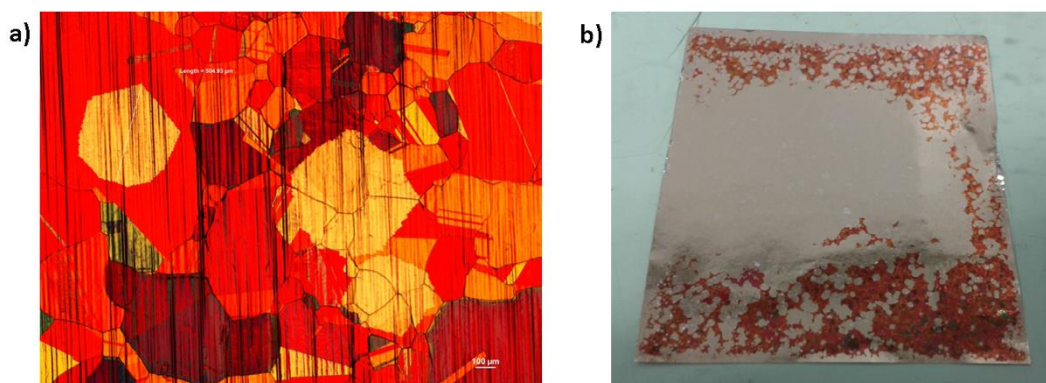


Figure 58 – Images of graphene flakes on copper after the oxidation on a hotplate a) optical microscope and b) photograph of the copper foil.

Optical microscopy and scanning electron microscopy

Optical microscopy was used to observe and evaluate the size and shape of the graphene flakes immediately after the oxidation process. For a more detailed analysis, scanning electron microscopy (SEM) was performed using a FEI Nova NanoSEM 650 at electron beam voltages of 5 kV and 10 kV. This provided high-resolution images to assess the morphology and quality of the graphene flakes

Raman spectroscopy

Raman spectroscopy was employed to further characterize the graphene flakes. The measurements were conducted using a Witec Alpha300R confocal Raman microscope equipped with a 532 nm frequency-doubled Nd laser. Raman spectroscopy is a powerful technique for assessing graphene quality and properties. While elastic light scattering (Rayleigh spectroscopy) can determine the number of graphene layers, it is primarily effective for exfoliated samples on optimized substrates and does not provide additional structural or electronic information [126]. In contrast, Raman spectroscopy is versatile and applicable to all types of graphene samples, providing comprehensive insights into graphene quality, including the presence of contaminants, doping, and defects, and enabling effective comparison among different samples [127]. In graphene, the Raman spectrum exhibits characteristic peaks due to phonon energy shifts caused by laser excitation. For a 532 nm laser excitation, these peaks are primarily the G peak (at approximately 1580 cm^{-1}), the 2D peak (at around 2690 cm^{-1}), and the D peak (at approximately 1350 cm^{-1}) [128]. The positions of these peaks can vary depending on the wavelength of the excitation laser used. The different Raman graphene peaks can be seen in Figure 59.

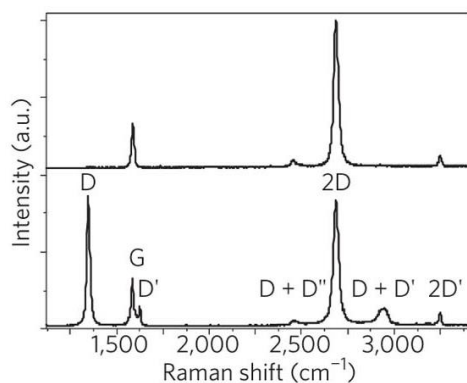


Figure 59 – Different Raman graphene peaks for a laser excitation of 532 nm[129].

The Raman spectrum of single-layer graphene differs slightly from that of multilayer graphene due to interactions between the graphene layers. Specifically, the 2D peak in single-layer graphene is narrower and sharper compared to that in multilayer graphene [130]. Additionally, the G peak exhibits a red shift with an increase in the number of graphene layers [131]. The number of graphene layers can be derived from the ratio of the peak intensities, I_{2D}/I_G , as well as from the position and shape of the peaks as shown in Figure 60 and Figure 62. The I_{2D}/I_G ratio is particularly useful for distinguishing between monolayer and multilayer graphene. The G and 2D peaks' positions and shapes provide additional information on the layer number and the presence of any defects or strain in the graphene structure [130].

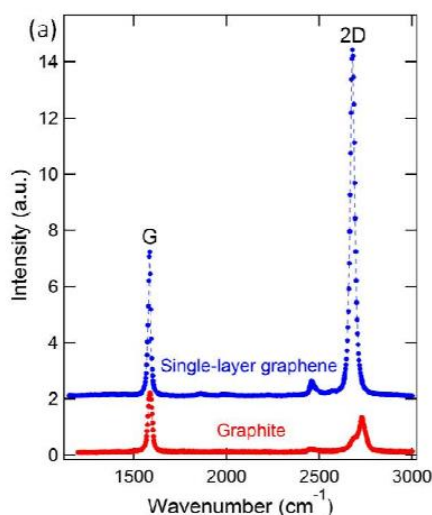


Figure 60 – Raman spectra of single layer graphene and bulk graphite at a 532 nm laser [132].

The position and intensity of the G band can be influenced by various factors such as doping and strain within the graphene. Consequently, shifts in the G band position can provide valuable information about these aspects of the graphene sample. The intensity of the G band also follows a predictable behaviour that aids in predicting the thickness of the graphene layers as shown in Figure 61.

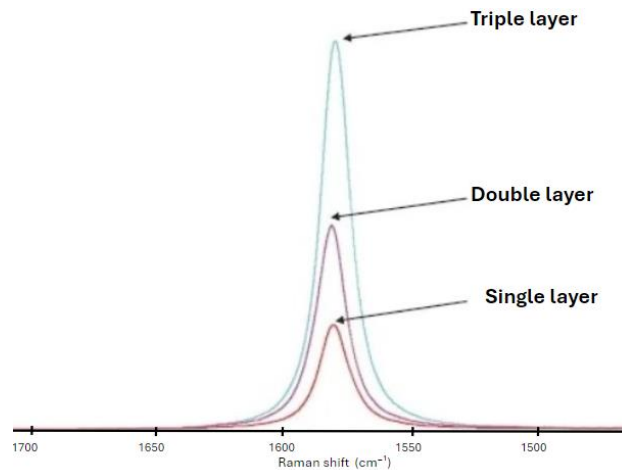


Figure 61 – A linear increase in G band intensity occurs as the number of graphene layers increases, with a 532 nm laser. Adapted from [133].

In addition to the G band, another prominent feature in the Raman spectrum of graphene is the D band, also referred to as the defect band. The D band appears around 1350 cm^{-1} and is indicative of defects within the graphene structure. The intensity of the D band is directly proportional to the level of defects present in the graphene sample. In high-quality graphene or graphite, the D band is typically very weak or absent [133].

This relationship between D band intensity and defect density provides a valuable tool for assessing the quality of graphene, with lower D band intensity signifying fewer defects and higher structural integrity.

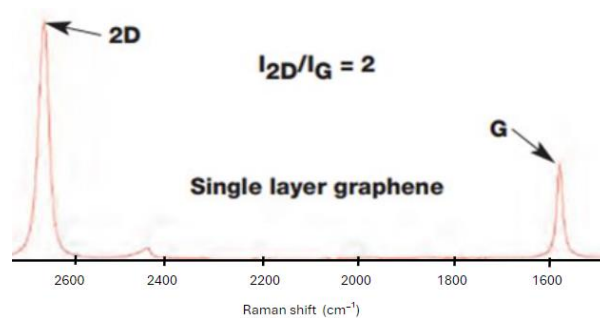


Figure 62 – Relationship between 2D peak and G peak for single layer graphene. Adapted from [133].

The 2D band in the Raman spectrum, which appears around 2690 cm^{-1} , is the second-order peak of the D band and is crucial for characterizing graphene. This band is a strong and consistent feature of the Raman spectrum, even in the absence of the D band. It plays a significant role in determining the number of graphene layers present in a sample. The position and shape of the 2D band are critical indicators; as the number of graphene layers increases, the peak becomes less symmetric due to the

overlapping spectra of the individual layers. The 2D band can be used to distinguish between single-layer and multilayer graphene, with the capability to identify up to four layers. For single-layer graphene, the intensity ratio between the 2D and G peaks (I_{2D}/I_G) is a key parameter. In high-quality graphene, this ratio is typically greater than or equal to 2.

Given these characteristics, Raman spectroscopy is an efficient method for evaluating the quality of graphene. Initially, Raman measurements were conducted immediately after the graphene growth, as shown in Figure 63. Subsequent Raman analyses were performed after transferring the graphene to the final substrate, which is critical for nanodevice fabrication.

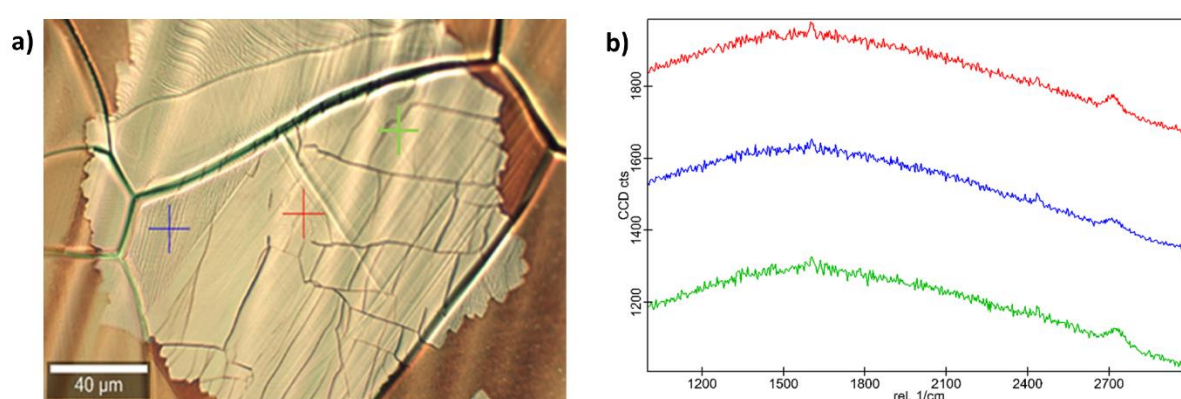


Figure 63 – a) Raman spectra a graphene flake on a copper foil and b) Raman spectra at 532 nm of the flake.

3.4.3 Graphene growth contaminants

As previously mentioned, the cleanroom facilities at INL are shared among various research projects. The Easytube system used for graphene growth was also used for carbon nanotube synthesis. The nanotube growth process used much higher flow rates of methane and ethylene (not used in graphene) compared to those required for graphene growth, which led to significant contamination of the reactor chamber and associated plumbing. Despite thorough cleaning efforts, large carbon deposits remained in the system. The high sensitivity of graphene growth parameters to environmental conditions made it challenging to achieve optimal results with this level of contamination. The residual carbon from nanotube synthesis (shown in Figure 64) adversely affected the ability to finely tune the growth conditions necessary for producing high-quality graphene. Consequently, the contamination impeded the development of graphene suitable for state-of-the-art RF devices.

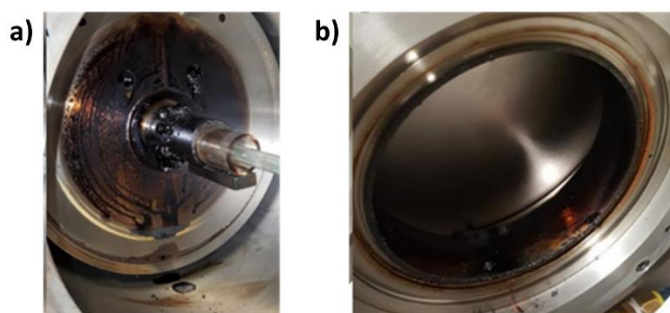


Figure 64 – Contaminated CVD furnace. The black portions are carbon chunks that resulted from CNT growth.

A cleaning protocol involving high-temperature oxidation with oxygen was developed to address contamination within the reactor chamber. However, this method proved insufficient to completely remove all residual carbon deposits from the pipes and chamber. Additionally, manual cleaning efforts were employed to further address contamination, but these measures still did not achieve the desired level of cleanliness.

The persistent contamination compromised the effectiveness of the cleaning procedures and adversely affected the reproducibility of the graphene growth process. As a result, maintaining consistent and high-quality graphene production for RF device applications became challenging.

3.4.4 Graphene transfer

PMMA is the most used polymer for supporting graphene during the transfer process. This polymer has excellent solubility in organic solvents such as acetone and toluene. After PMMA removal, following the graphene transfer to the final substrate, it is common to observe PMMA residues on top of the graphene membrane. Despite these residues, the PMMA transfer method remains the most reliable and widely used for graphene transfer. PMMA acts as a supporting layer to preserve the integrity of the graphene during the wet etching of the copper substrate and provides mechanical stability throughout the transfer process. However, these residues can dope the graphene, potentially degrading its thermal and electrical properties. The graphene carrier's mobility can decrease one order of magnitude after the transfer [134][135]. The graphene transfer is also affected by the appearance of cracks in the membrane as shown in the Figure 65. Several methods have been reported to remove the PMMA from the top of the graphene surface. Hot acetone was used to remove the PMMA, since the temperature enhances the solvent extraction [136]. Other solvents could be used to dissolve PMMA such as anisole, chlorobenzene and chloroform. Despite the PMMA solvents being used to remove the PMMA from the graphene surfaces

it has been agreed by several researchers that PMMA residues cannot be completely removed by the solvent alone [137].

Another approach to reduce the PMMA residues at the graphene's surface is the use of two layers of PMMA. This approach not only improves the cleanliness of the graphene [138] but also reduces the presence of cracks in the graphene membrane [139]. The use of solvents to remove the PMMA does not provide a fully clean surface due to the strong interaction between the polymer and the graphene. To reduce this interaction the degradation of the polymer through irradiation in small fragments have been studied. These fragments are more easily dissolved by the standard solvents of PMMA. A laser cleaning was reported in [140] without introducing defects in the graphene lattice. PMMA degradation can be also achieved thermally [141]. A temperature of 300 °C to 400 °C together with a flow of Ar and H₂ provides satisfactory results decomposing efficiently the PMMA polymer. Increasing the temperature could be beneficial for the PMMA decomposition however the production of amorphous carbon increases. The presence of Ar not only removes PMMA but also prevents the production of amorphous carbon. The use of a low molecular weight PMMA is also advantageous since it increases its solubility. Other polymers can be used to assist the graphene transfer; however, they are not so well established as the PMMA.

Other approaches could be used in graphene transfer, instead of the use of polymers. Dry transfers could be used to avoid the use of solvents to etch the polymers. Thermal release tape and PDMS have been being used as support materials to transfer graphene in a dry way. After the etching of the metal support layer where graphene was grown, the graphene could be transferred to the final substrate and the support material could be removed by annealing the sample. Despite the non-use of solvents and the consequent formed residues, some residuals could be left in the graphene's surface caused by the support polymer. Other approaches are being developed such as the use of h-BN as the protection layer of the graphene [142] or gold as the support layer [143]. More detailed information about the removing of the contaminants from transferred CVD graphene could be found in [144].

In this thesis, the formulation detailed in [121] was used. This method remains the most reliable and widely adopted for wet PMMA-assisted graphene transfer. The PMMA formulation used consists of a 2:1 ratio of PMMA-550K to PMMA-15K in anisole at a 3% weight concentration. This mixture is known for its optimal mechanical strength and flexibility during transfer while minimizing contamination. The copper foil is spin-coated with this solution to achieve a 150 nm thickness at 3000 rpm using an automatic coater, then left to dry overnight at room temperature. After coating, the graphene on the copper foil is subjected to O₂ plasma etching to facilitate the complete dissolution of the copper by the etchant, given graphene's impermeable nature. The graphene is then immersed in a 0.5M FeCl₃ solution for an average

of 3 hours, depending on the sample size. Once the copper is fully etched (as verified optically), the graphene is scooped into a container of water to remove excess iron chloride. A Si/SiO₂ substrate is used as a transfer tool.

To remove metal precipitants, the sample is transferred to a 2% HCl solution for 30 minutes. Following this, the graphene is rinsed in deionized water to eliminate residual chemicals. The graphene, along with the PMMA, is then transferred to the final substrate, which has been pre-treated with HDMS in a vapor prime oven to enhance adhesion. The substrate is left to dry vertically at room temperature overnight. Before proceeding to device fabrication, the PMMA is removed with acetone. Ensuring a clean graphene transfer is crucial, as any residues or cracks in the membrane can significantly impact the thermal and electrical properties of the graphene, affecting its performance in electronic applications.

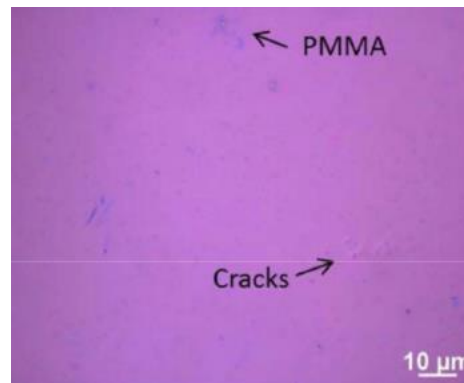


Figure 65 – Graphene cracks and PMMA residues [145].

3.5 Discussion

In this chapter, the design and fabrication of the devices were discussed. Techniques reported in the literature to address some of the challenges associated with graphene transistors were reviewed. Regarding this, we could evidence the difficulty to grow a high-k oxide on top of the graphene due to the lack of reactive sites for ALD deposition, which is mandatory to achieve high performance in RF devices, since they are essential to mitigate tunnelling effects, especially in devices with thin oxide layers, for example. To enable the ALD, the pre-functionalization of graphene's surface with metal or amorphous carbon would need to be performed. Alternatively, h-BN could be used as dielectric due to its good compatibility with graphene. Concerning RF devices, the high contact resistance that results from the contact between a metal and the 2D material is also a drawback of graphene devices. Nonetheless, this can be reduced by contacting graphene on the edges [146] or with the appropriate choice of the contact

metal and technique. To improve the RF performance, several techniques could be used like the use of physical gates to increase the $f_{\max}$ of the transistors [49] to the implementation of complex gate structures designed to reduce parasitic and access resistances [63]. Self-aligned structures are also being developed to minimize access resistance, thereby improving the RF performance of GFETs [53], which is a critical parameter for achieving high-performance graphene RF oscillators. Preserving the graphene lattice is essential for achieving high carrier mobilities. Consequently, polymer-free graphene transfer methods and the development of back-gated devices, avoiding the deposition of dielectrics on top of graphene, are being explored to enhance GFET performance [60], [64]. Graphene RF transistors have demonstrated the potential to achieve cutoff frequencies in the hundreds of GHz, as shown in [62]. Taking this into account and considering the constraints of the INL fabrication process, two fabrication approaches were presented: a buried bottom-gate graphene device fabrication process without surface planarization, using a critical point dryer to achieve crack-free graphene transfer, and a surface planarization technique employing ion milling prior to graphene transfer. As discussed in this thesis, fabricating such devices presents significant challenges; however, a repeatable process was established since it was effective in the fabrication of other types of graphene devices beyond the scope of this thesis.

Regarding the graphene material itself, the growth process and the PMMA-assisted transfer method were also detailed. While this polymer-assisted transfer introduces some residuals on the graphene surface, they are not expected to significantly affect device performance, given the dimensions of the graphene FET channels. Both fabrication approaches yielded satisfactory results, although limitations were identified in the production of graphene flakes, particularly in terms of yield and the additional steps required for their fabrication.

Contamination from carbon nanotubes, coupled with the complexity of fine-tuning growth parameters, impeded the development of an optimized graphene synthesis protocol. Consequently, producing large graphene flakes, preferred for high-yield RF performance, was challenging within the constraints of the experimental setup.

Despite these challenges, continuous graphene films were ultimately employed for RF device fabrication. The scalability of continuous films is a critical factor for large-scale production, which is essential to meeting industrial demands. The need for a scalable solution outweighed the challenges of optimizing conditions for large-flake production. Therefore, continuous graphene films were chosen to ensure both scalability and consistent RF performance, which are vital for industrial feasibility.

4 OSCILLATOR DEVELOPMENT

For the effective fabrication of a graphene device, it is crucial to develop a model, as it helps to predict the device behaviour quickly, supporting in the fabrication process or providing output predictions when direct measurements are not possible. In this chapter, the model of the fabricated transistors is presented, along with the performance assessment of the previously fabricated devices.

4.1 Transistor modelling

Device models are classified into physical and empirical types. Physical models, essential during initial development, offer insights into device behaviour based on carrier transport parameters. Physical models for GFETs, while essential for early device development, are complex and impractical for circuit-level modelling due to their computational demands. Empirical models, however, offer a balance between accuracy and efficiency and are suitable for use in electronic design automation (EDA) tools. These models, which describe current–voltage characteristics, often assume the same carrier mobility and contact resistance for both electrons and holes, disregarding substrate effects. However, due to differences in mobility and contact resistance for different carriers, particularly in short-channel devices, these models fail to account for asymmetries in GFET transfer characteristics. Recent models have incorporated aspects from short-channel Si MOSFET models to better predict I-V characteristics but still assume identical mobility for electrons and holes. Current models lack validation through RF methods, such as power spectrum analysis, which is crucial for improving model accuracy. The selected model for this thesis is reported in [147] and presents a semi-empirical analytical model for GFETs based on a square-root charge–voltage relation. The model is derived for single-layer zero-bandgap graphene and accommodates different electron and hole mobility values. It captures the symmetry of intrinsic GFETs, similar to models for HEMTs and MOSFETs. Additionally, the model accounts for asymmetric contact resistance for n- and p-type channels. It features few fitting parameters, with parameter extraction using S-parameters (RF) and DC data. From DC domain it is possible to extract the $I_{DS} - V_{DS}$ curve, g_m and graphene mobility. From the RF domain it is possible to complement the DC measurements, by allowing extraction of all the capacitances between interfaces, contact resistance and inductance, and determine the FOMs of the transistor directly from the measurement.

In this chapter, the model described before [147] will be implemented and the fabricated transistor that was designed based on that model will be characterized (RF + DC) and modelled.

Additionally, the design of a ring oscillator will be explored, and the key aspects for optimizing its performance will be addressed.

4.1.1 *Semi-empirical analytical model*

Following the model presented before and proposed in [147], which is compatible with EDA tools and allows for both DC and RF analysis, a good fit with measured values was achieved. In short, this model is advantageous because it accounts for the differences between hole and electron conduction in the GFET, which is significant since the metal/graphene contacts vary depending on the carrier type. With only a few fitting parameters, the parameter extraction can be performed using both S-parameters and DC data, making the model effective for DC and RF analysis. The model is divided into extrinsic and intrinsic components. At low frequencies, or in DC conditions, the extrinsic part can be ignored. However, at high frequencies, the parasitic elements included in the extrinsic part of the model must be considered. According to this work, in [147], the data extracted from the measurements of the fabricated devices can be used to construct this model effectively. In the following explanation of parameter extraction, intrinsic and voltage nodes are differentiated by using lowercase letters for intrinsic nodes and uppercase letters for extrinsic nodes (e.g., intrinsic gate-source voltage (V_{gs}) and extrinsic gate-source voltage (V_{GS})). There are two operational domains of the device that need to be extracted and analyzed to construct the model effectively: the DC and RF domains. From the DC domain, the I_{DS} - V_{GS} curve, transconductance (g_m), and graphene mobility are extracted. From the RF domain, in addition to the DC measurements, all capacitances between interfaces, contact resistance, and inductance are extracted as figures of merit (FOMs) from the measurements. This comprehensive extraction of parameters from both domains is crucial for accurately modelling the GFET. In the Figure 66 it is possible to observe the large signal model equivalent circuit, evidencing the parameters that should be extracted to correct model the fabricated devices.

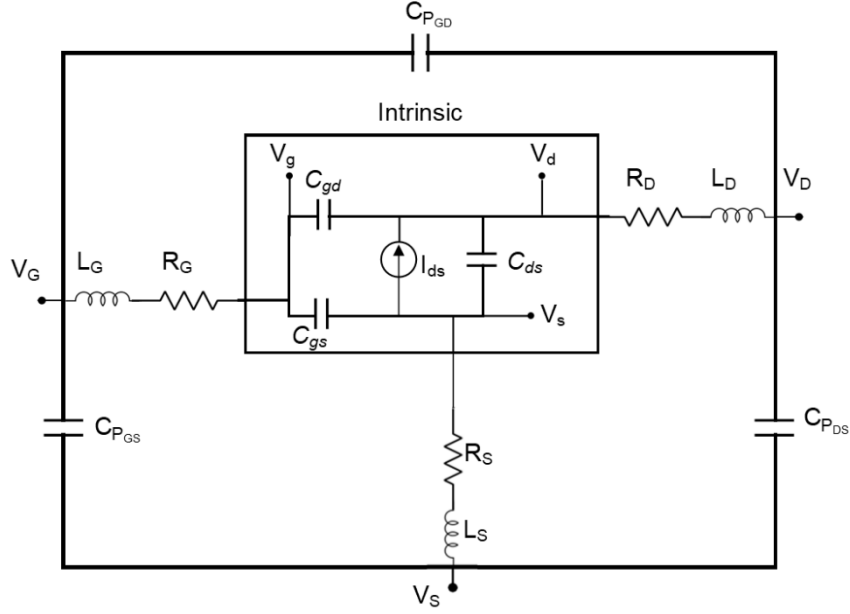


Figure 66 – Large-signal model equivalent circuit. C_{PGS} , C_{PDS} , L_G , L_D , and L_S are parasitic capacitance values and inductances. R_G is the gate resistance, and R_S and R_D are the source and drain resistances including contact and access resistances. Adapted from [147].

In this model [147], it is assumed the presence of the different carrier types, electrons and holes. As a result, there are four distinct scenarios for the type of the majority carriers in the GFET channel, only electrons, holes and electrons and only holes, depicted in Figure 67. The expressions shown in after the figure were derived using the drift-diffusion model.

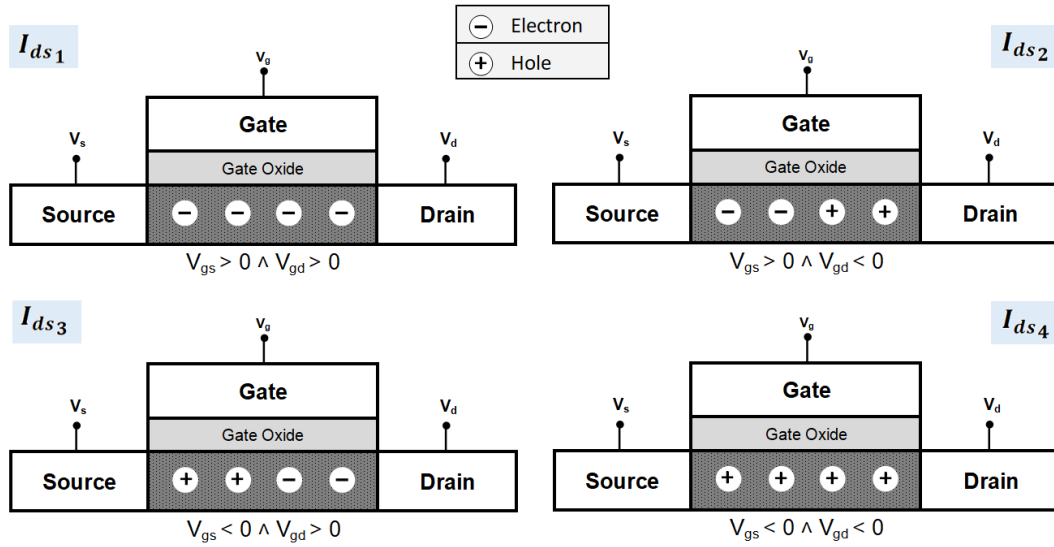


Figure 67 – Major carrier type in the graphene channel at different bias voltages.

$$I_{ds1} = \frac{\mu_e V_0 Q_0}{\sqrt[m]{1 + \left(\frac{\mu_e |V_{gs} - V_{gd}|}{L \bar{v}_{sat}} \right)^m}} \frac{W}{L} f(\bar{V}_{gs}, \bar{V}_{gd}) \quad (6)$$

$$I_{ds2} = \frac{\mu_e V_0 Q_0}{\sqrt[m]{1 + \left(\frac{\mu_e |V_{gs} - V_{gd}|}{L \bar{v}_{sat}} \right)^m}} \frac{W}{L} f(\bar{V}_{gs}, 0) + \frac{\mu_h V_0 Q_0}{\sqrt[m]{1 + \left(\frac{\mu_h |V_{gs} - V_{gd}|}{L \bar{v}_{sat}} \right)^m}} \frac{W}{L} f(0, \bar{V}_{gd}) \quad (7)$$

$$I_{ds3} = \frac{\mu_h V_0 Q_0}{\sqrt[m]{1 + \left(\frac{\mu_h |V_{gs} - V_{gd}|}{L \bar{v}_{sat}} \right)^m}} \frac{W}{L} f(\bar{V}_{gs}, 0) + \frac{\mu_e V_0 Q_0}{\sqrt[m]{1 + \left(\frac{\mu_e |V_{gs} - V_{gd}|}{L \bar{v}_{sat}} \right)^m}} \frac{W}{L} f(0, \bar{V}_{gd}) \quad (8)$$

$$I_{ds4} = \frac{\mu_h V_0 Q_0}{\sqrt[m]{1 + \left(\frac{\mu_h |V_{gs} - V_{gd}|}{L \bar{v}_{sat}} \right)^m}} \frac{W}{L} f(\bar{V}_{gs}, \bar{V}_{gd}) \quad (9)$$

$$f(x, y) = x\sqrt{1+x^2} - y\sqrt{1+y^2} + \ln\left(\frac{\sqrt{1+x^2}+x}{\sqrt{1+y^2}+y}\right) \quad (10)$$

$$\bar{v}_{sat} = \frac{v_F \beta}{\sqrt[4]{n_o^2 + \left(\frac{C(V_{gs} + V_{gd})}{2q}\right)^2}} \quad (11)$$

$$\bar{V}_{gs} = \frac{V_{gs}}{V_o} \quad (12) \quad \bar{V}_{gd} = \frac{V_{gd}}{V_o} \quad (13)$$

$$V_o = \frac{Q_o}{C} \quad (14) \quad C = \frac{C_{gd} + C_{gs}}{WL} \quad (15)$$

$$Q_o = qn_o \quad (16)$$

where μ_e and μ_h are electron and hole mobility. n_o is the residual carrier density due to disorder and thermal excitation, C is the gate capacitance per area, W and L are the channel width and length, q is the electron charge, β relates the phonon wavelength of the dominant scattering phonon and m is a fitting

parameter. These functions can be merged by using the operator $\Theta(x)$, i.e., using the combination of the step functions where the variables are V_{gs} and V_{gd} . Given that, the single I_{ds} and $\Theta(x)$ equations are:

$$I_{ds} = I_{ds1} \Theta(V_{gs}) \Theta(V_{gd}) + I_{ds2} \Theta(V_{gs}) \Theta(-V_{gd}) + I_{ds3} \Theta(-V_{gs}) \Theta(V_{gd}) + I_{ds4} \Theta(-V_{gs}) \Theta(-V_{gd}) \quad (17)$$

$$\Theta(x) = \frac{1 + \tanh(V_1 x)}{2} \quad (18)$$

where V_1 is a fitting parameter. The V_o parameter is introduced to add the unintentional charging effect in the channel at low V_{ds} , ($V_{gs} = V_{gs} - V_o$ and $V_{ds} = V_{ds} - V_o$).

Despite the dielectric thickness being less than 10 nm in that work [147], the authors of that model did not include quantum capacitance. Although critical, for simplicity, it was omitted because quantum capacitance appears in series with the geometric capacitance, and typically the smallest capacitance dominates. (the geometric capacitance).

As previously mentioned, the contact resistance varies based on the type of carrier within the channel. To account for this, the model uses a series resistance that depends on the carrier type to the contact resistance. Additionally, the contact resistance at both the source and drain is assumed to be identical, as it is influenced by the channel width rather than the contact area [147]. Consequently, the contact resistance is given by the following equation:

$$R_s = R_d = R_o + R_{ext}(V_{gs}, V_{gd}) \quad (19)$$

$$R_{ext}(x, y) = R_{ext_o} \frac{1 + \tanh(V_2 x)}{2} \frac{1 + \tanh(V_2 y)}{2} \quad (20)$$

where R_o is the resistance when $V_{gs} < 0$ and $V_{gd} < 0$, R_{ext_o} is the resistance added to account for the difference in the resistance due to different majority carriers, and V_2 is a fitting parameter.

For the extraction of the extrinsic parameters (L_s , L_g , L_D , C_{PGS} , C_{PDS} , and R_g), excluding R_s and R_D , the S-parameters of the de-embedding structures were used. A more detailed explanation of this approach can be shown below in the section 4.1.3. The R_s and R_D parameters aim to account for variations in contact resistance depending on the carrier type and can be obtained from DC measurements of $I_{DS} - V_{GS}$ curves at low drain voltages. This approach is necessary because, at low drain voltages, Equation 6 and 9, can simplify the intrinsic and extrinsic drain-source resistance to the equations presented in Table 3.

Table 3- Equations of intrinsic and extrinsic drain-source resistances

		Holes	Electron
Intrinsic	$R_{ds} = \frac{V_{ds}}{I_{ds}}$	$\frac{1}{\alpha_h} \sqrt{1 + \left(\frac{V_{GS}}{V_0}\right)^2}$	$\frac{1}{\alpha_e} \sqrt{1 + \left(\frac{V_{GS}}{V_0}\right)^2}$
Extrinsic	$R_{DS} = \frac{V_{DS}}{I_{DS}} = R_s + R_D + R_{ds}$	$2R_o + \frac{\alpha_h}{\sqrt{1 + \left(\frac{V_{GS}}{V_0}\right)^2}}$	$2R_o + 2R_{ext_o} \frac{\alpha_e}{\sqrt{1 + \left(\frac{V_{GS}}{V_0}\right)^2}}$
	$\alpha_{e,h} = \frac{L}{W_{\mu_{e,h}} Q_0}$		

By fitting the aforementioned equations (in Table 3) to model the R_{DS} profile, one can determine the values of R_s , R_D , (R_o and R_{ext_o}), V_0 , and $\alpha_{h,e}$. Extracting intrinsic capacitances involves measuring the device S-parameters when biased at the Dirac point (C_{gd} and C_{ds}). This specific bias point is crucial because, under these conditions, the g_m is equal to 0, and the parasitic parameters can be extracted following the de-embedding process in (section 4.1.3.) and the small-signal model shown in Figure 68, the following parameters can be obtained:

$$C_{gd} = \frac{Imag[-Y_{12}]}{jw} \quad (21)$$

$$C_{gs} = \frac{Imag[Y_{11} + Y_{12}]}{jw} \quad (22)$$

$$C_{ds} = \frac{Imag[Y_{22} + Y_{12}]}{w} \quad (23)$$

And the remaining parameters are calculated as follows:

$$C = \frac{C_{gs} + C_{gd}}{LW} \quad (24)$$

$$Q_o = CV_o \quad (25)$$

$$\mu_{e,h} = \frac{L}{W\alpha_{e,h}Q_o} \quad (26)$$

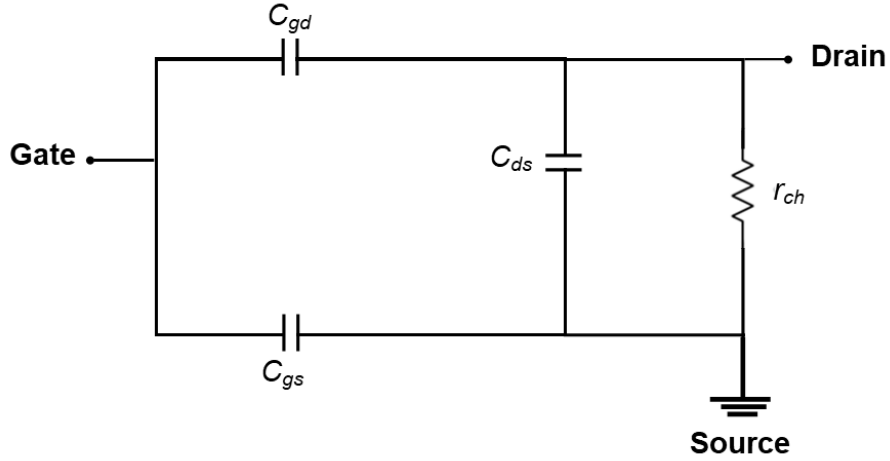


Figure 68 – Small-signal model after de-embedding the parasitic elements at $V_{GS} = V_{Dirac}$. Adapted from [147].

4.1.3 Transistor de-embedding

For RF measurements, a more complex setup is required. The device must be set at an operating point using a DC voltage, necessitating the use of a bias tee (Figure 71). The bias tee serves to combine the DC and RF signals. The output of the bias tee, carrying both RF and DC components, is then connected to the gate and drain terminals to bias the GFET and enabling the RF measurements. The S-parameters were acquired using a Vector Network Analyzer (VNA). The general matrix of the S-parameters is as follows:

$$\begin{bmatrix} b_1 \\ b_2 \end{bmatrix} = \begin{bmatrix} S_{11} & S_{12} \\ S_{21} & S_{22} \end{bmatrix} \cdot \begin{bmatrix} a_1 \\ a_2 \end{bmatrix} \quad (27)$$

where a is the input signal, b is the output signal, S_{11} is the input port voltage reflection coefficient, S_{12} is the reverse voltage gain, S_{21} is the forward voltage gain, and S_{22} is the output port voltage reflection coefficient.

The S-parameters are valuable for extracting the H-parameters (such as f_T), as well as the admittance parameters (Y) and impedance parameters (Z). These parameters are crucial for determining the device's capacitances, resistances, and inductances. It is important to note that $Y = Z^{-1}$.

The admittance parameters (Y) can be obtained from the S-parameters using the following relationships:

$$Y_{11} = \frac{(1 - S_{11})(1 + S_{22}) + S_{12}S_{21}}{(1 + S_{11})(1 + S_{22}) - S_{12}S_{21}} Y_0 \quad (28)$$

$$Y_{12} = \frac{-2S_{12}}{(1 + S_{11})(1 + S_{22}) - S_{12}S_{21}} Y_0 \quad (29)$$

$$Y_{21} = \frac{-2S_{21}}{(1 + S_{11})(1 + S_{22}) - S_{12}S_{21}} Y_0 \quad (30)$$

$$Y_{22} = \frac{(1 + S_{11})(1 - S_{22}) + S_{12}S_{21}}{(1 + S_{11})(1 + S_{22}) - S_{12}S_{21}} Y_0 \quad (31)$$

where Y_0 and Z_0 are the port impedance that typically $Z_0 = 50$ ohm. The two-port system equivalent circuit from the Y-parameters and Z-parameters is shown in Figure 69.

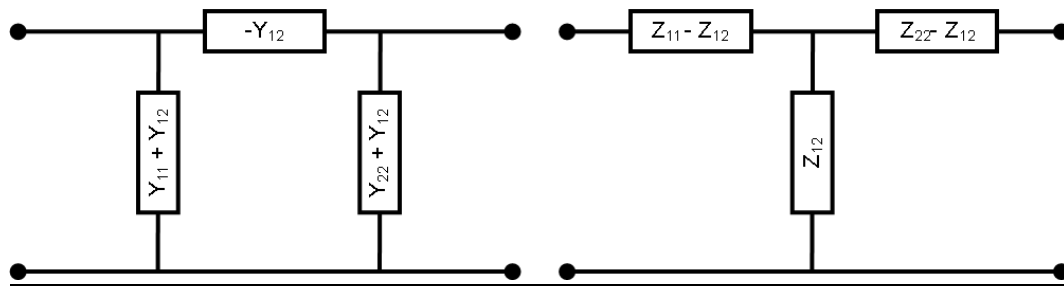


Figure 69 – Two-port system equivalent circuit from the Y-parameters (left) and Z-parameters (right).

As previously described, it is possible to extract the intrinsic characteristics of a device by de-embedding it. For that purpose, open and short structures should be measured to perform an open-short de-embedding. The figure of the complete device, along with the open and short structures, can be seen in Figure 70.

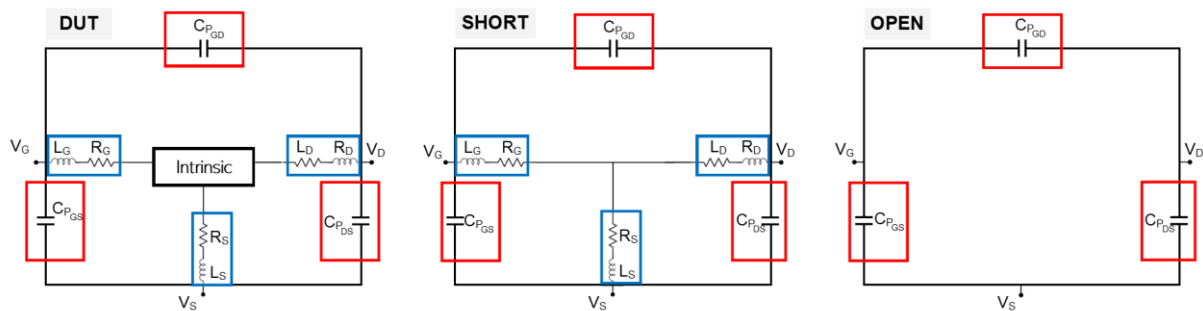


Figure 70 – De-embedding equivalent circuits. Device under test (left), Short (center) and Open (right).

Comparing the 2 previous figures (Figure 69 and Figure 70) and knowing that the $Y_C = j\omega C$, the following equations can be extracted:

$$C_{P_{GD}} = \frac{\text{Imag}[-Y_{O_{12}}]}{\omega} \quad (32)$$

$$C_{P_{GS}} = \frac{\text{Imag}[Y_{O_{11}} + Y_{O_{12}}]}{\omega} \quad (33)$$

$$C_{P_{DS}} = \frac{\text{Imag}[Y_{O_{12}} + Y_{O_{22}}]}{\omega} \quad (34)$$

where Y_O are the Y-parameters of the open structure of the de-embedding.

From the short circuit and knowing the Y_O and Y_S (Y-parameters of the short structure) it is possible to extract the Z parameters of the blue structure and knowing that the impedance of a resistor in series with an inductor is $Z_{RL} = R + j\omega L$, the following equations can be extracted:

$$R_G = \text{Real}[Z_{SO_{11}} - Z_{SO_{12}}] \quad (35)$$

$$R_D = \text{Real}[Z_{SO_{22}} - Z_{SO_{12}}] \quad (36)$$

$$R_S = \text{Real}[Z_{SO_{12}}] \quad (37)$$

$$L_G = \frac{\text{Imag}[Z_{SO_{11}} - Z_{SO_{12}}]}{\omega} \quad (38)$$

$$L_D = \frac{\text{Imag}[Z_{SO_{22}} - Z_{SO_{12}}]}{\omega} \quad (39)$$

$$L_S = \frac{\text{Imag}[Z_{SO_{12}}]}{\omega} \quad (40)$$

To de-embed the final structure, the following formula could be used [147].

$$Y_{intrinsic} = \frac{1}{\frac{1}{Y_{DUT} - Y_O} - \frac{1}{Y_S - Y_O}} \quad (41)$$

4.1.4 Extraction of g_m and graphene mobility from graphene transistors

Since it is important to extract the graphene properties to conclude about the graphene quality, the graphene mobility and transconductance (important parameters used to compare the performance of DC

transistors) can be extracted after the I_{DS} - V_{GS} measurements. The transconductance can be extracted by applying a numerical derivative using the following formula:

$$g_m[i] = \frac{I_{DS}[i+1] - I_{DS}[i]}{V_{GS}[i+1] - V_{GS}[i]} \quad (42)$$

The mobility of the graphene in the field-effect transistor can be extracted by:

$$\mu = \frac{L|g_m|}{WC_gV_{DS}} \quad (43)$$

where L and W are the channel length and width and C_g is the gate capacitance per area. Despite this method is used for simplicity, it underestimates the graphene mobility since it does not consider the contact resistance of the graphene and the ungated regions. To more accurately extract graphene mobility, Hall measurements should be conducted [147].

4.2 Transistor performance assessment

In this section, the performance of the previously fabricated devices, as described in section 3.3, will be evaluated. The analysis will begin with the extraction of the figures of merit. It is noteworthy that improvements in the fabrication processes, as highlighted earlier, have resulted in enhanced RF performance. Specifically, the devices detailed in Section 3.3.3, fabricated with a gate oxide thickness of 5 nm, demonstrated superior performance compared to those presented in Section 3.3.1 and 3.3.2. However, the devices discussed in Section 3.3.1 were not fully characterized, as the de-embedding structures did not achieve the expected performance.

4.2.1 Transistor figures of merit extraction

As previously reported in this work, and as agreed by the academic community, the key figures of merit (FOM) for GFETs are the cutoff frequency (f_T) and the maximum oscillation frequency (f_{max}). These FOMs are crucial for evaluating the performance of transistors in practical applications, whether in DC or RF circuitry. In brief, the cutoff frequency (f_T) is the frequency at which the magnitude of the small-signal current gain is unity ($H_{21} = 0 \text{ dB}$). Regarding the S-parameters, H_{21} can be expressed as:

$$H_{21} = \frac{-2S_{21}}{(1 - S_{11})(1 + S_{22}) + S_{12}S_{21}} \quad (44)$$

To predict the f_T , as shown before, the generally used expression is:

$$f_T = \frac{g_m}{2\pi [(C_{gs} + C_{gd})(1 + (R_d + R_s)g_{ds}) + C_{gd}g_m(R_d + R_s) + C_{pg}]} \quad (45)$$

The f_{max} is described as the frequency at the maximum gain (Mason's Gain (U)), Maximum Available Gain (MAG) and Maximum Stable Gain (MSG), or simply U/MAG/MSG, becomes unitary (U/MAG/MSG = 0 dB). This gain should satisfy some conditions to be calculated [148]. To extract the f_T and f_{max} from the S-params, the first thing to evaluate is the stability factor, extracted from the expression:

$$k = \frac{1 + |S_{11}S_{22} - S_{12}S_{21}|^2 - |S_{11}|^2 - |S_{22}|^2}{2|S_{12}||S_{21}|} \equiv \text{Stability Factor} \quad (46)$$

If all k's are less than one ($k < 1$ for all frequencies), the U/MAG/MSG corresponds to Mason's Gain (U), and it can be calculated using the following expression:

$$U = \frac{\left| \frac{S_{21}}{S_{12}} - 1 \right|^2}{2k \left| \frac{S_{21}}{S_{12}} \right| - 2 \operatorname{Real} \left[\frac{S_{21}}{S_{12}} \right]} \equiv \text{Mason's Gain} \quad (47)$$

If all k's are not less than one, the k should be evaluated for ever frequency. If $k < 1$, the U/MAG/MSG corresponds to Maximum Stable Gain (MSG) and can be calculated using the following expression:

$$MSG = \frac{|S_{21}|}{|S_{12}|} \equiv \text{Maximum Stable Gain} \quad (48)$$

If $k > 1$, the U/MAG/MSG corresponds to Maximum Available Gain (MAG) and can be calculated using the following expression:

$$MAG = MSG \cdot \left(k - \sqrt{k^2 - 1} \right) \equiv \text{Maximum Available Gain} \quad (49)$$

The general equation of f_{max} , as shown before, is:

$$f_{max} = \frac{f_T}{2\sqrt{g_{ds}(R_g + R_s) + 2\pi f_T R_g C_{gd}}} \quad (50)$$

The extraction of the figure of merit (FOM) for graphene field-effect transistors (GFETs) requires the experimental setup illustrated in Figure 71. This setup incorporates two bias tees to separate direct current (DC) and radio frequency (RF) signals, enabling the simultaneous application of a DC bias voltage and an RF signal to the device. A DC power supply is employed to provide the necessary gate and drain bias voltages, thereby biasing the GFET into the desired operational region. A vector network analyser (VNA) is used to generate and measure high-frequency RF signals, allowing for the determination of the device's scattering parameters (S-parameters), which are critical for the calculation of the transistor's FOM. Additionally, a control computer interface is employed to regulate the gate's DC voltage and to facilitate the extraction and analysis of the S-parameters.

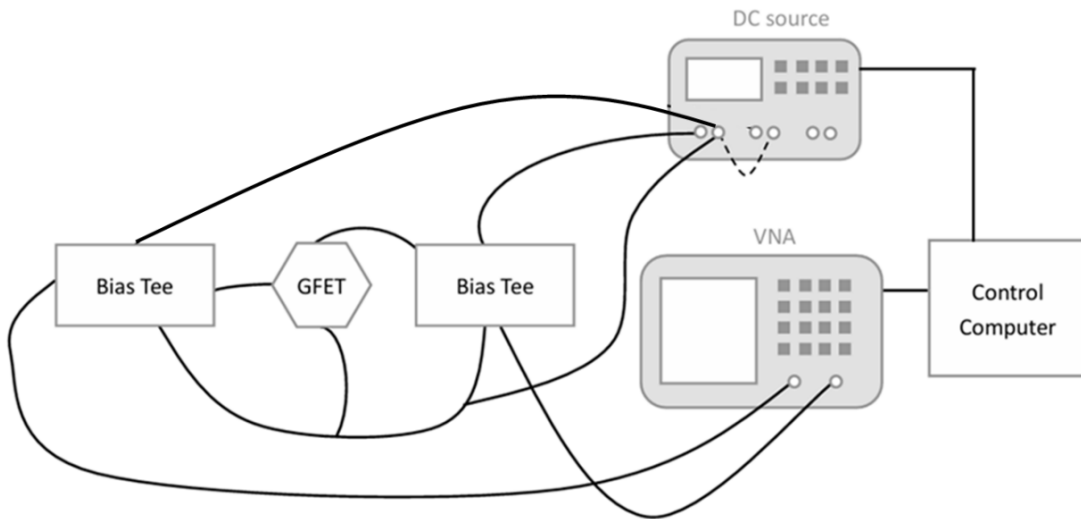


Figure 71 – Measurement setup used to extract the FOMs of the GFETs.

4.2.2 Bottom-gate graphene device fabrication process without surface planarization (with CPD)

To evaluate the performance of the devices fabricated using the CPD method (fabricated in section 3.3.1), extrinsic RF characterization was performed. Intrinsic RF characterization could not be performed due to limitations in the fabrication process since the de-embedding structures did not exhibit the expected performance. Not only RF measurements, but also the DC measurements, were performed with the V_{gs} vs I_{ds} and the respectively g_m is shown in Figure 72. Figure 73 illustrates the RF measurements, the S-parameters (a) and the extracted FOMs (b). In this device, an extrinsic cut-off

frequency (f_r) of 5.5 GHz and a maximum oscillation frequency (f_{max}) of 0.7 GHz, measured at a V_{DS} of 3 V and a V_{GS} of 5 V were demonstrated. These values were obtained without employing a global back gate, suggesting a high level of p-doping in the graphene membrane. This fabrication method achieved a high yield of operational devices, with approximately 70% exhibiting RF functionality.

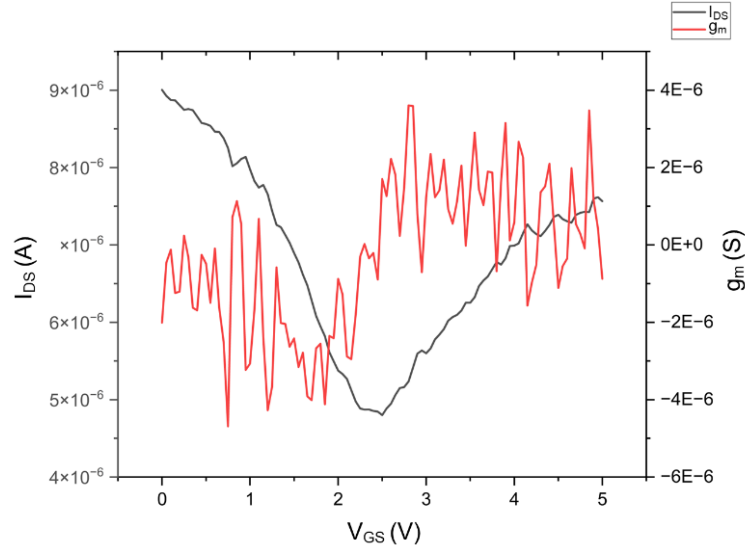


Figure 72 – V_{GS} vs I_{DS} and g_m characteristic curves of a device with $W = 39 \mu\text{m}$ and $L = 1.100 \mu\text{m}$ (0.95 μm of gate channel and 0.075 μm of drain/gate and source/gate overlap) measured at a V_{DS} of 100 mV.

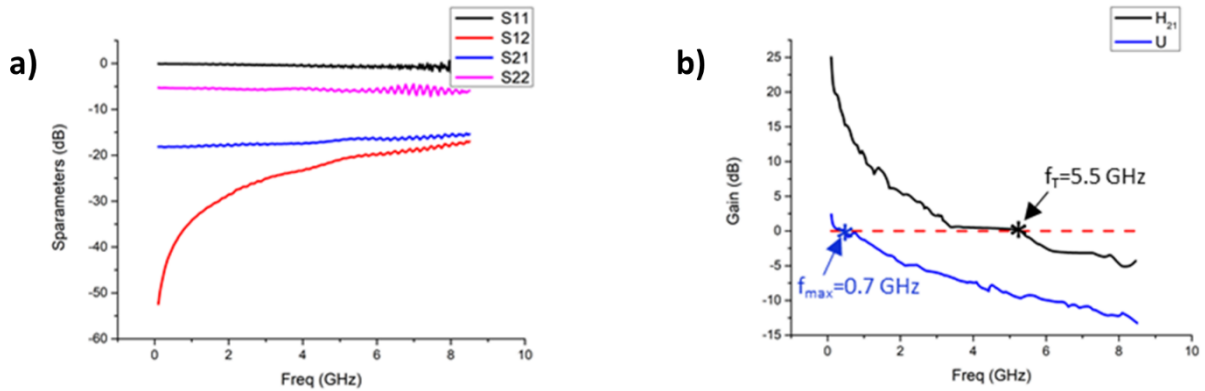


Figure 73 – a) S-parameters of a device with $W = 39 \mu\text{m}$ and $L = 1.100 \mu\text{m}$ and a L_a (access length) of 85 nm and respectively f_r and f_{max} . b). c) RF measurement scheme used to measure the devices.

4.2.3 Planar buried bottom-gate topology

The performance of the transistors fabricated through the buried process (presented in section 3.3.2) was analysed. In the first process ($t_{ox} = 10$ nm of alumina) a yield around 100% was achieved. To assess the success of the planar buried bottom-gate topology against the process without surface

planarization, a similar transistor with the same dimensions and access resistance was characterized. The measured extrinsic f_T and f_{max} were 6 GHz and 3 GHz, respectively, using the standard graphene/metal contact pattern (without additional patterning). These results can be explained by the quality of the graphene after the transfer onto a flat surface. The observed increase in f_{max} should be attributed to the decrease in source/drain resistance. This reduction is due to a lower contact resistance in top drain/source contacts compared to back drain/source contacts, with the top contacts exhibiting approximately ten times lower resistance [149]. Since f_{max} evaluates the transmitted power, a higher f_{max} indicates that the transistor is not only suitable for high-frequency digital electronics but also for high-frequency analogue applications, such as RF amplifiers [150]. The evolution of f_T and f_{max} with the increasing of L_a , which leads to an increase in the R_a as it can be observed in Figure 74 was also conducted. The RF performance decreases with the increase of L_a (access resistance), which was expected according to equation 2 and 3, given the increase in R_{sd} which leads to a decrease in g_m . An interesting finding was the bigger f_{max} around $L_a = 80$ nm, when compared with $L_a = 0$, which could be explained by the trade-off between the decrease in the parasitic capacitance from source/drain capacitance and the increase in the source/drain resistance. Despite the various patterns employed for the graphene/metal contact, no definitive conclusions could be drawn, as none consistently outperformed the others.

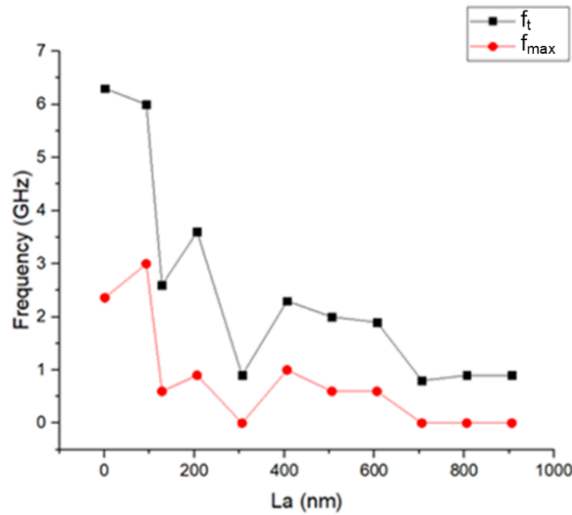


Figure 74 – Evolution of the f_T and f_{max} with the variation on access length.

4.2.4 Planar buried bottom-gate topology improved

Since the previous process yielded favorable results, the performance of the second process (presented in section 3.3.3 with $t_{ox} = 5$ nm) was evaluated. As this process also demonstrated promising

outcomes, the DC characteristics were assessed initially. The data derived from these measurements (transfer curves) are illustrated in the following figure for a device with $L = 1.101 \mu\text{m}$ and $W = 33.82 \mu\text{m}$.

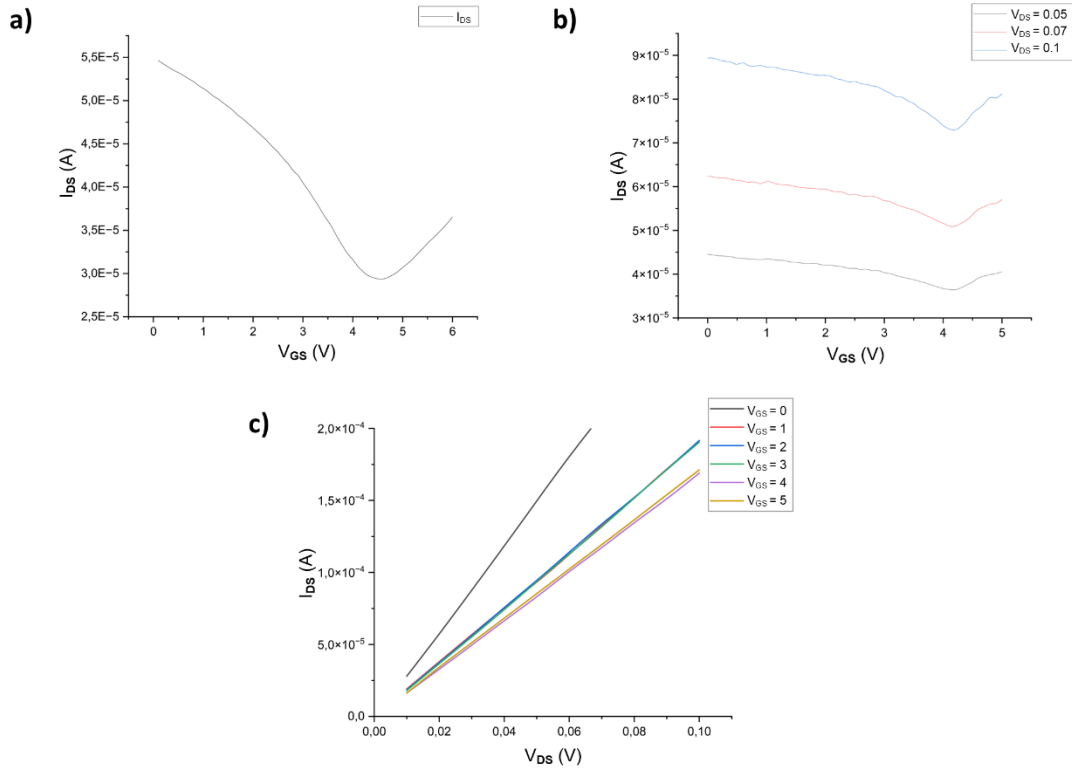


Figure 75 – Transfer curves of a device with $L = 1.102 \mu\text{m}$ and $W = 33.82 \mu\text{m}$. a) V_{GS} vs I_{DS} curve for a V_{DS} of 10 mV and b) Curves of V_{GS} vs I_{DS} for different V_{DS} and c) curves of V_{DS} vs I_{DS} for different V_{GS} .

The Dirac point of the device is observed at approximately 4.5 V, indicating p-type doping, as previously suggested during the Raman evaluation. The characteristics of the GFET will be discussed in the modelling section; however, the extracted mobility is around $900 \text{ cm}^2/\text{V}\cdot\text{s}^{-1}$ for holes and $1100 \text{ cm}^2/\text{V}\cdot\text{s}^{-1}$ for electrons, which is sufficient for a ring oscillator to oscillate, given the similar mobilities in [37]. Nevertheless, due to the high p-doping context, a back gate is necessary to shift the Dirac point closer to 0 V to ensure that the device operates within an acceptable voltage range. Considering the DC performance of the devices, the RF performance was also evaluated. Notably, de-embedded structures were fabricated to extract both the intrinsic f_T and extrinsic f_{max} , isolating the contributions from parasitic elements external to the device that significantly impact its performance. The open structure consisted of a device similar to the fabricated transistors but without graphene in the channel. The short structure, in contrast, was fabricated with all electrodes connected. Figure 76 shows the RF performance of two distinct devices after the de-embedding, showing the extrinsic and intrinsic performance of the transistors. As concluded earlier, and as expected, the device with a small L_g exhibited a better performance than the one without L_g .

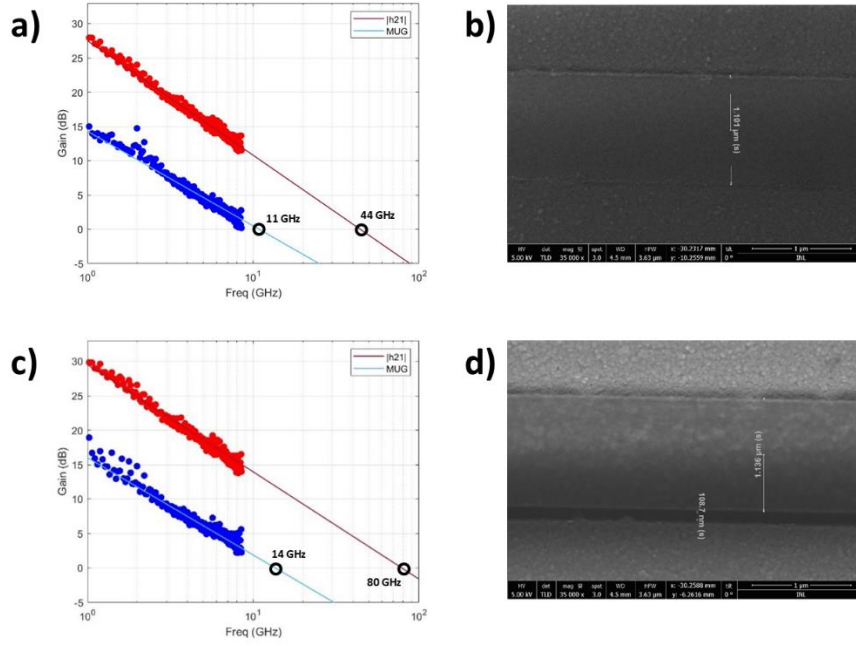


Figure 76 – RF performance of the de-embedded devices. H_{21} and MUG of a device with an $L = 1.101 \mu\text{m}$ a) and c) of a device with a $L = 1.136 \mu\text{m}$ and a L_a of 54.35 nm . b) and d) SEM images of the respective devices showing the measurements of the channel length and access length. Device d) shows a small misalignment in between the drain and gate. The f_{max} and f_r of a) are 11 GHz and 44 GHz respectively and in c) are 14 GHz and 80 GHz respectively.

Based on the results obtained, with a device achieving an intrinsic f_r and f_{max} of 14 GHz and 80 GHz ($W = 33.82 \mu\text{m}$ and $L = 1.101 \mu\text{m}$), it can be concluded that the previously fabricated transistors exhibit significant potential for use in the fabrication of ring oscillators. This is demonstrated by their high f_{max} , which indicates the transistors' ability to provide power gain at high frequencies, thus ensuring signal integrity. Moreover, the observed high f_r suggests that the ring oscillator can achieve very fast switching speeds, further confirming the suitability of these transistors for high-frequency applications.

4.3 Circuit level transistor performance assessment

The previously fabricated devices underwent validation through integration into various circuits to demonstrate their suitability for real-world applications. These circuits covered a range of functionalities, from basic logic operations to more complex nonlinear applications. For instance, simple inverters were implemented to evaluate the devices' switching capabilities and overall performance in digital applications. Additionally, the devices were tested in nonlinear circuits, such as mixers and frequency doublers, which are critical in RF and communication systems. Mixers were employed to analyze the devices' behavior in frequency conversion, assessing their linearity and intermodulation characteristics. Frequency doublers provided insights into harmonic generation and efficiency under nonlinear conditions. These tests helped

characterize the devices under different operating conditions, providing a comprehensive understanding of their potential for practical use.

4.3.1 Transistor integrated to operate as an inverter

The graphene inverters, which serve as the fundamental building blocks for RF graphene oscillators, were fabricated and validated to evaluate their RF performance and suitability for integration. To test the inverter, a square wave with a 1 V amplitude swing centered at 5.7 V (chosen because of the Dirac voltages since V_{Dirac} are far from 0 V) was applied to the inverter's input (V_{in}). The schematic of the inverter is shown in Figure 77 a), while the fabricated device is depicted in Figure 77 b). The inverter was powered by a supply voltage (V_{DD}) of 8 V. For the applied V_{in} , the measured output voltage (V_{out}) was 500 mV, corresponding to an inverter gain (A_v) of 0.5. The output signal is centered at 0 V due to the use of a bias tee, which isolates and recovers the AC component of the output. Figure 77 c) presents the oscilloscope capture, displaying both the input and output signals, further confirming the inverter's operation and performance.

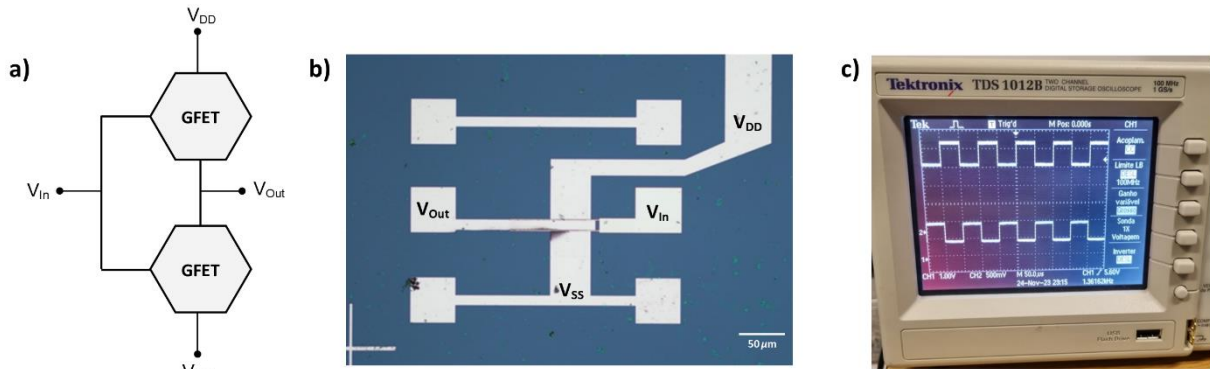


Figure 77 – a) Inverter schematic with GFET. b) Equivalence of the fabricated device with the schematic shown in a) c) Measurement of a graphene inverter with a V_{DD} of 8V showing a V_{out} of 500 mV of amplitude swing (channel 2) for a V_{in} of 1V swing centered in 5.7 V.

Despite the favorable f_T and f_{max} reported earlier, the measured inverter did not exhibit a gain greater than 1 ($A_v = 0.5$), a criterion essential for oscillation according to Barkhausen's stability criterion. This limitation may arise from the selected device or the design of the inverter itself. Efforts were made to measure the fabricated ring oscillator to validate its functionality; however, no output was observed when using the RF probes. To ensure proper operation of the ring oscillators, it is necessary to increase the gain of the inverter. However, due to the high p-doping observed in the fabricated transistors, increasing the supply voltage (V_{DD}) to boost the gain is not a viable solution, given the breakdown field of the materials. In fact, the scaling of electronic circuits typically involves a reduction in the supply voltage

to ensure that the electric field in scaled devices remains below the breakdown field of the material [151]. Therefore, alternative approaches must be considered, as will be discussed in Section 4.5. In the following subsection, some nonlinear blocks, such as a frequency doubler and a mixer, will be analyzed.

4.3.2 Transistor as a non-linear block

Given the RF performance of the transistors, an RF mixer and an RF frequency doubler were implemented to validate their capability to operate at GHz frequencies. To demonstrate the mixer, the device was powered with a V_{DS} of 4 V. Then, a 3.2 GHz 0 dBm signal was combined with a 3 GHz 0 dBm signal through a combiner. This signal was injected in the gate of the device through the help of a bias-tee to isolate the DC from the RF sources. A DC component of 2.5 V was applied to the gate of the device, given the Dirac point of the device.

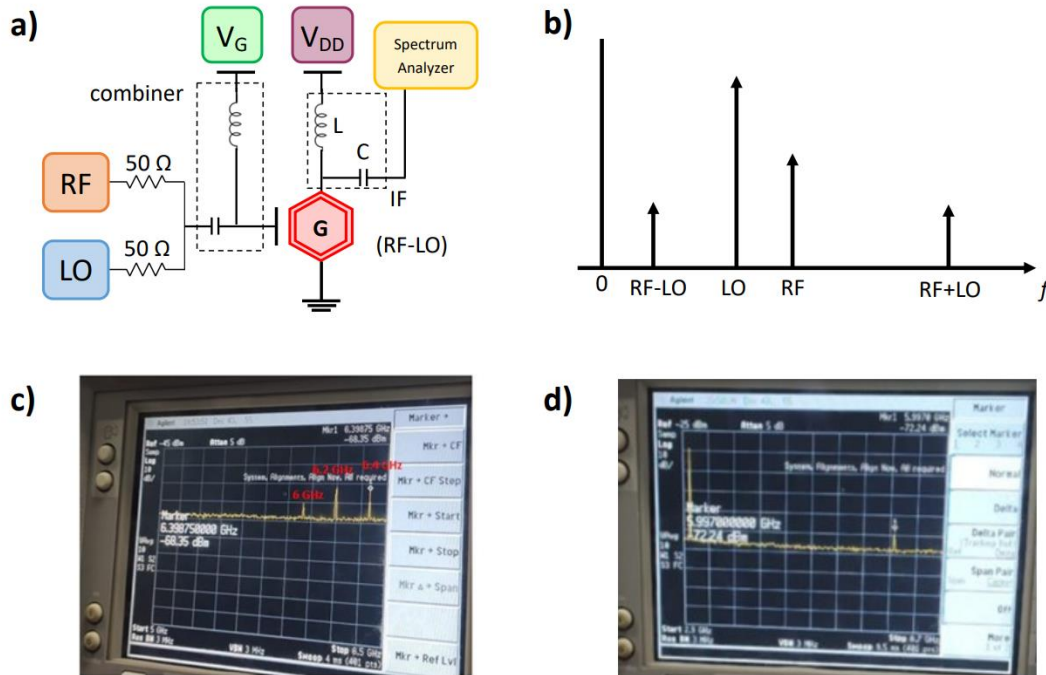


Figure 78 – RF graphene mixer and frequency doubler. a) circuit of the graphene mixer and b) expected output spectrum. c) Measured RF spectrum of the graphene mixer and d) output spectrum of the frequency doubler for an input signal with a frequency of 3 GHz at 0 dBm.

In Figure 78 c) it can be observed that the expected outputs of a mixer were generated and measured from the injected RF signals. These outputs include signals at 6 GHz with a power of -76.3 dBm, 6.2 GHz with a power of -67.2 dBm, and 6.4 GHz with a power of -68.35 dBm. This demonstrates the feasibility of implementing a mixer using the presented design. The measurement of the multiplier used a setup that is similar to the mixer. The difference is that only one RF source was used, and no

combiner was used. The signal was inputted directly into the device's gate with an RF probe, and the resulting signal was measured through the other RF probe. The device was powered with 4 V_{DS} and the gate voltage was 2.5 V. An input of 3 GHz at 0 dBm resulted in a detected signal of 6 GHz at -72.24 dBm as shown in Figure 78 d). In the following section, the transistor model will be extracted, and the simulations of the inverters and ring oscillators will be conducted to predict their behavior. These simulations will provide insights into the necessary improvements for future designs and help determine whether the fabricated device should theoretically oscillate.

4.4 Oscillator design

As mentioned before, the models play a crucial role to predict the performance and the suitability of such technology for specific applications. Given that, and in the context of this work, it is necessary to simulate the ability of the fabrication devices as well as the future improvements to achieve RF oscillators. In this section the oscillator design and optimization will be addressed.

4.4.1 RF transistor model extraction

Leveraging the previously discussed equations establishes the foundation for modelling electronic devices, which is crucial for predicting their behaviour and exploring innovative applications. This section uses empirical data to validate the anticipated performance of a specific device, thereby elucidating the inherent limitations observed in devices fabricated within the scope of this doctoral research.

In this section, both RF and DC measurements were employed to extract the parameters essential for accurate modelling. These measurements provided a comprehensive understanding of the device's behaviour across different frequency domains. However, challenges emerged during the RF measurements at the Dirac point, where transistor failure occurred due to operational constraints. Consequently, the model's validation of RF performance at high frequencies was compromised.

In this context, the modelled device features dimensions of $L = 1.101 \text{ } \mu\text{m}$ and $W = 33.82 \text{ } \mu\text{m}$ (device reported in section 4.2.4). The DC analysis was performed by sweeping the V_{GS} from 0 to 6 V with a V_{DS} of 0.01V. As observed, a good fit was achieved, with the extracted mobility for graphene being $899.56 \text{ cm}^2\text{V}^{-1}\text{s}^{-1}$ for holes and $1124.45 \text{ cm}^2\text{V}^{-1}\text{s}^{-1}$ for electrons. These values align with the transistors reported in [29] for use in ring oscillators. However, the maximum transconductance is approximately 0.01 mS, which is relatively low compared to the values reported in [29]. The comparison between the measured I_{DS} and the simulated I_{DS} demonstrates a strong agreement, indicating that the previously

reported model accurately captures the transistor's behaviour. This level of accuracy suggests that the model is sufficiently robust to predict the performance of other transistors, provided that relevant parameters are appropriately adjusted. Analysing this device under various conditions offers critical insights into its operational thresholds and performance metrics, which are essential for validating theoretical predictions against practical outcome. The Figure 79 illustrates the model's fit to the device, along with the extracted parameters (Table 4), which will be used in subsequent sections to perform the circuit simulations.

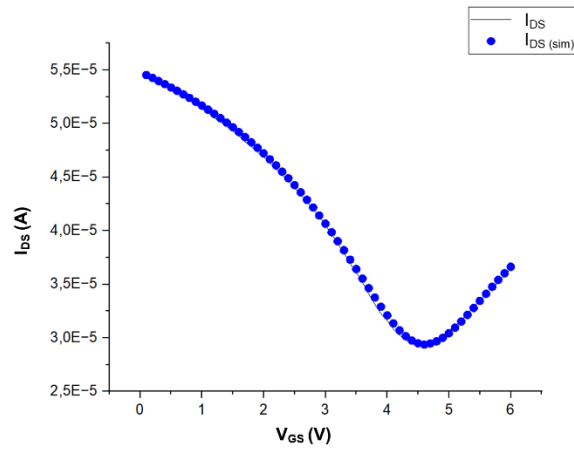


Figure 79 – Simulated vs measured I_{DS} vs V_{GS} of the transistor.

Table 4 - Extracted parameters from the model by using the previous transistor.

W (μm)	L (μm)	t_{ox} (nm)	μ_n ($\text{cm}^2\text{V}^{-1}\text{s}^{-1}$)	μ_p ($\text{cm}^2\text{V}^{-1}\text{s}^{-1}$)
33.82	1.102	5	899.56	1124.45
C_{ox} (fF)	C_{int} (fF)	R_s (Ω)	R_d (Ω)	R_{ext} (Ω)
$22.5e^{-6}$	$45e^{-15}$	$70=(R_D+R_S)/2$	10	20

4.4.2 Inverter design

Like previously reported, the unity element of the ring oscillator is the inverter. With that purpose, a graphene inverter was designed and simulated with the previous model by using a finite element analysis software. To note that all the next simulations were performed using this finite element analysis software. An inverter is created by connecting two GFETs in series, as shown in Figure 77 a). This setup mirrors the configuration of CMOS inverters, where the upper transistor functions like a p-type and the lower one like an n-type. The operating principle of this inverter is that when one transistor is fully conducting, the other should be turned off, or in the case of GFETs, operate near the Dirac point. Due to

a slight variation in V_{DS} , there is a corresponding small difference in the V_{Dirac} of the GFETs, allowing for the construction of an inverter with closely matched GFETs. This arrangement produces a transfer curve with a distinct "W" shape, and an inverter can be effectively implemented by operating the device with V_{in} set between the lowest points of this “W-shaped” curve. To conduct the simulations with more practical values suitable for use in circuits, the Dirac point was adjusted to 0 V. It's important to note that due to the shift in the Dirac voltage (V_{Dirac}) caused by the drain-source voltage (V_{DS}), the inverter's maximum gain is not at 0 V but rather shifted to approximately 1.5 V. The V_{DS} of the inverter is set at 3.3 V. As observed, for an input signal with a peak-to-peak voltage of 1.3 V, the output peak-to-peak voltage is around 0.62 V, which closely matches the values (regarding the inverter's gain) observed in the measured device described Figure 80. It is worth mentioning that some discrepancies between the simulation and the experimental measurements are expected. These differences arise from variations in the modeled devices, which, despite being similar, exhibit differences in graphene quality, this variability is due to the inherent challenges of achieving uniform graphene characteristics across a sample. Additionally, small variations in the fabrication process, such as lithography misalignments or slight changes in channel length or width, can lead to noticeable differences in device behavior, especially at smaller dimensions. The characteristics of the simulated inverter could be seen in the next figure being the maximum inverter's gain (A_{vmax}) of 0.7. Given that gain, and according to Barkhausen's criterion, it is expected that the ring oscillator fabricated with that devices will not oscillate.

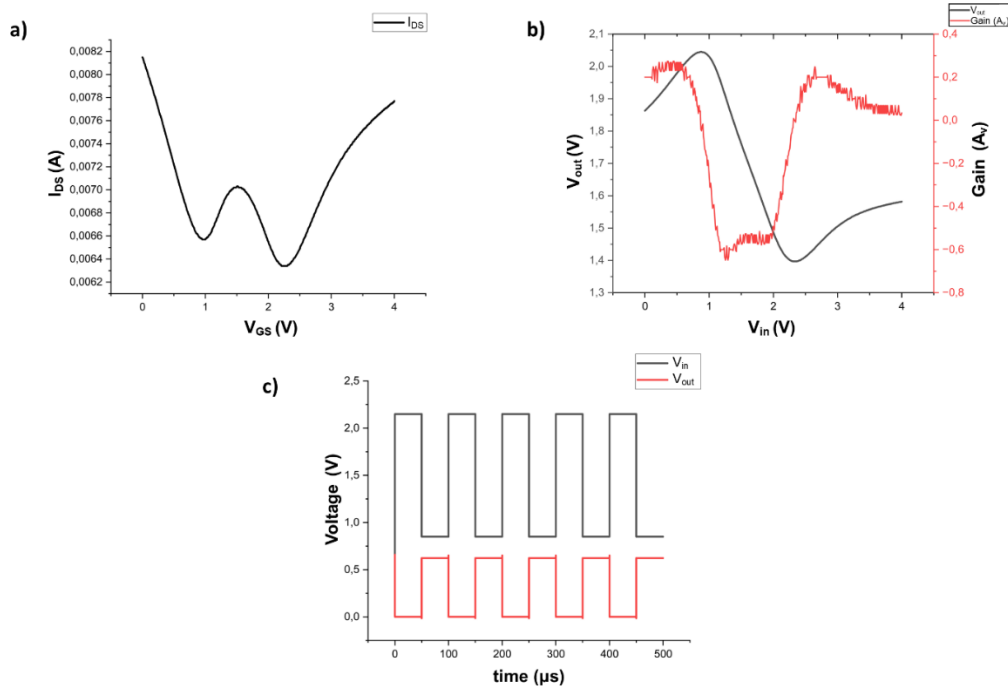


Figure 80 – Simulation of an inverter with the extracted parameters. a) W shape curve of the inverter; b) V_{out} vs V_{in} and Gain of the inverter showing a maximum gain of 0.7 and c) response of the inverter to a 10 kHz square wave.

4.5 Oscillator trimming

As discussed before, given the low gain of the previous devices, maximum gain (A_{vmax}) lower than 1 (0.7), and according to Barkhausen's criteria, it is expected that the device will not oscillate. In the measurements conducted in the previous section, it was not possible to measure all the fabricated devices, due to the time constraints. Due to variations in W/L ratios, L_a , and the different characteristics of the graphene (stemming from the variability in graphene quality across the sample), it is possible that some oscillators may have oscillated. To explore the parameters that should be optimized for developing graphene inverters with A_{vmax} greater than 1, several parameters will be varied, and their influence on the A_{vmax} of the inverter will be analysed.

4.5.1 Reducing R_{ext0} to 10

To investigate the impact of graphene's characteristics on the inverter and achieve a maximum gain (A_{vmax}) greater than 1, thereby satisfying the Barkhausen criterion, various parameter adjustments were performed. Since graphene mobility influences some of the other parameters, R_{ext0} was initially reduced to 10, an achievable as reported in [147]. Since R_{ext0} represents the extrinsic resistance at zero voltage, including contact resistance (the resistance between graphene and metal electrodes) and access resistances, this parameter can be minimized by optimizing graphene-metal contacts or by employing the techniques previously discussed to reduce the access length (L_a). The W-shaped transfer curve and the V_{in} vs. V_{out} characteristics, along with the corresponding maximum gain, are shown in the Figure 81. Although the gain increased, reaching a value of 0.8, it remains insufficient to satisfy the Barkhausen criterion, making this inverter unsuitable for use in a ring oscillator.

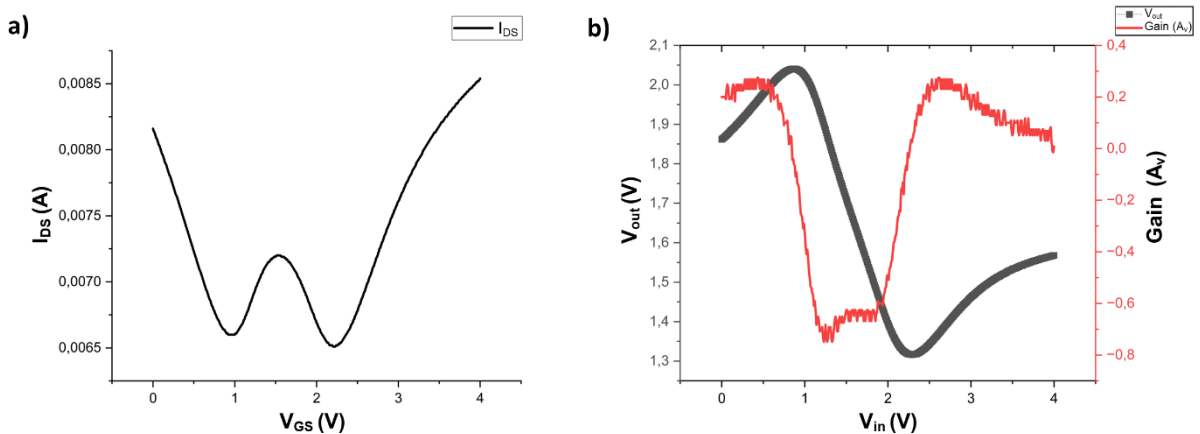


Figure 81 – Simulation of the inverter by reducing the R_{ext0} to 10. a) W shape curve of the inverter; b) V_{out} vs V_{in} and Gain of the inverter showing a maximum gain of 0.8.

4.5.2 Reducing R_o to 40

Since R_o represents the intrinsic channel resistance at the Dirac point, determined by the inherent properties of the graphene material, its value was reduced to 40, a value that is readily achievable as reported in the literature [147]. To achieve this reduction, higher quality graphene (with increased carrier mobility) should be used, or a suitable substrate, such as h-BN, should be employed to minimize the interactions between graphene and the substrate. Additionally, this parameter can be further decreased by using a high-k gate dielectric with low thickness, which enhances carrier control over the channel, thereby reducing R_o . With this reduction, it was possible to achieve a graphene inverter with a maximum gain of 2.6, which is sufficient to satisfy the Barkhausen criterion. The obtained results are presented Figure 82.

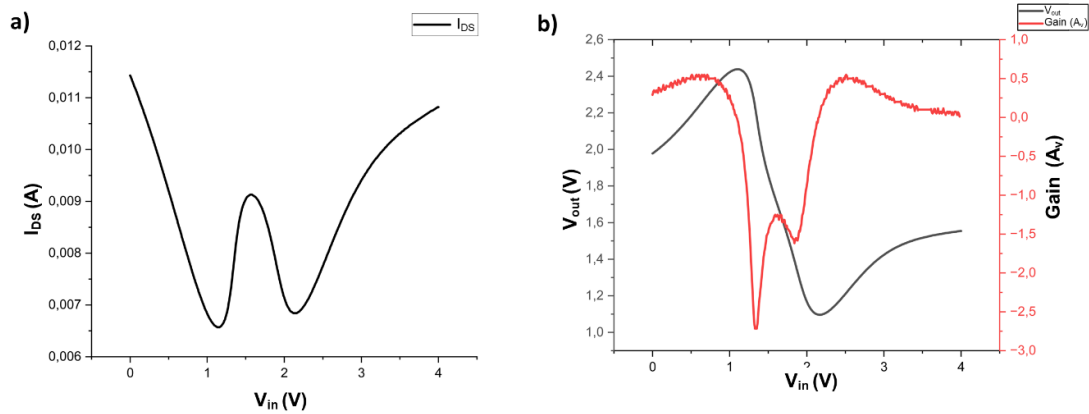


Figure 82 – Simulation of the inverter by reducing the R_o to 40. a) W shape curve of the inverter; b) V_{out} vs V_{in} and Gain of the inverter showing a maximum gain of 2.7.

To further optimize this inverter, the Dirac point of the top GFET (which functions as the p-type FET) was shifted to $V_{Dirac} + 0.3$ V.

4.5.3 Reducing R_{ext} to 10, R_o to 40 and shift V_{Dirac} to $V_{Dirac} + 0.3$ V

The V_{Dirac} of the transistors was initially slightly unmatched, and as discussed earlier, the inverter operates due to the slight difference in V_{DS} and V_{Dirac} between the transistors. To further increase the mismatch, the V_{Dirac} of the top transistor (p-mos) in the previous inverter was shifted to $V_{Dirac} + 0.3$ V. After this adjustment, as observed in the W-shaped curve, the difference between $I_{DS\ max}$ and $I_{DS\ min}$ increased, leading to an improvement in the inverter's gain from 2.6 to nearly 2.7. This kind of shift can be achieved using a dual-gate structure, where one gate specifically adjusts the Dirac point, or by chemical doping. The resulting characteristics of the inverter are shown in Figure 83.

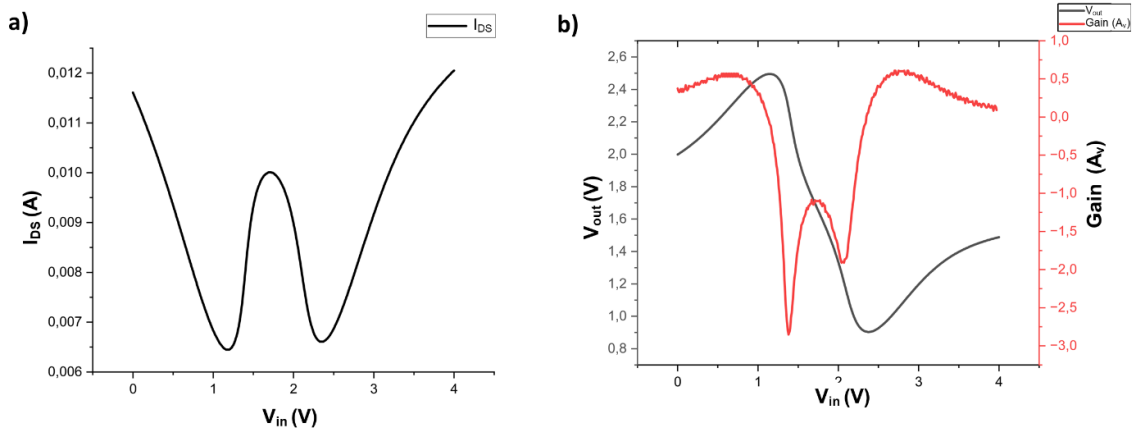


Figure 83 – Simulation of the inverter by reducing shifting the V_{Dirac} to $V_{Dirac}+0.3$. a) W shape curve of the inverter; b) V_{out} vs V_{in} and Gain of the inverter showing a maximum gain of 2.8.

4.5.4 Oscillator frequency tuning

To validate the previously optimized inverter, a square wave with a maximum voltage (V_{max}) of 2.35 V with a minimum voltage (V_{min}) of 1.15 V, and a frequency of 10 kHz was applied to the inverter's input. This input resulted in an output square wave with a V_{max} of 2.5 V and a V_{min} of 0.880 V, thereby confirming the calculated gain of approximately 2.7. The results are illustrated in Figure 84 (a), and the updated parameters for the optimized inverter are listed in Table 5. The suitability of this optimized inverter for use in a ring oscillator was also assessed. According to the Barkhausen criterion, essential for establishing oscillations in a feedback loop, the total loop gain must be equal to or greater than one, and the total phase shift around the loop must be 360 degrees. With a gain of 2.7, the inverter meets these requirements, ensuring that any initial noise or perturbation is sufficiently amplified to initiate and sustain oscillations, while the appropriate phase shift ensures constructive reinforcement of the signal as it traverses the loop. The simulation results validate this, demonstrating that the oscillator operates at 1.08 GHz with a voltage swing of 2.318 V ($V_{max} = 3.263$ V and $V_{min} = 0.945$ V) as seen Figure 84.

Table 5- Parameters used for the inverter and in the ring oscillator simulation.

W (μm)	L (μm)	t_{ox} (nm)	μ_n ($\text{cm}^2 \text{V}^{-1} \text{s}^{-1}$)	μ_p ($\text{cm}^2 \text{V}^{-1} \text{s}^{-1}$)
33.82	1.102	5 nm	899.56	1124.45
C_{ox} (F)	C_{it} (F)	R_o (Ω)	R_s (Ω)	R_{load} (Ω)
$22.5e^{-5}$	$45e^{-15}$	$40 = (R_o + R_s)/2$	20	10

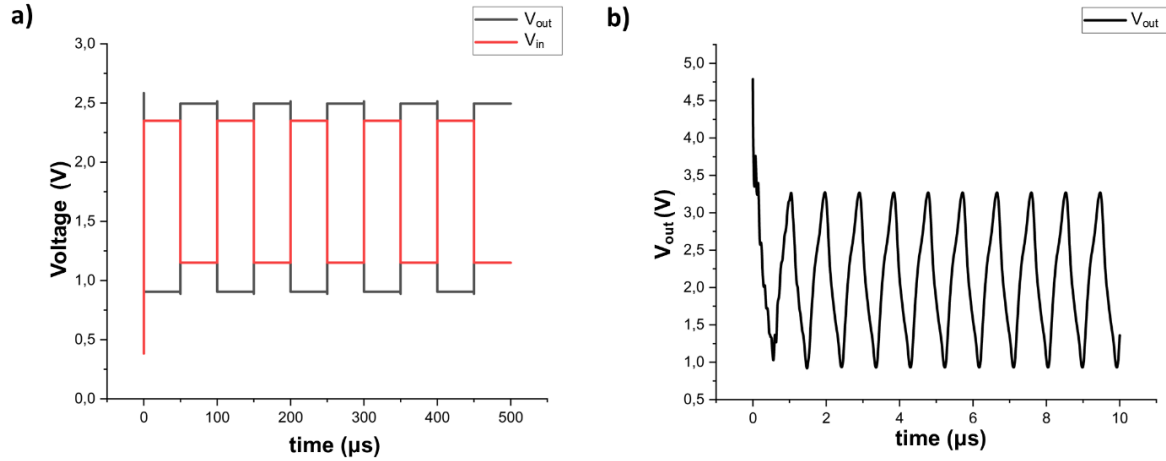


Figure 84 – Ring oscillator assessment. Simulation of the optimized inverter (a) and ring oscillator simulation (b).

4.6 Discussion

Modelling the fabricated devices plays a vital role in enhancing their performance and predicting the behaviour of oscillators, particularly when direct measurements are not feasible. The devices produced through a planar fabrication process demonstrated intrinsic cut-off frequencies of up to 80 GHz. This frequency, notably high compared to other values reported in the literature, highlights a strong correlation between the achieved f_T and the simplicity of the fabrication process, as shown in Table 1.

The practical realization of a ring oscillator using the optimized inverter confirms the design's viability and its potential applications in timing circuits and signal generation within digital systems. While simulations suggest the potential for oscillation, further enhancements are required to achieve reliable oscillation in the fabricated devices. Potential improvements include optimizing graphene-metal contacts, reducing the access length to decrease R_{exto} , using higher-quality graphene with increased carrier mobility, and enhancing substrate quality, such as by employing boron nitride. Additionally, the use of a high-k gate dielectric with reduced thickness could be advantageous. To address the mismatch in Dirac points among transistors, various techniques can be considered. These include chemical doping [152], electrical gating configurations [153], or induced strain in graphene [154]. Furthermore, ferroelectric polarization fields may also be used to shift the Dirac point [155].

It is important to note that, given the fabrication of various graphene transistors and oscillator topologies and considering the variability in graphene quality across the sample, some of the fabricated ring oscillators are likely to function. However, as previously mentioned in this thesis, time domain constrains prevented the validation of these oscillators.

5 CONCLUSIONS

Graphene has become a breakthrough material with high interests because of its unique properties and potentials for disruptive applications in various fields. Graphene's application in electronics, especially for radiofrequency (RF) circuits, is quite promising within its various use cases. Nevertheless, transferring this possibility into real-world graphene-based RF devices is a significant challenge requiring additional efforts and technological development. This thesis aimed to advance the understanding of graphene's capabilities, address the challenges associated with its integration into RF devices, and contribute to the development of state-of-the-art graphene technology.

This work is concerned with design, fabrication, and characterization of graphene-based RF transistors and oscillators paving the way of its integration in biosensors. These were developed using standard fabrication processes to be repeatable and enable seamless technology transfer to industrial applications. A comprehensive review of the literature identified key obstacles were performed.

The fabrication process was a critical aspect of this work, particularly in shared facilities, which required adaptations to prevent equipment contamination and accommodate facility limitations. Two fabrication methodologies were developed: a bottom-gate process without surface planarization and a planarized buried bottom-gate process using ion milling prior to graphene transfer. The use of critical point drying proved effective in preventing graphene from breaking after patterning. Despite constraints, these approaches proved effective, enabling the successful fabrication of graphene-based devices. The graphene's growth and transfer processes were also studied. The PMMA-assisted transfer method, while introducing residuals, showed negligible impact on the performance of graphene FETs due to the device dimensions. Challenges such as the production of large graphene flakes, which are critical for high-yield RF performance, were noted, being the influence of H_2 and CH_4 in the graphene morphology. The complexity of fine-tuning growth parameters and contamination from carbon nanotubes hindered the development of an optimized synthesis protocol. Consequently, continuous graphene films were employed for device fabrication to prioritize scalability and consistent performance.

The modelling and characterization of the fabricated devices highlighted the progress achieved. Intrinsic cutoff frequencies up to 80 GHz and a maximum oscillation frequency of 14 GHz were obtained using the planar bottom-gate topology with a 5 nm oxide layer. While a functional ring oscillator was not obtained with these transistors, simulations demonstrated that trimming inverter parameters enable the design of a RF graphene ring oscillators with this fabrication process. This underscores the potential of the proposed approach, contingent on further optimization. Despite the variability in graphene quality across samples, the thesis established a repeatable fabrication process applicable to other graphene-

based devices beyond the scope of this research. Proposed improvements include optimizing metal-graphene contacts, reducing access length to lower external resistance, and employing higher-quality graphene with enhanced carrier mobility. The use of improved dielectrics with high-k could also significantly elevate device performance.

In conclusion, this thesis has made significant contributions to leverage graphene technology use by addressing critical challenges in the design, fabrication, and characterization of graphene-based RF devices. Although the fabrication of a graphene oscillator demonstrating RF performance was not achieved, the findings of this research lay the groundwork for future developments. In particular, the potential application of this technology in biosensors is highly promising, thanks to the developed standard-compatible fabrication process and the designed layouts. Since graphene remains exposed during fabrication, this opens opportunities to develop functionalization methods specifically tailored for biosensing applications. These results provide a foundation for integrating graphene's unique properties into next-generation biomedical and RF technologies, paving the way for further exploration and innovation in these fields.

5.1 Future work

Future work should build on the progress achieved in this thesis, which provided valuable insights into graphene's RF properties and developed a process compatible with the standard fabrication processes. To validate the proposed ring oscillator design, fabrication using the optimized parameters and improvements outlined in this research is essential. This practical realization would confirm the accuracy of the simulations and enable further performance refinement. Considering the intended application of these ring oscillators in biosensors, their validation should include functionalization strategies. This could involve functionalizing graphene interconnects or using the capacitive elements of the proposed graphene-based structures. Such functionalization would allow for changes in the oscillation frequency in response to the binding of specific analytes, paving the way for highly sensitive and selective biosensor development. Additionally, the properties of graphene must be further enhanced to improve device performance. Efforts should focus on increasing carrier mobility, minimizing defect density, and refining synthesis methods to produce high-quality, uniform graphene. A back gate should be applied to shift the Dirac point of the transistors, enabling the use of the devices at reasonable voltages. These advancements would not only optimize the performance of RF devices but also broaden graphene's potential applications in cutting-edge electronic and sensing technologies.

6 REFERENCES

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