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Processing-Induced Performance Limits of Platinum Resistance Temperature Detectors for Reliable Organ-On-A-Chip Sensing

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Received: 2 June 2026 | **Revised:** 29 July 2026 | **Accepted:** 6 August 2026

Keywords: annealing | microfabrication | platinum | resistance-temperature-detectors | resistivity

ABSTRACT

Reliable temperature monitoring remains a critical bottleneck in Organ-on-a-Chip (OoC) systems, where integrated temperature sensors must provide electrical stability, biocompatible encapsulation, and efficient thermal coupling to the biological environment. While the effects of thermal annealing on platinum (Pt) thin films are well established, the influence of fabrication-related thermal budgets associated with OoC manufacturing has not been systematically correlated with device performance. Here, we establish a direct processing–microstructure–device performance relationship for Pt-based resistance temperature detectors (RTD). Using Si/Pt and Si/SiO_2/Pt architectures, we investigate the impact of thermal annealing (up to 900°C) on film morphology and electrical properties and correlate them with device-level sensing performance. Moderate annealing temperatures (≈300°C), representative of oxide passivation processes, significantly improve electrical performance, reducing resistivity by up to 40% and increasing the temperature coefficient of resistance (TCR) through stress relaxation and grain coarsening. Higher annealing temperatures induce surface roughening and morphological instability, compromising sensor reliability. A SiO_2 interlayer delays degradation and reduces resistivity drift, preserving film integrity under harsh thermal conditions. These results demonstrate that the thermal budget associated with dielectric passivation can be exploited to optimize RTD performance while defining practical processing windows for reliable integration into OoC and other biointegrated microsystems.

1 | Introduction

Precise temperature regulation is essential in Organ-on-a-Chip (OoC) systems, as even small thermal fluctuations can alter cellular behavior and compromise the physiological relevance of microengineered tissues. To maintain stable thermal conditions, OoC platforms commonly integrate microheaters and resistance temperature detectors (RTDs), with platinum (Pt) and aluminum (Al) being among the most widely used materials for their fabrication due to their compatibility with microfabrication processes [1–3]. Among these, Pt is particularly attractive due to its high temperature coefficient of resistance (TCR), chemical stability, high conductivity, long-term reliability, and biocompatibility [4, 5]. Accordingly, several Pt-based RTDs have been reported in the literature, demonstrating high sensitivity and linearity across physiologically relevant temperature ranges [2, 4, 6].

The influence of thermal processing conditions on sputtered Pt thin films has been extensively investigated, particularly regarding the effects of post-deposition annealing on grain growth, residual stress relaxation, electrical resistivity, temperature coefficient of resistance (TCR), and long-term thermal stability [7–12].

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In addition, several studies have examined the influence of adhesion layers [13], substrate materials [9], and high-temperature stability on Pt-based RTDs [12], providing important insights into material optimization and sensor performance. Comparisons with alternative materials, such as aluminum, further highlight the superior electrical stability and sensing characteristics of Pt, although differences in thermal uniformity and device integration strategies remain [1, 7].

However, these studies have primarily investigated thermal annealing as a material optimization strategy. Unlike previous studies, which intentionally employed post-deposition annealing to optimize Pt thin-film properties, the present work investigates the unavoidable thermal exposure associated with the standard OoC fabrication workflow. In particular, we examine how the thermal budget introduced by mandatory dielectric passivation influences Pt microstructural evolution, electrical properties, and device-level RTD performance. In OoC devices, dielectric passivation is a mandatory fabrication step that typically involves moderate thermal processing (≈300°C), thereby exposing the underlying Pt thin films to a fabrication-induced thermal budget capable of modifying their microstructure and electrical properties. Despite its practical relevance, this fabrication-induced thermal budget has not been systematically investigated.

Silicon is widely employed as the substrate material for OoC platforms [14] because it enables direct monolithic integration with Complementary Metal-Oxide-Semiconductor (CMOS) electronics, allowing the co-integration of microheaters, RTDs, and additional sensing functionalities on the same chip. Such integrated architectures require dielectric layers that electrically isolate the metallic devices from both the silicon substrate and the biological environment, making oxide deposition an essential fabrication step.

In OoC applications, an electrically insulating passivation layer is required to ensure safe and reliable device operation while maintaining adequate thermal coupling with the biological environment (Figure 1a). This dielectric layer, typically silicon dioxide (SiO_2) [15, 16] or silicon nitride (Si_3N_4) [17, 18], acts as an electrical barrier between the metallic heaters or RTDs and the cellular culture medium, preventing current leakage and electrochemical reactions. Although these dielectric materials exhibit a much lower thermal conductivity than silicon, their small thickness results in a sufficiently low thermal resistance to maintain effective heat transfer between the sensing element and the biological environment. SiO_2 also exhibits excellent biocompatibility and low toxicity, making it particularly suitable for these applications. In addition to its role as a top passivation layer, SiO_2 is widely used as a dielectric interlayer between the silicon substrate and the metallic film, where it provides electrical insulation, improves interfacial stability, and suppresses metal-silicon interdiffusion during thermal processing [14, 19, 20]. Both the interlayer and the passivation layer serve distinct functional roles, yet together they contribute significantly to the overall device performance and reliability.

Among the available deposition techniques, plasma-enhanced chemical vapor deposition (PECVD) is widely used for oxide passivation in microfabricated devices due to its exceptional coating uniformity, conformality, strong adhesion, and compatibility with complex geometries [21–23]. However, PECVD processes inherently involve moderate thermal budgets (≈300°C) that are often unavoidable and required to ensure film quality and adhesion. While alternative low-temperature approaches exist, they often compromise film density, stability, or interface quality. Consequently, this thermal exposure should not simply be regarded as a fabrication constraint, but also as a potential opportunity to tailor the microstructure and electrical performance of the underlying Pt thin films without introducing additional processing steps.

In this work, rather than investigating thermal annealing as an isolated material optimization strategy, the novelty lies in examining the thermal budget inherently associated with OoC fabrication and establishing a direct link between thermal processing, Pt microstructural evolution, electrical properties, and device-level RTD performance. By combining a systematic annealing study up to 900°C with morphological and electrical characterization, device-level measurements, and finite-element modelling, we show how the thermal budget governs the evolution of Pt film properties and their impact on RTD response. We demonstrate that moderate thermal treatments, representative of passivation processes (≈300°C), improve conductivity and TCR through grain coarsening and defect reduction, whereas higher temperatures lead to morphological instability and performance degradation. Furthermore, we show that SiO_2 interlayers act as effective diffusion barriers, extending the thermal stability window and preserving electrical integrity.

By linking fabrication-related thermal budgets to material properties and device functionality, this work defines practical processing windows for the reliable integration of Pt thin-film RTDs into OoC platforms. Rather than introducing an additional annealing step, our results demonstrate that the thermal budget already associated with dielectric passivation can be exploited to optimize sensor performance while preserving fabrication compatibility, thereby improving temperature accuracy and long-term reliability of integrated OoC platforms. These findings provide practical design guidelines for thermally robust sensing platforms in OoC and related microfabricated systems.

2 | Materials and Methods

2.1 | Materials and Fabrication

The experimental workflow comprised two stages. In the first stage, thin-film test samples with two configurations were fabricated to study the effect of the SiO_2 interlayer and thermal annealing on Pt films: one consisting of a multilayer stack of SiO_2, Ta, and Pt; and another comprising only Ta and Pt deposited directly onto the substrate. For both cases, the substrate was a single side polished 8-inch silicon wafer with 725 µm in thickness. In the first configuration, illustrated in Figure 1b(b.1), a 1 µm SiO_2 insulating layer was previously deposited by PECVD at 300°C for 30 min, using a PECVD (CPX from SPTS) equipment. Then, a metallic bilayer consisting of an adhesion layer of Ta (5 nm) and Pt (234 nm)

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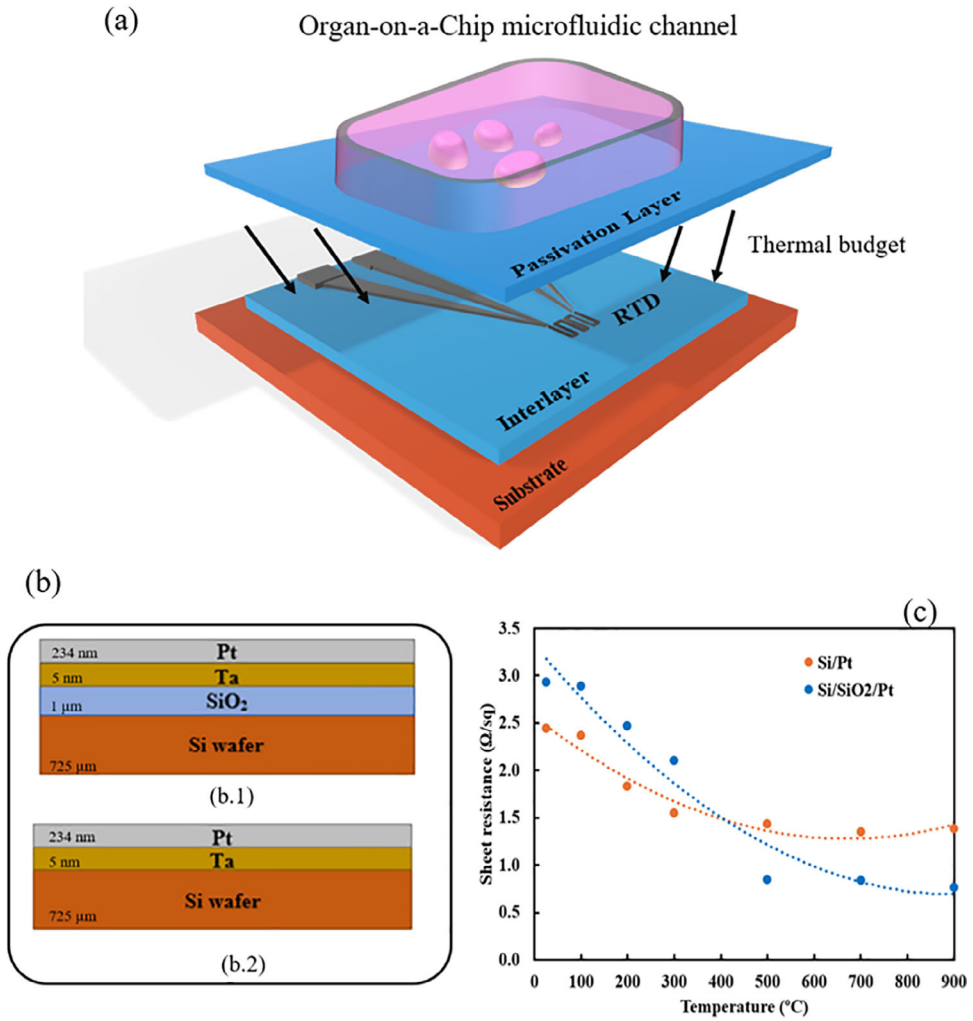


FIGURE 1 | (a) Schematic illustrating the two oxide roles for an OoC device. The interlayer oxide electrically isolates the RTD from the substrate, while the passivation oxide protects the RTD from the fluidic cellular medium above inside the microfluidic channel. (b) Schematic cross-sections (not in scale) of the first stage fabricated configurations: (b.1) Pt/Ta on SiO_2/Si wafer and (b.2) Pt/Ta directly on Si wafer. (c) Evolution of the sheet resistance of Pt thin-films (Ω/sq) with the increase of the annealing temperature for Si/Pt and Si/SiO_2/Pt thin-film stacks.

was deposited by DC sputtering (KS1000 from Kenosistec). The selected thicknesses of SiO_2 ensure robust electrical insulation from the silicon substrate, minimizing leakage currents and guaranteeing stable RTD operation in contact with biological media; whereas the thickness of Ta guarantees strong interfacial bonding preventing delamination during thermal cycling without significantly affecting the electrical properties of the sensing layer; and the thickness of Pt represents an optimal compromise between electrical stability, TCR performance, and resistance to thermally induced morphological degradation [13]. The second configuration, shown in Figure 1b(b.2), followed the same process flow, but excluded the SiO_2 deposition step, enabling a direct comparison of devices fabricated with and without the oxide interlayer, thereby assessing its influence on the overall device performance. In both configurations, the thickness of the Pt layer was measured using a mechanical profilometer (KLA, Tencor P-16+ Surface Profiler), yielding an average value of 234 nm.

In the second stage, functional devices, specifically two types of RTDs, were fabricated. Both employing the SiO_2 interlayer, which was identified in the first stage as beneficial for the device stability. The RTDs were fabricated on 8-inch single-side polished Si wafers using a combination of photolithography and lift-off techniques. To define the pattern, a bilayer resist system was employed: LOR 5B (0.5 µm, Kayaku Advanced Materials) was first spin-coated, followed by AZ 1505 (1.035 µm, MicroResist). Patterning was performed using a direct-write lithography system (Heidelberg Instruments, DWL 2000). After exposure, the resist was developed using AZ 400K developer (MicroResist). Subsequently, the desired metal configurations were deposited, and the final structures were obtained through a lift-off process, leaving the patterned RTD stack intact. Two sets of RTDs were fabricated: one without any additional passivation layers, and another with passivation encapsulation deposited by PECVD, using an SPTS PECVD system. In the latter case, a 1 µm-thick SiO_2 passivation layer was first deposited at 300°C, followed by a 300 nm-thick SiN_x layer deposited under the same temperature conditions. These layers provided additional insulation and surface protection for the encapsulated RTDs. This passivation step also includes a thermal budget (300°C, 30 min), allowing for the evaluation of whether the annealing inherent to oxide

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deposition produces the same effects observed in the initial thin-film annealing study.

2.2 | Thermal Annealing Treatment

The Pt films of the test samples (from the first experimental stage, Figure 1b) were subjected to a series of thermal annealing steps at increasing temperatures of 100°C, 200°C, 300°C, 500°C, 700°C, and 900°C using a TCVD system (Roth & Rau) in an argon (Ar) atmosphere. Each annealing step was performed for 30 min, corresponding to the typical processing times for SiO_2 deposition [24].

After each annealing step, a systematic evaluation of the influence of annealing temperature on the electrical and morphological properties of the Pt thin-films was performed, with direct implications for their application as RTDs.

2.3 | Electrical Characterization

The samples were electrically characterized after the PECVD deposition and also after each annealing step at 100°C, 200°C, 300°C, 500°C, 700°C, and 900°C. Resistance measurements were carried out using a CMT-SR2000N sheet resistance probe based on the four-point probe method [25]. In this configuration, the two outer probes supply current to the Pt film, while the two inner probes measure the voltage drop, thus eliminating contact and lead resistance effects, as no current flows through the voltage probes, ensuring accurate determination of the sheet resistance. This setup assures the precise evaluation of the electrical stability of the Pt films as a function of the applied thermal annealing treatments.

2.4 | Surface Morphology Characterization

The morphological properties of the Pt films were inspected using two complementary techniques: scanning electron microscopy (SEM) and atomic force microscopy (AFM). SEM provided high-resolution analysis of surface morphology, grain size, and microstructural homogeneity, enabling the identification of annealing-induced changes in the film structure. Elemental composition was evaluated by energy-dispersive X-ray spectroscopy (EDX) using an Oxford Instruments detector, with spectra processed using INCA Suite software (version 4.15). The images were obtained using a NovaNanoSEM 650 system. AFM was employed to obtain three-dimensional nanoscale surface profiles, allowing quantitative assessment of surface roughness and fine morphological features. A force microscope (model Dimension Icon, Bruker) working in tapping mode was employed. For the measurements, a silicon AFM tip with aluminum coating and a radius of curvature below 10 nm was used in air. The stiffness of the cantilever was 48 N/m. The scan size was 5 μm × 5 μm and 2 μm × 2 μm. For each test sample, 256 line scans and at least three measurements were performed. The root-mean-square (RMS) area was the chosen parameter to describe the surface morphology. All the data were analyzed by using Gwyddion software v.3.63. Together, both methods offered a comprehensive view of the evolution of Pt thin-film morphology under different thermal annealing conditions.

3 | Experimental Results—Thin-Film Test Samples

3.1 | Electrical Characterization

Figure 1c shows the sheet resistance of Pt films annealed for 30 min at different temperatures, comparing Pt directly deposited on Si (Si/Pt) with Pt deposited on a SiO_2 layer ($Si/SiO_2/Pt$).

The sheet resistance decreases with increasing annealing temperature, with the effect being significantly more pronounced in the SiO_2 samples at temperatures above 400°C. This reduction in sheet resistance is primarily attributed to microstructural changes in the Pt films. As the temperature rises, grain growth occurs, leading to larger crystalline domains and fewer grain boundaries, which reduces electron scattering. Additionally, thermal annealing helps eliminate structural defects such as dislocations and vacancies, further enhancing the conductivity of the film. These combined effects result in an improved conductivity of the Pt film, especially noticeable at higher annealing temperatures [24].

For Si/Pt, the resistance decreases up to about 500°C but subsequently stabilizes and slightly increases at higher annealing temperatures. This behavior is attributed to Pt/Si interdiffusion and the formation of Pt silicides, as well as partial film dewetting, both of which disrupt the conductive pathways [26].

In contrast, the SiO_2 interlayer acts as a diffusion barrier, preventing silicidation and enabling further densification and crystallization of the Pt film. Consequently, the sheet resistance decreases monotonically from approximately 3.0 Ω/sq at room temperature to approximately 0.6 Ω/sq after annealing at 900°C, approaching the resistivity expected for well-crystallized Pt thin-films and close to the bulk resistivity of Pt, 10.62 μΩ·cm (0.45 Ω/sq for a 234 nm film) [27]. These results demonstrate that introducing a SiO_2 barrier substantially enhances the thermal stability and electrical performance of the heated Pt films, making the $Si/SiO_2/Pt$ stack more suitable for RTD applications in OoC platforms.

3.2 | Surface Morphological Characterization

The electrical behavior is strongly correlated with morphological changes, which were observed by SEM, as presented in Figure 2. In the $Si/SiO_2/Pt$ configuration (Figure 2a), the Pt film evolves from a fine-grained micro-structure, observed after deposition, to larger, coalesced grains at annealing temperatures between 500°C and 700°C. This grain growth correlates with the lowest measured sheet resistance values, indicating improved electrical conductivity due to reduced grain boundary scattering. At 900°C, the film exhibits early-stage agglomeration, with island formation and surface roughening. Although these features indicate the onset of structural degradation, they do not yet produce a measurable change in the electrical resistance, which remains stable above 500°C.

SEM images of the Si/Pt system are presented in Figure 2b. In this configuration, surface morphology changes occur at lower temperatures compared to the Si/SiO2/Pt system. Irregular grain structures and enhanced surface roughness are already evident

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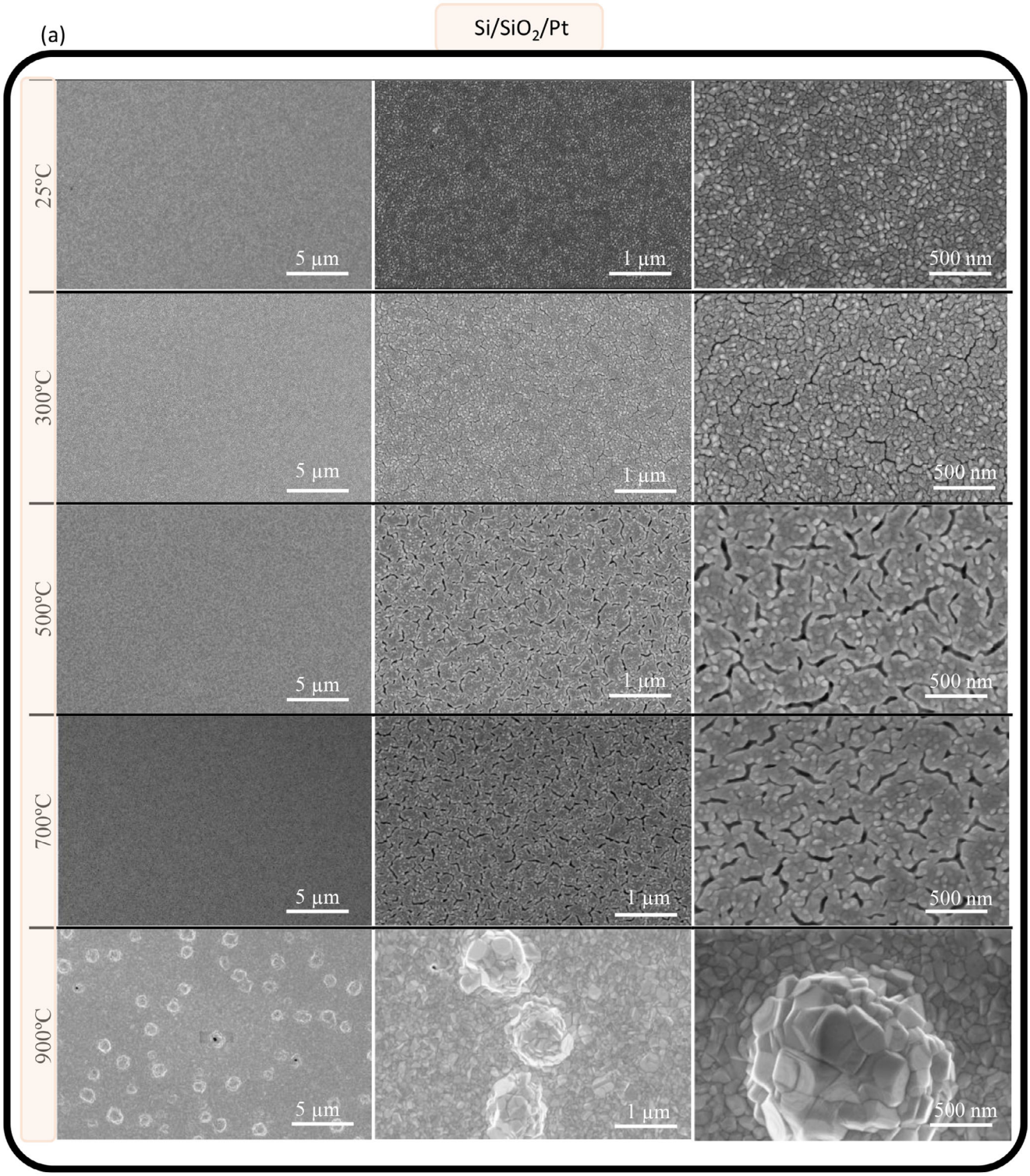


FIGURE 2 | SEM micrographs of (a) $Si/SiO_2/Pt$ and (b) Si/Pt films annealed at different temperatures.

after annealing at 500°C. These features are consistent with Si/Pt interdiffusion and silicide formation, explaining the limited improvement and eventual degradation in electrical performance compared to $Si/SiO_2/Pt$ configuration (Figure 1c).

The AFM roughness analysis (Figure 3) quantitatively supports the morphological changes observed in the SEM images, confirming the evolution of surface features with annealing temperature. For each sample and annealing condition, the root mean square roughness (Sq) was measured in four independent scan areas to account for local morphological variations. The mean and standard deviation were then calculated from these independent measurements, providing a statistically representative assessment of the film topography.

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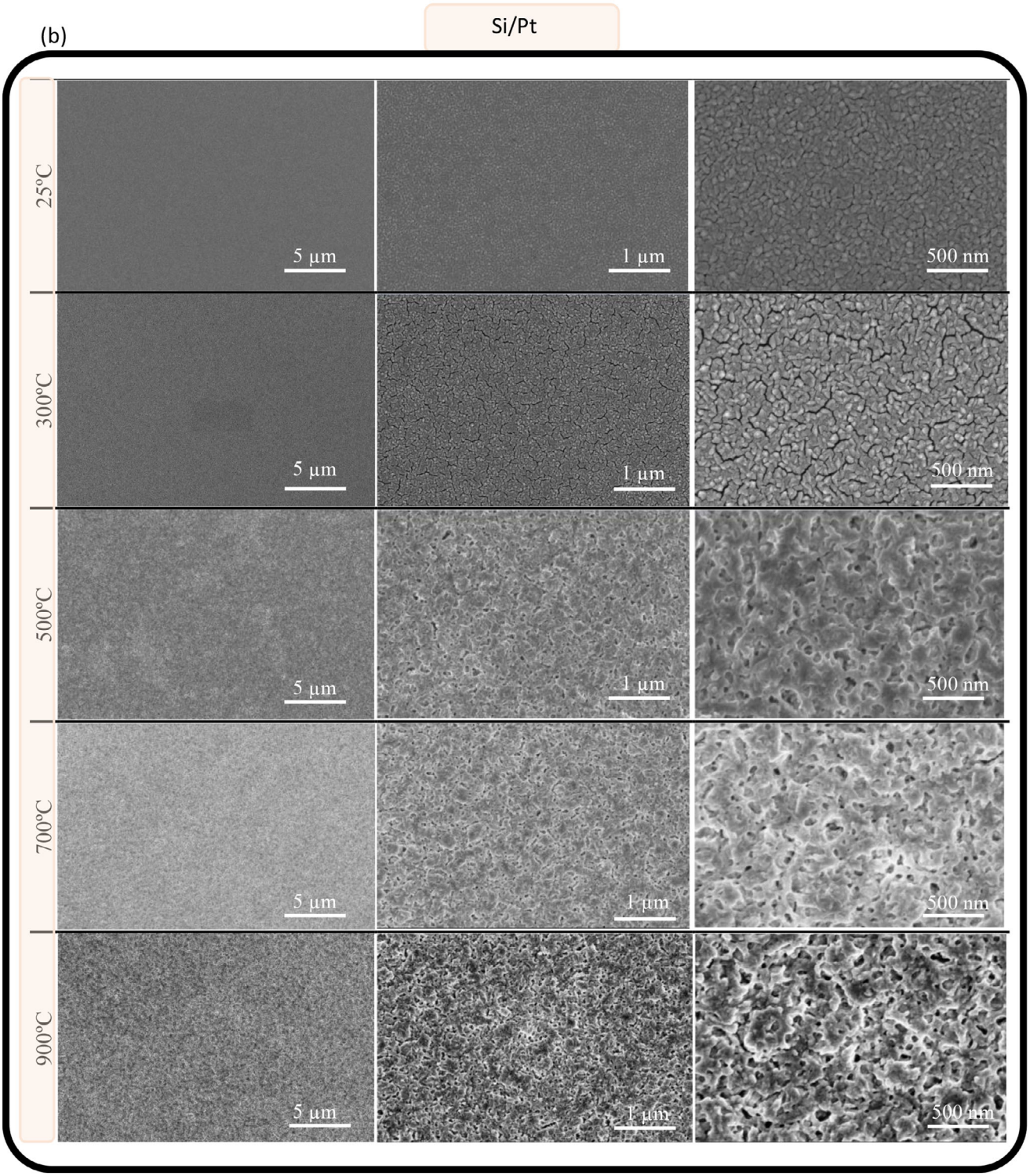


FIGURE 2 | (Continued)

As presented in Figure 3a,b, the roughness of Si/Pt films increases significantly after 500°C, reaching values above 20 nm and remaining elevated at higher temperatures. In contrast, the $Si/SiO_2/Pt$ samples maintain lower surface roughness (<10 nm) up to 700°C, confirming the stabilizing effect of the SiO_2 barrier (Figure 3a). However, at 900°C both the average roughness and the variability between measurements increase significantly, as indicated by the error bars (Figure 3a). This reflects a pronounced surface heterogeneity caused by agglomeration, consistent with the analysis of the SEM images.

Together, the SEM and AFM results demonstrate that the SiO_2 interlayer plays a critical role in preserving both the morphology and the nanoscale surface quality of Pt films under high-temperature processing, directly supporting the superior electrical stability observed in Section 3.1 (Figure 1c).

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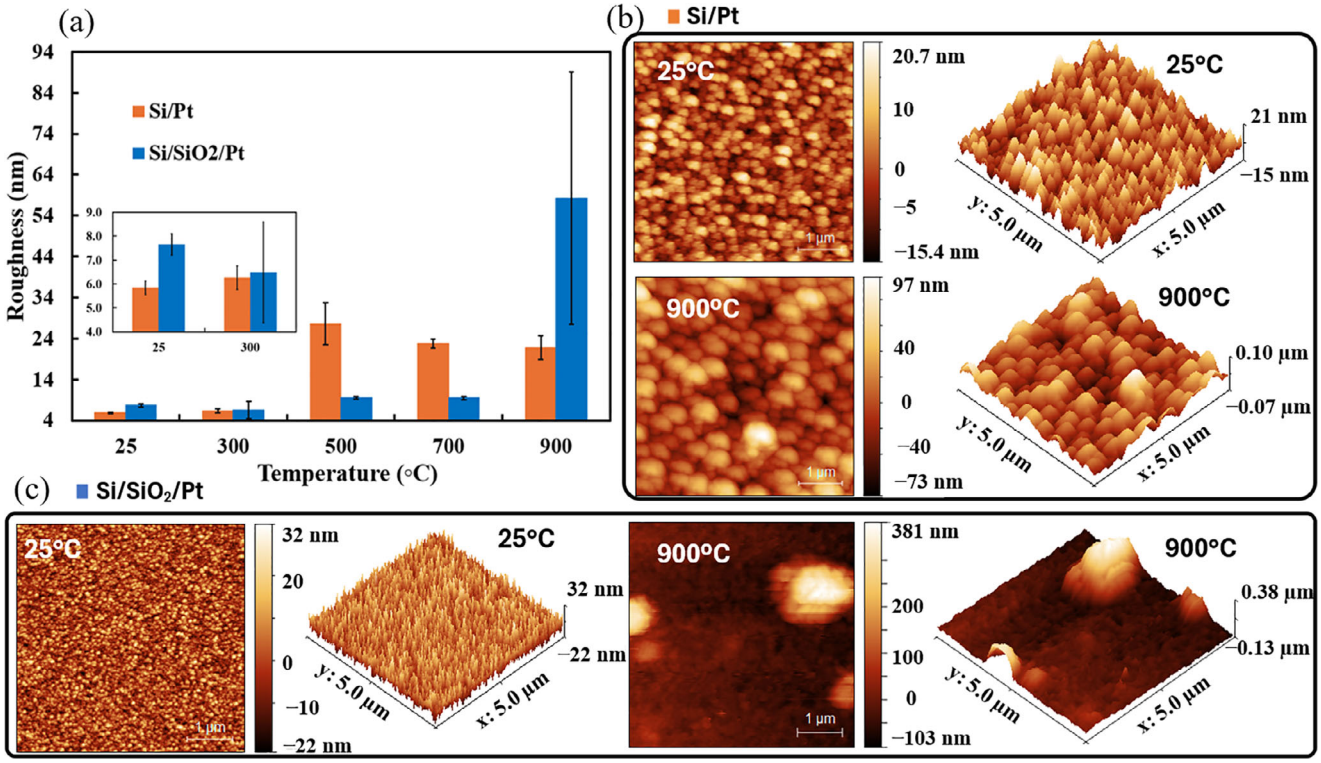


FIGURE 3 | (a) Root mean square roughness of Pt films as a function of the annealing temperature, obtained by AFM analysis, for the two stack configurations: Si/Pt and Si/SiO_2/Pt. AFM surface topography and corresponding 3D views for (b) Si/Pt and (c) Si/SiO_2/Pt samples, at 25°C and 900°C.

To further investigate the morphological degradation observed at high annealing temperatures, EDX analyses were performed on selected samples annealed at 900°C. Figure 4 presents the EDX spectra acquired for the Si/Pt configuration in the as-deposited state and after annealing at 900°C, as well as for the Si/SiO_2/Pt configuration at 900°C, distinguishing between localized surface protrusion and flat region identified in the SEM micrographs. EDX measurements were performed at 5 kV to enhance surface sensitivity and improve detection of light elements (Si and O). Under these conditions, Pt was detected through its M-lines (≈1.5–2.3 keV).

For the Si/Pt samples (Figure 4a,b), the as-deposited film exhibits a spectrum dominated by Pt peaks, confirming the integrity of the metallic layer prior to thermal treatment. However, after annealing at 900°C in an Ar atmosphere, the EDX spectrum reveals a significant increase in the Si signal along with detectable presence of oxygen, likely arising from brief contact with air between process steps and due to residual impurities. Quantitative analysis shows that while Pt remains the dominant element (≈84%), a substantial Si contribution (≈12%) and detectable oxygen content (≈3%) emerge. This compositional change provides direct evidence of Pt-Si interdiffusion and partial surface oxidation at high temperatures, consistent with Pt silicide formation and interfacial reactions. These processes explain the morphological roughening and the degradation of electrical performance observed for the Si/Pt stack above 500°C.

In contrast, the Si/SiO_2/Pt samples annealed at 900°C exhibit markedly different behavior (Figure 4c,d). EDX spectra acquired from both the flat region and localized surface protrusion region show Pt contents exceeding 99%. Importantly, no significant compositional difference is observed between the localized surface protrusion and flat regions, indicating that the large hillocks observed by SEM originate from Pt surface diffusion and agglomeration rather than from chemical contamination or substrate interdiffusion. The absence of a strong Si signal confirms the effectiveness of the SiO_2 interlayer as a diffusion barrier, preventing Pt-Si reactions even under extreme thermal exposure.

Therefore, the results obtained from the EDX analysis, SEM imaging, and AFM measurements demonstrate that the underlying mechanisms differ fundamentally between the two configurations. In the absence of an oxide interlayer (Si/Pt stack), high-temperature annealing promotes chemical interdiffusion and silicide formation, accelerating morphological breakdown and electrical instability. Conversely, in the Si/SiO_2/Pt stack, the SiO_2 interlayer suppresses interdiffusion, confining degradation to physical agglomeration processes at very high temperatures (≥ 900°C), while preserving the chemical purity and electrical continuity of the Pt film over a much wider thermal window.

4 | Application to RTD Devices

The annealing study presented in Section 3 sheds new line on the thermal budget that the Pt film will experience during SiO_2 passivation deposition (≈300°C for 30 min) and reveals how the SiO_2 interlayer stabilizes the Pt structure under high-temperature processing.

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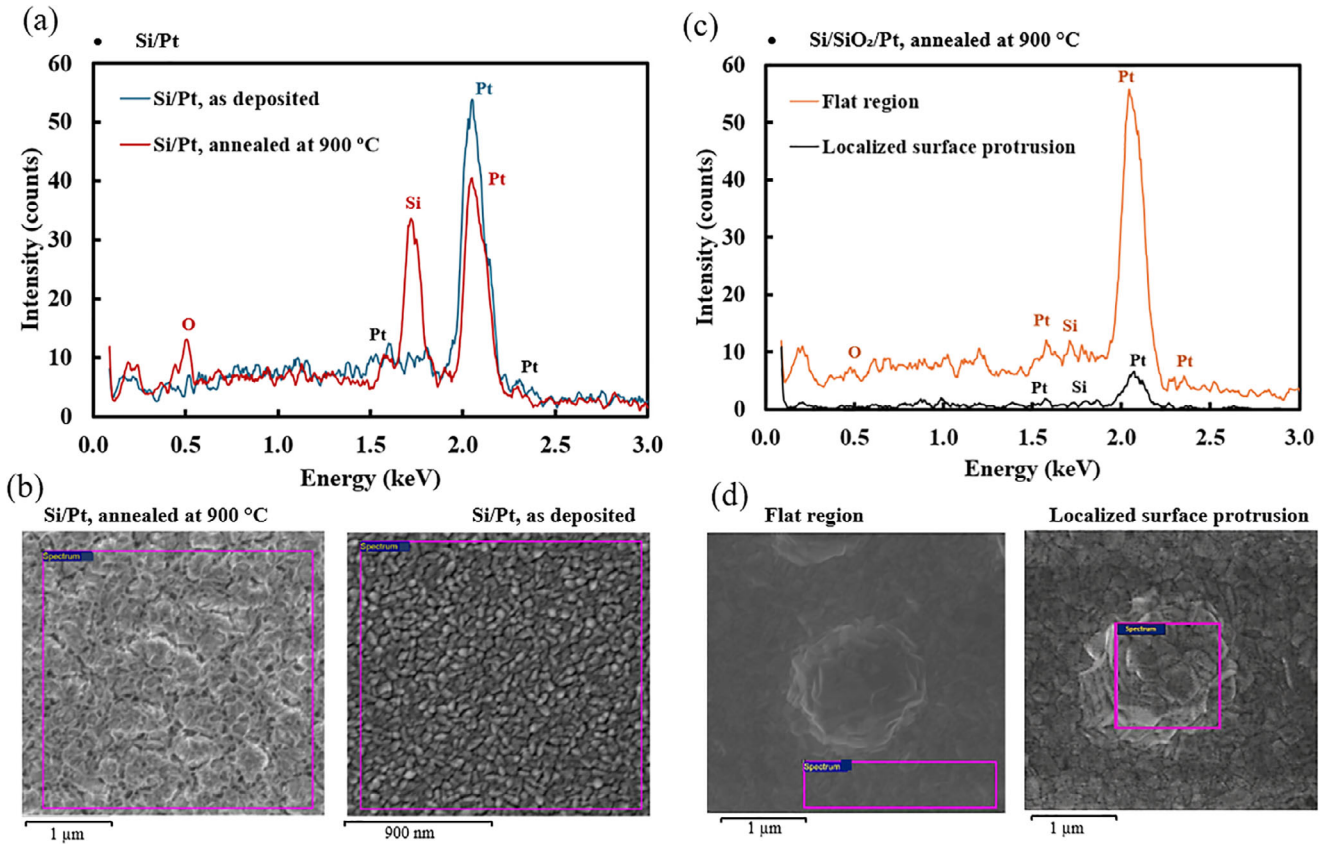


FIGURE 4 | (a) EDX spectra of Si/Pt samples in the as-deposited state and after annealing at 900°C. (b) Corresponding SEM micrographs of EDX acquisition areas in (a). (c) EDX spectra acquired on the $Si/SiO_2/Pt$ sample annealed at 900°C, comparing flat regions and protrusion regions identified in SEM images. (d) SEM locations corresponding to the EDX acquisition areas in (c), highlighting the agglomerated and non-agglomerated.

In practice, however, OoC platforms operate in the physiological range (35-45°C). The purpose of this section is therefore to translate these material-level findings to functional RTDs fabricated on the same $Si/SiO_2/Pt$ base stack and to evaluate whether the fabrication-related annealing will affect their sensing behavior in the OoC operating regime. To this end, two complementary analyses were performed: (i) finite-element numerical simulations of $Si/SiO_2/Pt$ RTDs with and without an additional SiO_2 passivation layer, and (ii) experimental characterization of fabricated RTDs across the 35–45°C range, comparing devices with and without a passivation layer.

4.1 | Numerical Simulations of the Thermal and Electrical Behavior of the RTDs

Finite element simulations were performed in COMSOL Multiphysics (v5.3) to reproduce the electrical and thermal behavior of RTDs for further integration in OoC devices. The device geometry is shown in Figure 5a, which integrates two spiral-shaped microheaters and eight four-wire Pt RTDs radially distributed. This design was conceived to provide both localized heating and distributed temperature monitoring in microfluidic devices for OoC applications [28]. In the present work, only one RTD was selected for numerical analysis, since the goal was not to assess the entire platform, but to isolate and understand the impact of oxide deposition and annealing on the Pt film properties and, ultimately, to output a model to predict this impact. The other RTDs and microheaters were not included in this study but remain available for future experimental validation within OoC environments.

As illustrated in Figure 5b, the numerical model considers single-crystal silicon as the substrate, SiO_2 as the dielectric interlayer, and Pt as the metallic sensing element. The material properties were obtained from COMSOL Multiphysics material library [29]. The simulations were performed under prescribed temperature conditions (35–45°C) to evaluate the electrical response of the RTD, rather than to analyze heat transfer within the substrate. The Pt layer was modelled as a conductive thin shell, while the SiO_2 layer was modelled as an electrically insulating dielectric interlayer with a thermal conductivity of 1.4 $W{\cdot}m^{-1}{\cdot}K^{-1}$, consistent with literature values for SiO_2 [30]. A sensitivity analysis confirmed that moderate variations in the thermal conductivity of the SiO_2 layer do not affect the simulated RTD response under the imposed thermal boundary conditions (Figure S1). Although SiO_2 has a much lower thermal conductivity than silicon, its thickness of 1 µm results in a sufficiently low thermal resistance to maintain effective thermal coupling between the Pt sensing layer and the substrate. A Pt layer with a thickness of 234 nm and a SiO_2 interlayer of 1 µm were used, matching the measured values of the experimentally deposited films (cf. Section 4.2).

The physics setup combined electrical and thermal domains. The Electric Currents in Shells interface described current conduction through the Pt track, while Heat Transfer in Solids modeled

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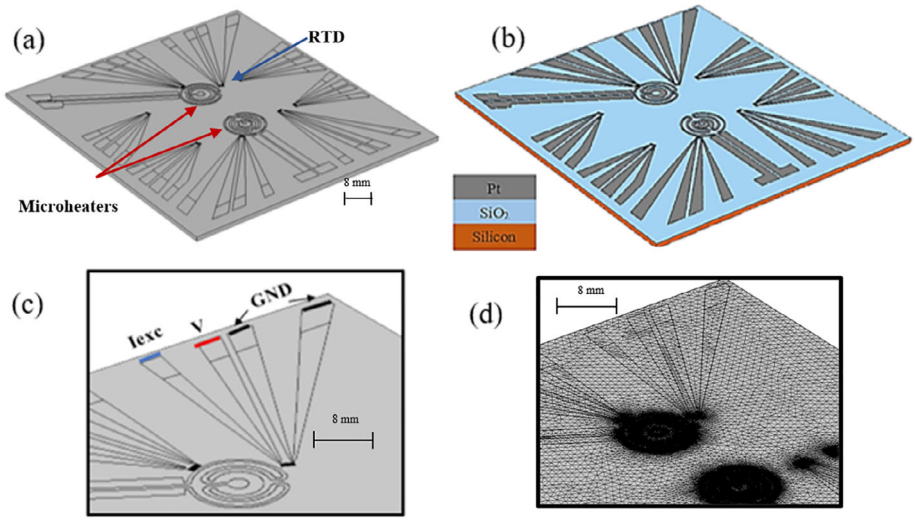


FIGURE 5 | Schematic representation of the simulated RTD chip and model configuration. (a) 3D geometry of the full microdevice containing two integrated microheaters and eight four-wire platinum RTDs. (b) Layered structure of the model showing the $Si/SiO_2/Pt$ stack used in the numerical simulations. (c) Detail of one RTD highlighting the electrical boundary conditions applied in the simulation: excitation current (I_{exc}), voltage probe (V), and ground (GND). Only one RTD was activated in the simulation, as it represents the configuration used for experimental comparison, while the remaining structures will be used in future OoC applications. (d) Detail of the mesh for the finite element analysis, generated for the thermal and electrical coupled analysis.

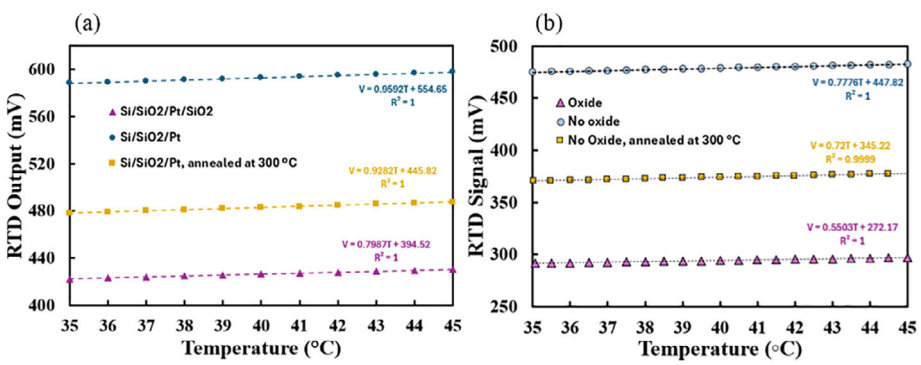


FIGURE 6 | (a) Simulated electrical response of platinum RTDs in the physiological temperature range (35–45°C) for three configurations: with SiO_2 passivation layer on top of Pt (purple triangles); without oxide on top (blue circles); and without oxide on top but annealed at 300°C for 30 min (yellow squares). (b) Experimentally measured electrical response of platinum RTDs in the physiological range (35–45°C) for three configurations: with SiO_2 passivation layer deposited on top of Pt (purple triangles), without oxide on top (blue circles), and without oxide on top but annealed at 300°C for 30 min (yellow squares).

temperature evolution within Pt, Si, and SiO_2. Multiphysics coupling via Electromagnetic Heating (Joule heating) converted electrical dissipation into thermal power. Boundary conditions included electrical contacts at the RTD terminals and thermal insulation at the sample edges. One boundary pad was defined to excite the RTD with a current of 100 μA (*Iexc*), two boundaries as ground (*GND*), and another boundary as a terminal to measure voltage (*V*) (Figure 5c). A refined mesh (Figure 5d), with 1987055 elements and a minimum element size of 10.4 μm, was applied to the entire geometry to accurately capture the output voltage as a function of temperature, $V(T)$, of the RTD using a stationary solver.

Figure 6a presents the simulated electrical response of the Pt RTDs in the physiological temperature range (35–45°C), considering three configurations: (i) with no oxide passivation on top ($Si/SiO_2/Pt$), (ii) with oxide passivation on top ($Si/SiO_2/Pt/SiO_2$), and (iii) with no oxide passivation on top but annealed at 300°C for 30 min.

Initial simulations using identical electrical material parameters (theoretical Pt resistivity ρ_0 and TCR) for cases (i) and (ii) revealed that the response of the RTDs was unchanged by the presence of a SiO_2 passivation layer. The results of this simulation (Figure S2 and Table S1) confirm that from an electrical standpoint, the SiO_2 layer does not significantly affect the intrinsic resistivity or temperature sensitivity of the Pt film, as it does not form part of the electrical conduction path. In a four-terminal RTD configuration, the measurement current flows within the Pt layer, while the sensor measures the voltage drop across this metallic

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TABLE 1 | Measured resistivity (21°C) and TCR for the Pt-based RTD structures before and after annealing at 300°C.

RTD	Resistivity (Ω•m)	TCR ($°C^{-1}$)
$Si/SiO_2/Pt$	6.85×10^{-7}	0.00163
$Si/SiO_2/Pt/SiO_2$	4.92×10^{-7}	0.00189
$Si/SiO_2/Pt$—Annealed 300°C	5.57×10^{-7}	0.00194

resistor. Consequently, the presence of the passivation layer has a negligible impact on the electrical behavior of the RTD, and its role is primarily thermal rather than electrical.

To better align the numerical model with the experimental behavior, the values of ρ_0 and TCR were updated using the experimental measurements obtained from the fabricated devices, as described in Sections 3.1 and 4.2. These experimentally adjusted parameters (Table 1) reflect not only the intrinsic properties of Pt but also the influence of the fabrication process, which affects film morphology, grain structure, residual stress, and possible impurities or surface contamination. Since these factors modify the effective resistivity, ρ_0, and TCR of the Pt thin-film, incorporating the experimentally extracted ρ_0 and TCR values resulted in simulated RTD characteristics that better replicate the observed measurements. As shown in Figure 6a, all configurations display a linear relationship between RTD voltage output and temperature, with correlation coefficients equal to one ($R^2 \approx 1$), confirming excellent thermal sensitivity and ohmic behavior. The slope of each curve reflects the TCR of the Pt film. The simulated RTD responses (with the experimental ρ_0 and TCR) reproduced the relative trends observed experimentally, confirming that variations in electrical output are originate from process-induced modifications of the Pt thin-film rather than from the presence of the passivation layer itself. This trend confirms that the improvement observed in oxide-coated RTDs primarily arises from the thermal annealing effect introduced during oxide deposition. This process promotes Pt grain growth and reduces defect density, effects consistent with the SEM and AFM characterizations discussed in Section 3.2. These findings emphasize the critical role of thermal processing in shaping the electrical behavior of thin-film Pt temperature sensors.

4.2 | Experimental Characterization of the RTD Devices

To directly assess the implications of the thin-film analysis for practical device operation, the Pt RTDs presented in Section 4.1 were fabricated and tested, as shown in Figure 7.

As predicted by the first simulations (performed without incorporating the experimentally measured ρ_0 and TCR, *cf*. Figure S2), the SiO_2 passivation layer was not expected to influence the intrinsic resistivity of the RTD. However, the experimental results revealed the opposite trend, with passivated devices exhibiting a lower resistance (Figure 6b). Once again, the addition of a SiO_2 layer decreased the device resistance or, similarly, increased the conductivity as previously discussed and further attested in the simulations with the measured ρ_0 and TCR, as predicted in Figure 6a. Thus, RTDs with a SiO_2 passivation layer exhibited a lower electrical resistance than devices without passivation oxide. To decouple the effect of the oxide from the effect of the deposition process, a third test was performed using the device with no oxide but subjected to a controlled annealing step at 300°C for 30 min. The electrical response of this device decreased when compared with the same stack structure without passivation (Figure 6b), confirming that the key factor responsible for the reduced resistance was not the presence of the oxide, but the thermal treatment introduced during its deposition.

To further quantify these differences, Table 1 summarizes the resistivity and TCR values extracted from the experimental RTD measurements. The as-deposited $Si/SiO_2/Pt$ devices exhibit the highest resistivity and the lowest TCR, reflecting the higher density of grain boundaries and structural defects present in the non-annealed Pt film. In contrast, both the $Si/SiO_2/Pt/SiO_2$ and the annealed $Si/SiO_2/Pt$ devices display significantly reduced resistivities together with enhanced TCR values. These values are consistent with the temperature-dependent trends observed in the thin-film annealing study (Figure S3) and confirm that the thermal treatment of the oxide deposition process plays the dominant role in improving the electrical response of the Pt films. The small difference between the numerical and experimental values of the RTD voltages can be attributed to the non-uniformity roughness across the device and uncertainties in the effective wire lengths in the experimental measurements. Nevertheless, both results exhibit a consistent linear trend. Moreover, the purpose of the numerical model is not to exactly replicate the experimental data, but to corroborate that the variations in RTD response arise exclusively from process-induced modifications of Pt resistivity and TCR, rather than from the presence of the oxide layer itself.

This observation directly correlates with the thin-film studies presented in Sections 3.1 and 3.2: annealing at 300°C induces Pt grain growth and defect reduction, lowers sheet resistance, and results in smoother surface morphology. SEM and AFM analyses corroborate these findings, showing that the annealed Pt films display more uniform structures with reduced roughness compared to as-deposited samples.

Overall, these results highlight a crucial point for the design of RTD in OoCs: while the SiO_2 insulating layer is essential for biological isolation and device integration, its PECVD deposition process also introduces a beneficial annealing effect that enhances the electrical characteristics of the Pt film. Consequently, the oxide deposition step not only fulfills a biocompatibility requirement but also improves sensor performance, making it a dual-functional process step.

5 | Discussion

The obtained results demonstrate a clear correlation between the electrical performance of Pt thin-films and their microstructural evolution under thermal treatment. Both sheet resistance and TCR values evolve consistently with the morphological transformations observed by SEM and AFM (Section 3.2). In particular, it was demonstrated that even moderate annealing conditions

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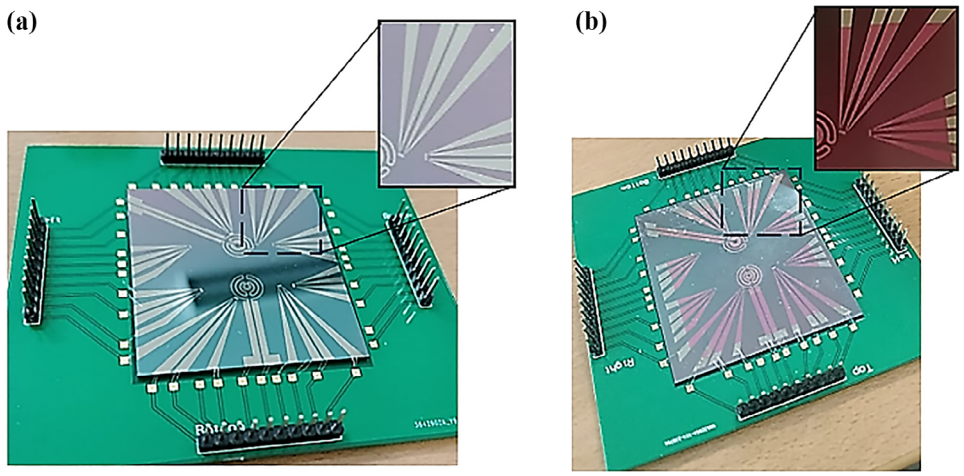


FIGURE 7 | Images of the fabricated RTDs dies assembled on printed circuit boards: (a) without a SiO_2 insulating layer, and (b) with a SiO_2 passivation layer deposited on top of the Pt film.

(300°C for 30 min) significantly reduce resistivity and enhance TCR, confirming that controlled thermal processing can improve Pt film conductivity without the need for high thermal budgets. At annealing temperatures between 100 and 500°C, the resistivity decreases due to stress relaxation and grain growth, leading to improved charge transport across grain boundaries. This finding is consistent with trends reported by Schmid et al. [31], who observed similar improvements in sputtered Pt thin films with thicknesses ranging from 24 to 105 nm after post-deposition annealing.

Consistent with the electrical results, the surface roughness remains relatively stable up to 500°C for both Si/Pt and $Si/SiO_2/Pt$, followed by a gradual increase and a pronounced rise at 900°C (Section 3.2). The stronger roughness evolution observed in the $Si/SiO_2/Pt$ sample at 900°C can be related to enhanced interdiffusion at the SiO_2/Pt interface, promoting grain boundary mobility and surface restructuring. This morphology is consistent with literature reports describing Ostwald ripening and film dewetting in Pt thin films subjected to high-temperature annealing, ultimately leading to discontinuous morphologies and higher surface roughness.

In agreement with these findings, Schössler et al. [21] observed that sputtered Pt films on Si/SiO_2 exhibited a reduction in resistivity from 16.8 to 12.7 μΩ·cm, and an increase in TCR from 2180 to 2850 ppm·K^{-1} after annealing between 450 and 800°C for 1 h. Although our resistivity remains slightly higher, consistent with the shorter annealing time, our improvement confirms that grain growth and stress relaxation begin at lower thermal budgets. Schössler et al. also reported pronounced grain coarsening above 600°C due to recrystallization processes, which aligns with our SEM observations of significant grain enlargement and roughness increase at 700–900°C.

Comparable trends were also reported by Tiggelaar et al. [13], who systematically analyzed the structural and electrical stability of sputtered Pt thin-films with different adhesion layers (Ta, Ti, or none) after annealing between 250 and 950°C. Their results are consistent with our findings, where 200 nm Pt films (with 5 nm Ta adhesion layer) exhibited a significant reduction in resistivity after annealing at 700°C, followed by pronounced morphological degradation at 900°C. The lower TCR values obtained here ($1.63–1.94 \times 10^{-3}°C^{-1}$) compared to $2.3–3.7 \times 10^{-3}°C^{-1}$ reported by Tiggelaar et al. [13], can be attributed to the shorter annealing duration (30 min vs. 1 h), the thinner adhesion layer, and the temperature range (35–45°C) used for TCR evaluation. These results indicate that, while moderate thermal annealing promotes conductivity through stress relaxation and grain coarsening, higher annealing temperatures lead to surface instability and film discontinuity.

The beneficial role of the SiO_2 layer is further supported by Golosov et al. [32], who demonstrated that SiO_2 acts as an effective diffusion barrier, preventing Pt silicide formation and preserving the structural and electrical integrity of Pt films up to approximately 800°C. In contrast, Pt films deposited directly on Si exhibited early degradation above 500–600°C, due to interdiffusion and silicidation processes, roughening, and void formation [32]. These findings align well with our results presented in Sections 3.1 and 3.2, where the $Si/SiO_2/Pt$ samples retained lower roughness and resistivity at moderate annealing temperatures (400°C–700°C) compared to Si/Pt samples. The improved performance of the oxide-based configuration thus confirms the critical function of SiO_2, as both an electrical insulator and a diffusion barrier, ensuring the long-term stability of Pt films under thermal stress, a key requirement for reliable sensor integration in OoC platforms.

Beyond these material-level improvements, the experimental results demonstrate that the fabrication-related thermal budget directly affects device performance. Compared with the as-deposited $Si/SiO_2/Pt$ RTDs, the fabrication-compatible thermal treatment associated with SiO_2 passivation reduced the electrical resistivity by approximately 28% (from 6.85×10^{-7} to 4.92×10^{-7} Ω·m) while increasing the TCR by approximately 16% (from 0.00163 to 0.00189°C^{-1}). When the same thermal treatment was applied without the oxide layer, the TCR increased by approximately 19% (to 0.00194°C^{-1}), indicating that the electrical improvement primarily results from the thermal budget itself rather than from the dielectric layer.

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This improvement is directly reflected in the simulated RTD response. For a constant excitation current, the voltage output varies linearly with temperature, and the higher TCR translates into a larger voltage variation per degree Celsius. Accordingly, the simulated sensitivity increased from approximately 0.80 to 0.93 $mV \cdot °C^{-1}$, corresponding to an improvement of about 16%. Consequently, the same physiological temperature variation generates a larger electrical output signal, enhancing temperature resolution without modifying the RTD geometry or readout circuitry. For OoC systems, where physiological temperature must be tightly controlled to preserve cell viability, metabolism, and drug response, this increased sensitivity enables the detection of smaller temperature variations while maintaining the same sensor architecture and acquisition electronics, thereby improving the accuracy of thermal monitoring without increasing device complexity.

From an OoC perspective, these findings are particularly relevant because Pt RTDs are typically fabricated before dielectric encapsulation and are therefore inevitably exposed to the thermal budget required for oxide deposition. Rather than representing solely a fabrication constraint, this mandatory process can be exploited as an in situ annealing treatment that simultaneously provides electrical insulation, biocompatible encapsulation, and optimization of the Pt electrical properties. Although Pt films directly deposited on Si remain functional under moderate processing conditions, their higher susceptibility to Pt–Si interdiffusion and thermally induced morphological degradation makes the $Si/SiO_2/Pt$ architecture a more robust solution for integrated into OoC devices, where dielectric encapsulation and subsequent fabrication steps are unavoidable. As a result, the oxide-buffered configuration provides greater long-term electrical stability while maintaining the enhanced post-fabrication sensitivity, making it better suited to multilayer OoC fabrication workflows in which metallic sensors must preserve stable electrical performance throughout successive processing and encapsulation steps.

Therefore, these results establish a practical fabrication window for integrated Pt RTDs: moderate thermal budgets ($\leq$300°C for 30 min) associated with SiO_2 passivation promote stress relaxation and grain coarsening, ensuring stable electrical performance and enhanced sensor sensitivity, whereas higher thermal excursions (>700°C) induce morphological instability and electrical degradation. More broadly, this work demonstrates that fabrication-related thermal budgets should be considered not only as processing constraints but also as design parameters that can be intentionally exploited to optimize device performance under realistic OoC manufacturing conditions.

Overall, the present study establishes a direct processing–microstructure–device performance relationship, demonstrating that controlled thermal processing simultaneously improves Pt thin-film properties and enhances the reliability, sensitivity and manufacturability of integrated temperature sensors for OoC applications. The experimentally validated processing window and material configuration identified in this work provide practical design guidelines for the reliable integration of Pt RTDs into multilayer OoC devices, where thermal processing is an inherent part of the fabrication workflow.

6 | Conclusion

This work investigated the influence of thermal processing and oxide integration on the electrical and morphological stability of sputtered Pt thin-films and their translation into functional RTDs for OoC platforms. By combining thin-film annealing studies up to 900°C with microstructural (SEM, AFM, EDX), electrical, device-level, and numerical analyses, we established a direct and quantitative link between fabrication conditions, material properties, and sensor-level performance, addressing a critical knowledge gap in the integration of metallic sensors into microfluidic and OoC systems.

The results demonstrate that moderate thermal treatments, representative of the thermal budget imposed during PECVD oxide deposition (≈300°C for 30 min), significantly improve Pt film conductivity and temperature sensitivity, driven by stress relaxation and grain coarsening, while preserving film continuity and surface integrity. In contrast, excessive thermal exposure (>700°C) induces surface roughening, agglomeration and, in the absence of an oxide interlayer, Pt–Si interdiffusion and silicide formation, leading to electrical degradation and morphological instability that compromise device reliability.

The presence of a SiO_2 interlayer between the Si substrate and the Pt film plays a critical role in preserving electrical and structural stability by acting as an effective diffusion barrier and preventing silicide formation. Although agglomeration occurs at 900°C even in oxide-buffered stacks, EDX analysis confirms that the Pt composition remains preserved, indicating predominantly morphological rather than chemical degradation. This explains the superior electrical stability of $Si/SiO_2/Pt$ stacks throughout the thermal processing window relevant for OoC fabrication.

At the device level, both numerical simulations and experimental measurements in the physiological temperature range (35-45°C) confirm that the presence of an oxide passivation layer does not intrinsically affect the electrical response of the RTD. Instead, the improved performance of passivated devices is originated from the annealing effect inherently introduced during oxide (or nitride) deposition. Rather than requiring an additional post-deposition annealing step, this mandatory fabrication process can be exploited as an in situ annealing treatment that simultaneously provides electrical insulation, biocompatible encapsulation, and optimization of the Pt electrical properties. Fully passivated RTDs, subjected to multiple thermal cycles, exhibit the lowest resistivity and enhanced TCR, demonstrating the effectiveness of this dual-function fabrication strategy.

Overall, this study highlights that, in OoC-integrated Pt RTDs, the thermal history imposed during fabrication is the dominant factor governing electrical performance. These insights define a practical and safe processing window for Pt-based temperature sensors, where moderate thermal budgets enhance performance, reduce fabrication uncertainty, and improve device reliability without increasing process complexity. The methodology and conclusions presented here provide experimentally validated design guidelines and a predictive framework for the reliable integration of thin-film metallic temperature sensors in OoC and related microfabricated platforms.

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Acknowledgements

The authors acknowledge the financial support of the project HfPT – Health from Portugal, with reference n.ž C644937233–00000047, cofunded by Component C5 – Capitalisation and Business Innovation under the Portuguese Resilience and Recovery Plan, through the Next GenerationEU Fund. This work was supported by the project PTDC/EEI-EEE/2846/2021 (https://doi.org/10.54499/PTDC/EEI-EEE/2846/2021), through national funds (OE), within the scope of the Scientific Research and Technological Development Projects (IC&DT) programme in all scientific domains (PTDC), through the Foundation for Science and Technology, I.P. (FCT, I.P.). This work was also partially supported by the projects COMPETE2030-FEDER-00689800, reference 2023.16645.ICDT (DOI https://doi.org/10.54499/2023.16645.ICDT), and COMPETE2030-FEDER-00712000, co-financed by the European Regional Development Fund (FEDER) and national funds through the Foundation for Science and Technology (FCT), under the Innovation and Digital Transition Programme – Compete2030. The authors also acknowledge the FCT financial support within the scope of the R&D Unit Project UID/4436/2025, LA/P/0029/2020. Gabriel M. Ferreira thanks the FCT for his Ph.D. grant, reference 2022.10519.BD. P.J.S. thanks the FCT for the contract funding provided through 2021.01086.CEECIND (https://doi.org/10.54499/2021.01086.CEECIND/CP1664/CT0008).
The authors thank Aritz Retolaza for his help with the annealing measurements.

Conflicts of Interest

The authors declare no conflicts of interest.

Data Availability Statement

The data that support the findings of this study are available on request from the corresponding author. The data are not publicly available due to privacy or ethical restrictions.

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